

## 54ACTQ657

# Quiet Series Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE® Outputs

### General Description

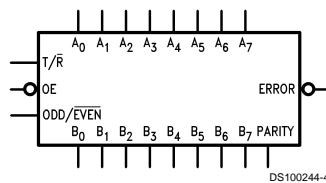
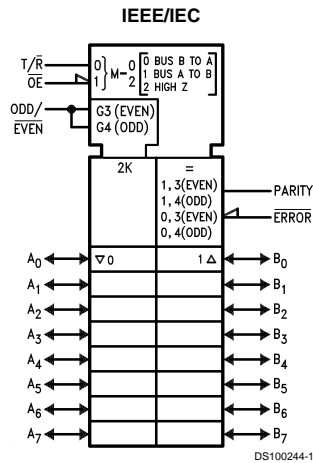
The ACTQ657 contains eight non-inverting buffers with TRI-STATE outputs and an 8-bit parity generator/checker. Intended for bus oriented applications, the device combines the '245 and the '280 functions in one package.

The ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

### Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Combines the '245 and the '280 functions in one package
- Outputs source/sink 24 mA
- 'ACTQ has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD) 5962-92197

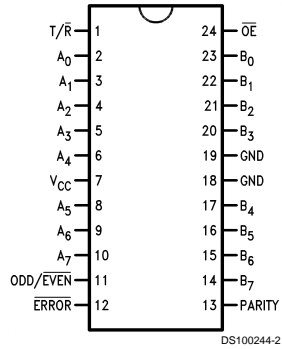
### Logic Symbols



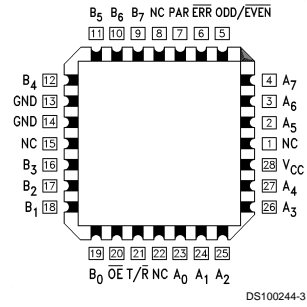
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 TRI-STATE® is a registered trademark of National Semiconductor Corporation.  
 FACT Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

## Connection Diagrams

**Pin Assignment  
for DIP and Flatpak**



**Pin Assignment  
for LCC**



Pin Names	Description
A <sub>0</sub> –A <sub>7</sub>	Data Inputs/TRI-STATE Outputs
B <sub>0</sub> –B <sub>7</sub>	Data Inputs/TRI-STATE Outputs
T/ $\bar{R}$	Transmit/Receive Input
$\bar{O}E$	Enable Input
PARITY	Parity Input/TRI-STATE Output
ODD/ $\bar{E}VEN$	ODD/ $\bar{E}VEN$ Parity Input
$\bar{E}RROR$	Error TRI-STATE Output

## Functional Description

The Transmit/Receive ( $\overline{T/R}$ ) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from the A port to the B port; Receive (active LOW) enables data from the B port to the A port.

The Output Enable ( $\overline{OE}$ ) input disables the parity and  $\overline{ERROR}$  outputs and both the A and B ports by placing them in a HIGH-Z condition when the Output Enable input is HIGH.

When transmitting ( $\overline{T/R}$  HIGH), the parity generator detects whether an even or odd number of bits on the A port are HIGH and compares these with the condition of the parity select (ODD/EVEN). If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode ( $\overline{T/R}$  LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, then  $\overline{ERROR}$  will be HIGH to indicate no error. If an odd number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the  $\overline{ERROR}$  will be LOW indicating an error.

## Functional Description (Continued)

### Function Table

Number of Inputs That Are High	Inputs			Input/Output	Outputs	
	$\overline{OE}$	$T/R$	ODD/EVEN	Parity	ERROR	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
Immaterial	H	X	X	Z	Z	Z

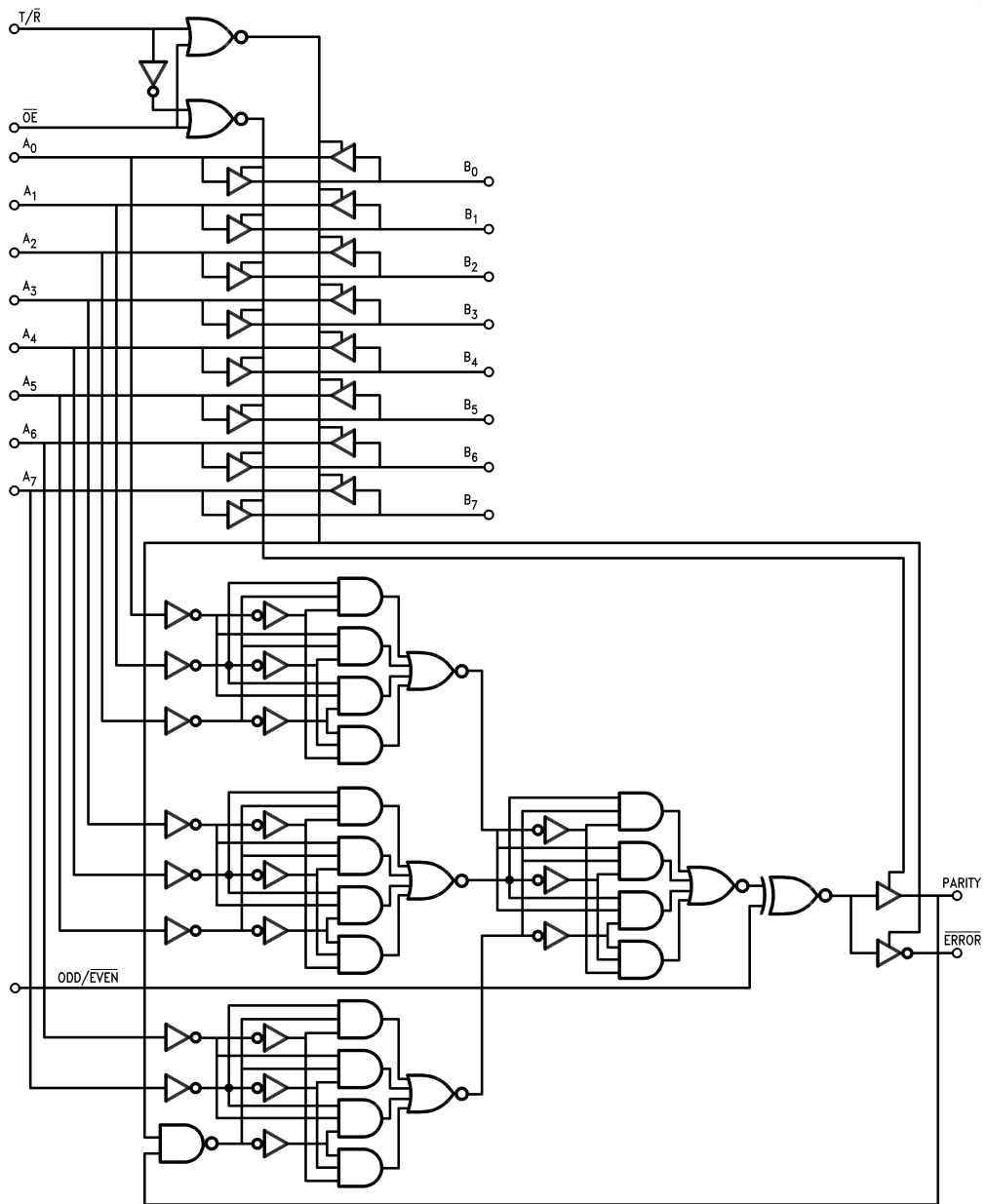
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

### Function Table

Inputs		Outputs
$\overline{OE}$	$T/R$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

## Functional Block Diagram



2 GROUND PINS  
1 V<sub>CC</sub> PIN

DS100244-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-up Source or Sink Current	±300 mA

Junction Temperature ( $T_J$ )

CDIP

175°C

### Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54ACTQ	-55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

### DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54ACTQ	Units	Conditions
			$T_A =$		
			Guaranteed Limits		
$V_{IH}$	Minimum High Level Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
$V_{IL}$	Maximum Low Level Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
$V_{OH}$	Minimum High Level Output Voltage	4.5	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.4		
		4.5	3.70	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		5.5	4.70		
$V_{OL}$	Maximum Low Level Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current ( $T/\bar{R}$ , $\overline{OE}$ , ODD/EVEN Inputs)	5.5	±1.0	μA	$V_I = V_{CC}, GND$
$I_{OZT}$	Maximum I/O Leakage Current ( $A_n$ , $B_n$ Inputs)	5.5	±11.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$
$I_{CCT}$	Maximum $I_{CC}$ /Input	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$

## DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54ACTQ	Units	Conditions
			T <sub>A</sub> = -55°C to +125°C		
			Guaranteed Limits		
I <sub>OLD</sub>	Minimum Dynamic Output Current (Note 3)	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>		5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	160.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 4)
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.5	V	(Note 5)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-1.2	V	(Note 5)

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

**Note 5:** Max number of outputs defined as (n). n-1 Data Inputs are driven 0V to 3V; one output @ GND.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 6)	54ACTQ		Units
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to B <sub>n</sub> , B <sub>n</sub> to A <sub>n</sub>	5.0	1.5	9.0	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to Parity	5.0	1.5	13.5	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay ODD/EVEN to PARITY	5.0	1.5	10.5	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay ODD/EVEN to ERROR	5.0	1.5	11.0	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay B <sub>n</sub> to ERROR	5.0	1.5	13.5	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay PARITY to ERROR	5.0	1.5	10.5	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time OE to A <sub>n</sub> /B <sub>n</sub>	5.0	1.5	11.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time OE to A <sub>n</sub> /B <sub>n</sub>	5.0	1.5	9.0	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time OE to ERROR (Note 7)	5.0	1.5	11.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time OE to ERROR	5.0	1.5	9.0	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time OE to PARITY	5.0	1.5	11.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time OE to PARITY	5.0	1.5	8.5	ns

**Note 6:** Voltage Range 5.0 is 5.0V ±0.5V

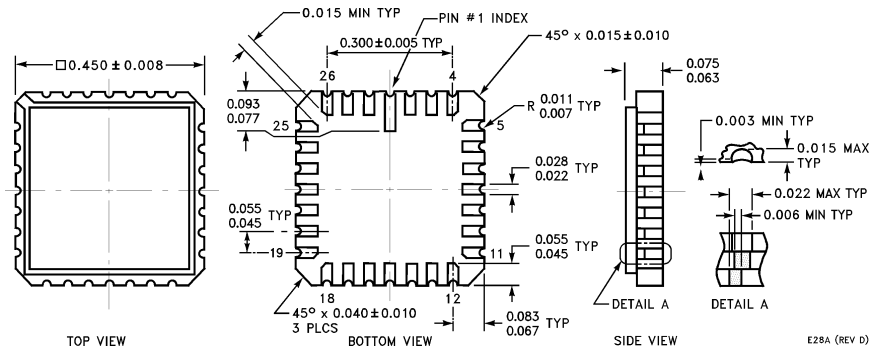
**Note 7:** These delay times reflect the TRI-STATE recovery time only and not the signal time through the buffers or the parity check circuitry. To assure VALID information at the ERROR pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the ERROR output after the ERROR pin has been enabled (Output Enable times). VALID data at the ERROR pin ≥ (A to PARITY) + (Output Enable Time).

## Capacitance

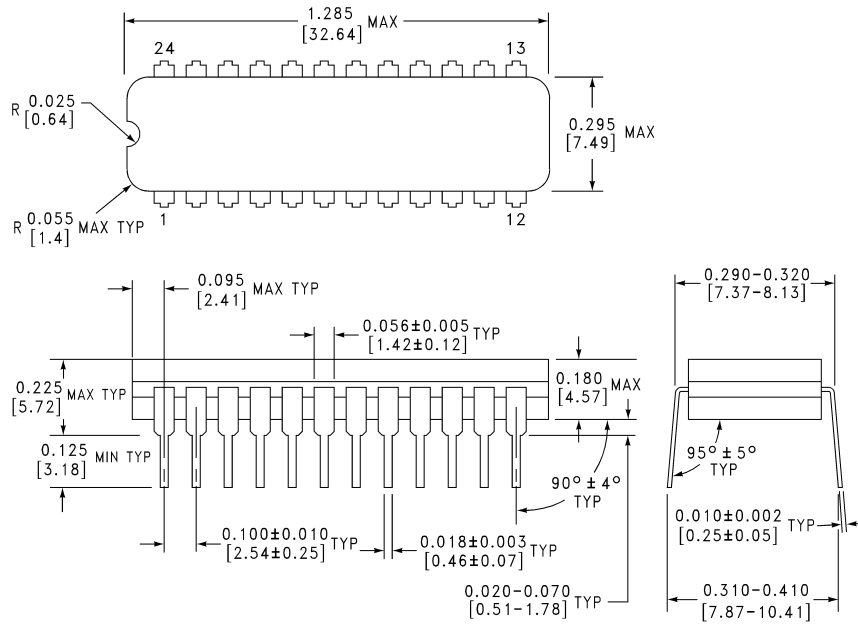
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	160.0	pF	V <sub>CC</sub> = 5.0V



**Physical Dimensions** inches (millimeters) unless otherwise noted

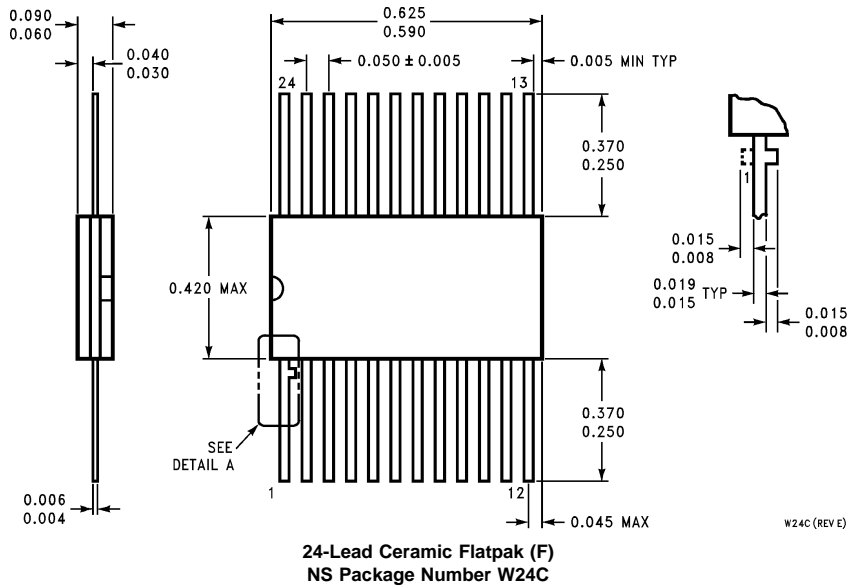


**28-Terminal Ceramic Leadless Chip Carrier (L)  
 NS Package Number E28A**



**24-Lead Slim Ceramic (0.300" Wide)  
 Dual-In-Line Package (SD)  
 NS Package Number J24F**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



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