Signetics

54F432
Latch

Multi-Mode Buffered Latch, INV (3-State)

Product Specification

Military Logic Products

FEATURES

- **Status flip-flop for interrupt commands**
- **Asynchronous or latched receiver mode**
- **Inverting**
- **3-State outputs**
- **300mil-wide Slim DIP package**
- **Functional equivalent to Intel 8212 except that 54F432 has inverting outputs**

DESCRIPTION

The 54F432 has 8 data latches with 3-State output buffers. Also included is a status flip-flop for providing service-busy or request-interrupt commands. Separate Mode (M) and Select ($\overline{S}_0$, S_1) inputs allow data to be stored with the outputs enabled or disabled. The device can also be operated in a fully transparent mode.

This device is functionally equivalent to the Intel 8212 except that the 54F432 has inverting outputs.

ORDERING INFORMATION

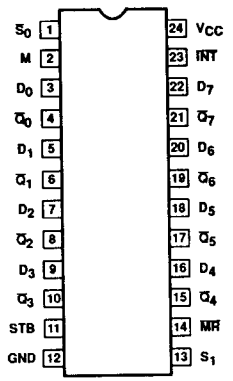
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54F432/BLA
24-Pin Ceramic FlatPack	54F432/BKA
28-Pin Ceramic LLCC	54F432/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{S}_0$, S_1	Select inputs	1.0/1.0	20μA/0.6mA
STB	Strobe input	1.0/1.0	20μA/0.6mA
M	Mode Control input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input	1.0/1.0	20μA/0.6mA
$\overline{INT}$	Interrupt output	50/33	1.0mA/20mA
Q_0 - Q_7	Data latched outputs	150/33	3.0mA/20mA

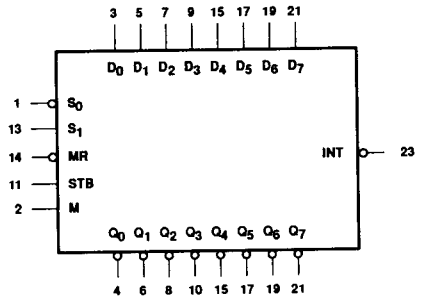
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



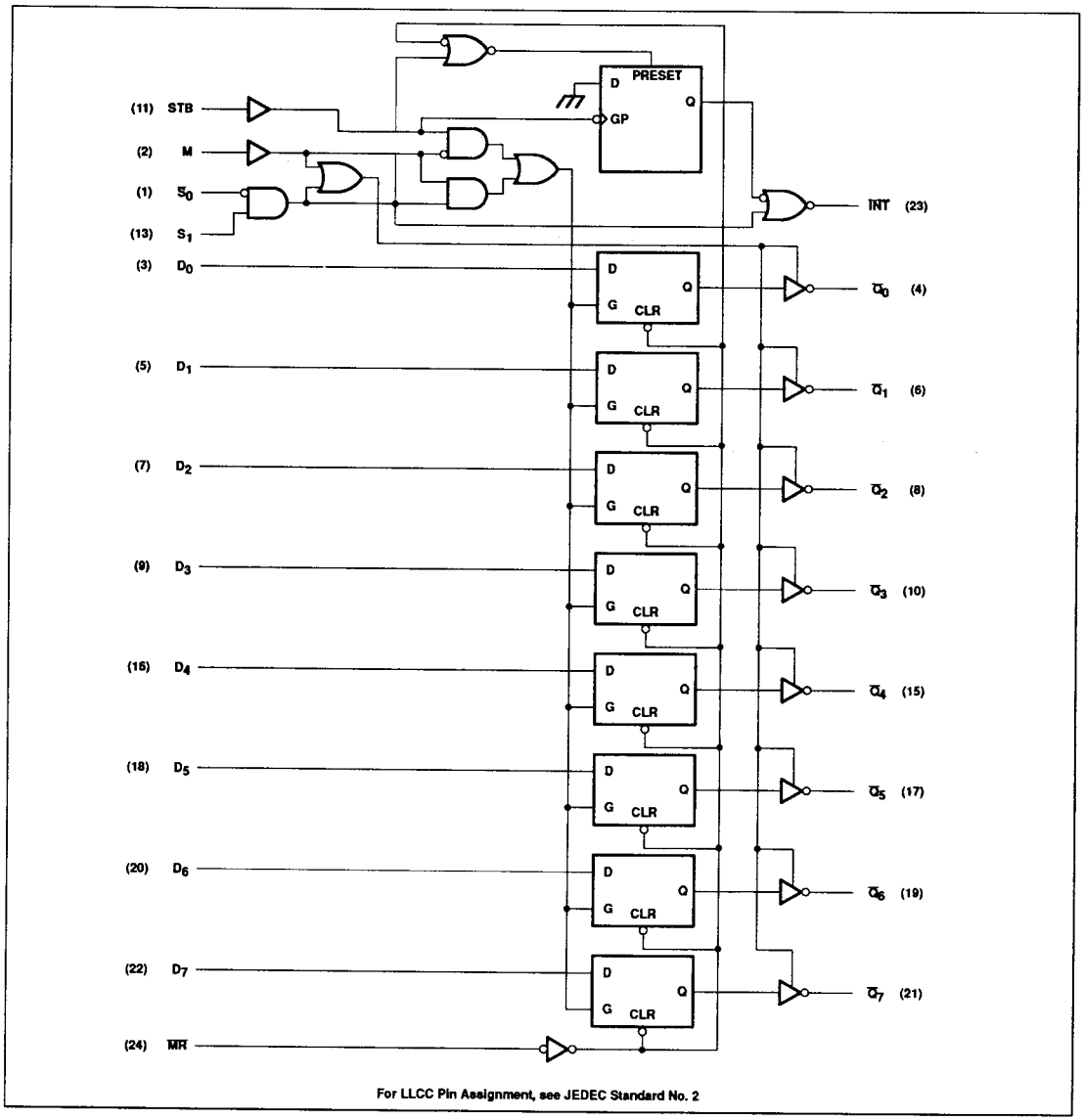
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC Pin Assignment, see JEDEC Standard No. 2

Latch

54F432

FUNCTIONAL DESCRIPTION

This high-performance eight-bit parallel expandable buffer register incorporates mode selection inputs and an edge-trigger status flip-flop designed specifically for implementing bus organized input/output ports. The 3-State data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable input, G, is High and the outputs are enabled. Latch transparency is selected by the mode control (M), select ($\overline{S}_0$ and S_1), and the strobe (STB) inputs and during transparency each data output (Q_n) follows its respective data input (D_n). This mode of operation can be terminated by clearing, deselecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode, M=L, the eight data latch inputs are enabled when the strobe is High regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken Low, the latches will store the most recently set up data.

In the output mode, M=H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S}_0$ and S_1) inputs. See the Data Latches Function Table.

STATUS FLIP-FLOP FUNCTION TABLE

INPUTS				OUTPUT
$\overline{MR}$	$\overline{S}_0$	S_1	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low clock transition

DATA LATCHES FUNCTION TABLE

INPUTS					DATA IN	DATA OUT	OPERATING MODE
$\overline{MR}$	M	$\overline{S}_0$	S_1	STB			
L L	H L	H L	X H	X L	X X	H H	Clear
X X	L L	X H	L X	X X	X X	Z Z	De-select
H H	H L	H L	X H	X L	X X	$\overline{Q}_0$ $\overline{Q}_0$	Hold
H H	H H	L L	H H	X X	L H	H L	Data Bus
H H	L L	L L	H H	H H	L H	H L	Data Bus

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5	mA
V_O	Voltage applied to output in High output state range		-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	$\overline{INT}$	40	mA
		Q_0 - Q_7	40	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{INT}$			-1.0	mA
		Q_0, Q_7			-3.0	mA
I_{OL}	Low-level output current	$\overline{INT}$			20	mA
		Q_0, Q_7			20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max,	I_{OH} = -1mA	2.5			V
		V_{IH} = Min	I_{OH} = -3mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max	±10% V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OZH}	Off-state output current High-level voltage applied	V_{CC} = Max, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current Low-level voltage applied	V_{CC} = Max, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max, V_O = 0.0V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max		40	55	mA
		I_{CCL}			50	70	mA
		I_{CCZ}			50	65	mA

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	4.5 2.5	7.5 4.5	10.5 7.0	4.0 2.5	13.0 6.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 or STB to Q_n	Waveform 1, 2	8.5 6.0	14.0 9.5	17.0 13.0	8.0 5.5	24.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$ or S_1 to $\overline{INT}$	Waveform 1, 2	3.0 3.5	6.0 6.5	9.5 10.0	2.5 3.0	10.5 10.5	ns ns
t_{PLH}	Propagation delay $\overline{MP}$ to Q_n	Waveform 2	8.0	12.0	16.0	7.5	18.5	ns
t_{PHL}	Propagation delay STB to $\overline{INT}$	Waveform 2	7.0	10.0	13.5	6.5	14.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{S}_0$ or S_1 to Q_n	Waveform 5 Waveform 6	6.0 6.0	9.0 11.0	12.5 14.0	5.5 5.5	15.5 15.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level $\overline{S}_0$ or S_1 to Q_n	Waveform 5 Waveform 6	4.0 6.0	7.5 11.5	11.5 15.0	3.5 5.5	12.5 17.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level M to Q_n	Waveform 5 Waveform 6	5.0 6.0	7.5 8.0	11.0 11.5	4.5 5.5	12.0 13.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level M to Q_n	Waveform 5 Waveform 6	3.5 6.0	6.0 10.0	9.5 13.0	3.0 5.5	10.5 15.0	ns ns

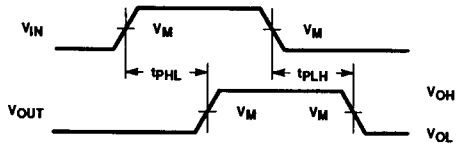
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to $\overline{S}_0$, S_1, STB or M	Waveform 3	0 0			1.0 1.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low D_n to $\overline{S}_0$, S_1, STB or M	Waveform 3	9.0 8.0			9.5 9.5		ns ns
t_w(H) t_w(L)	$\overline{S}_0$, S_1 or STB Pulse width High or Low	Waveform 3	8.0 8.0			9.0 9.0		ns ns
t_w(L)	$\overline{MR}$ Pulse width	Waveform 4	8.0			9.0		ns
t_{rec}	Recovery time	Waveform 4	0			0		ns

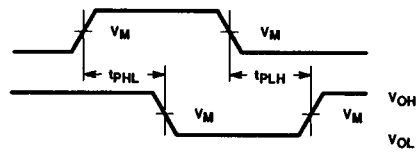
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

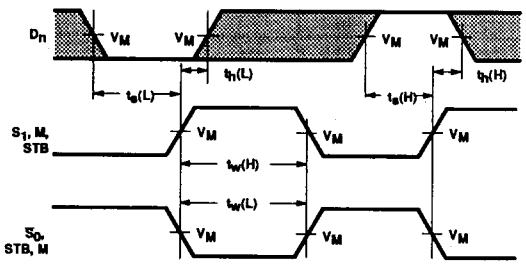
AC WAVEFORMS



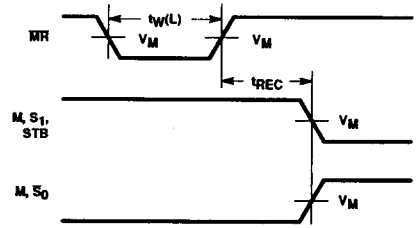
Waveform 1. Propagation Delay for Non-Inverting Outputs



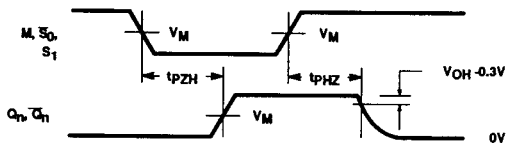
Waveform 2. Propagation Delay for Inverting Outputs



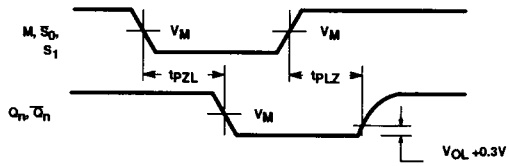
Waveform 3. Setup and Hold Times



Waveform 4. Recovery Times



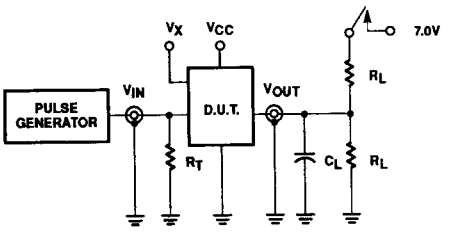
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



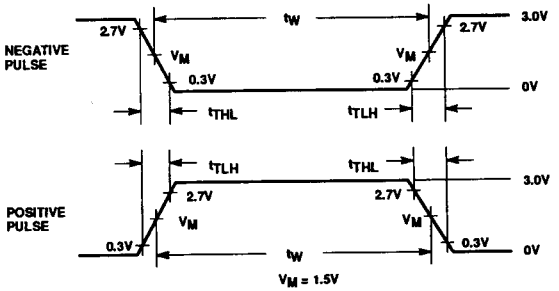
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.