64M-BIT [4M x 16] CMOS EQUAL SECTOR FLASH MEMORY

FEATURES

GENERAL FEATURES

- 4,194,304 x 16 word structure
- Sector Structure
  - 128 Equal Sectors with 32K word each
- Extra 128-word sector for security
  - Features factory locked and identifiable, and customer lockable
- Sector Groups Protection / Chip Unprotect
  - Provides sector group protect function to prevent program or erase operation in the protected sector group
  - Provides chip unprotect function to allow code changing
  - Provides temporary sector group unprotect function for code changing in previously protected sector groups
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 250mA from -1V to Vcc + 1V
- Low Vcc write inhibit : Vcc <= 1.5V
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash

PERFORMANCE

- High Performance
  - Fast access time: 90/120ns
  - Fast program time: 11us/word (typical)
  - Fast erase time: 0.9s/sector, 45s/chip (typical)
- Low Power Consumption
  - Low active read current: 9mA (typical) at 5MHz
  - Low standby current: 0.2uA (typical)
- Minimum 100,000 erase/program cycle
- 20 years data retention

SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

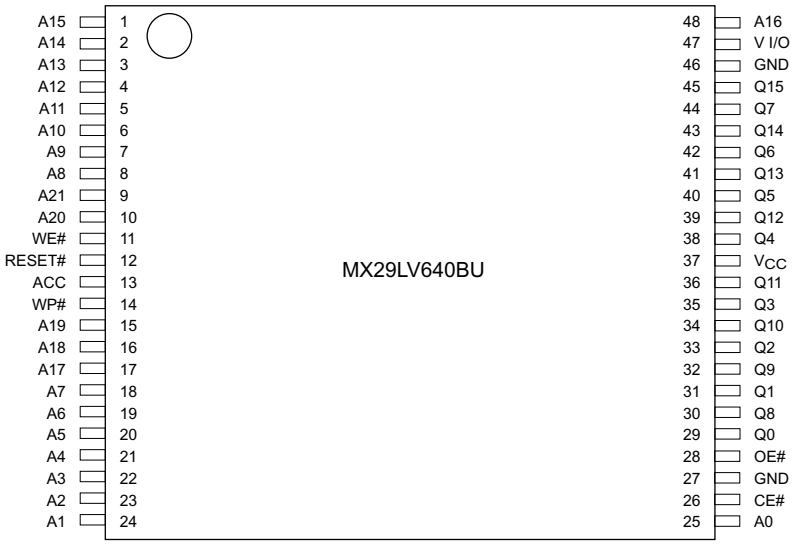
- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- ACC input pin
  - Provides accelerated program capability
- WP# pin
  - Write protect the first sector regardless of sector protect/unprotect status

PACKAGE

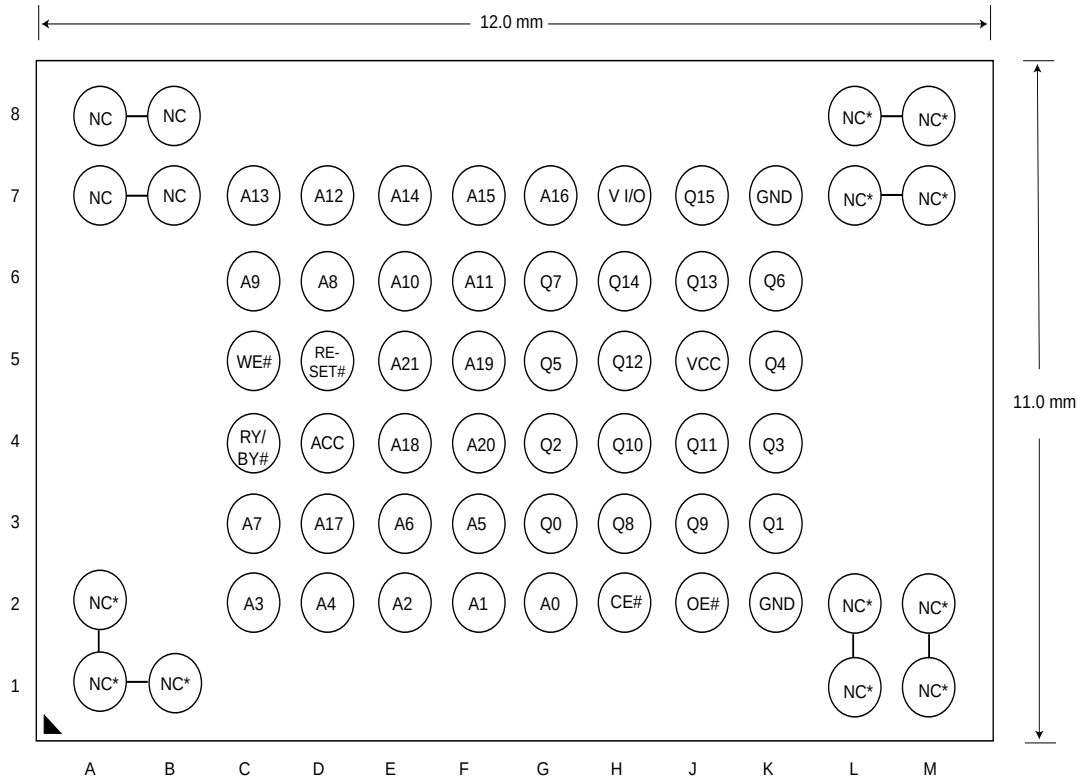
- 48-Pin TSOP
- 63-Ball CSP
- **All Pb-free devices are RoHS Compliant**
- **All non RoHS Compliant devices are not recommeded for new design in**

PIN CONFIGURATION

48 TSOP



63 Ball CSP (Top View, Ball Down)

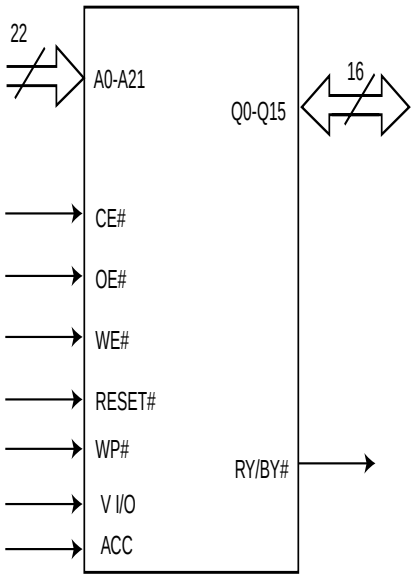


* Ball are shorted together via the substrate but not connected to the die.

PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A21	Address Input
Q0~Q15	16 Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
WP#	Hardware Write Protect Input
RY/BY#	Read/Busy Output
VCC	+3.0V single power supply
ACC	Hardware Acceleration Pin
GND	Device Ground
NC	Pin Not Connected Internally
V I/O	Input/Output buffer (2.7V~3.6V) this input should be tied directly to VCC

LOGIC SYMBOL



BLOCK DIAGRAM

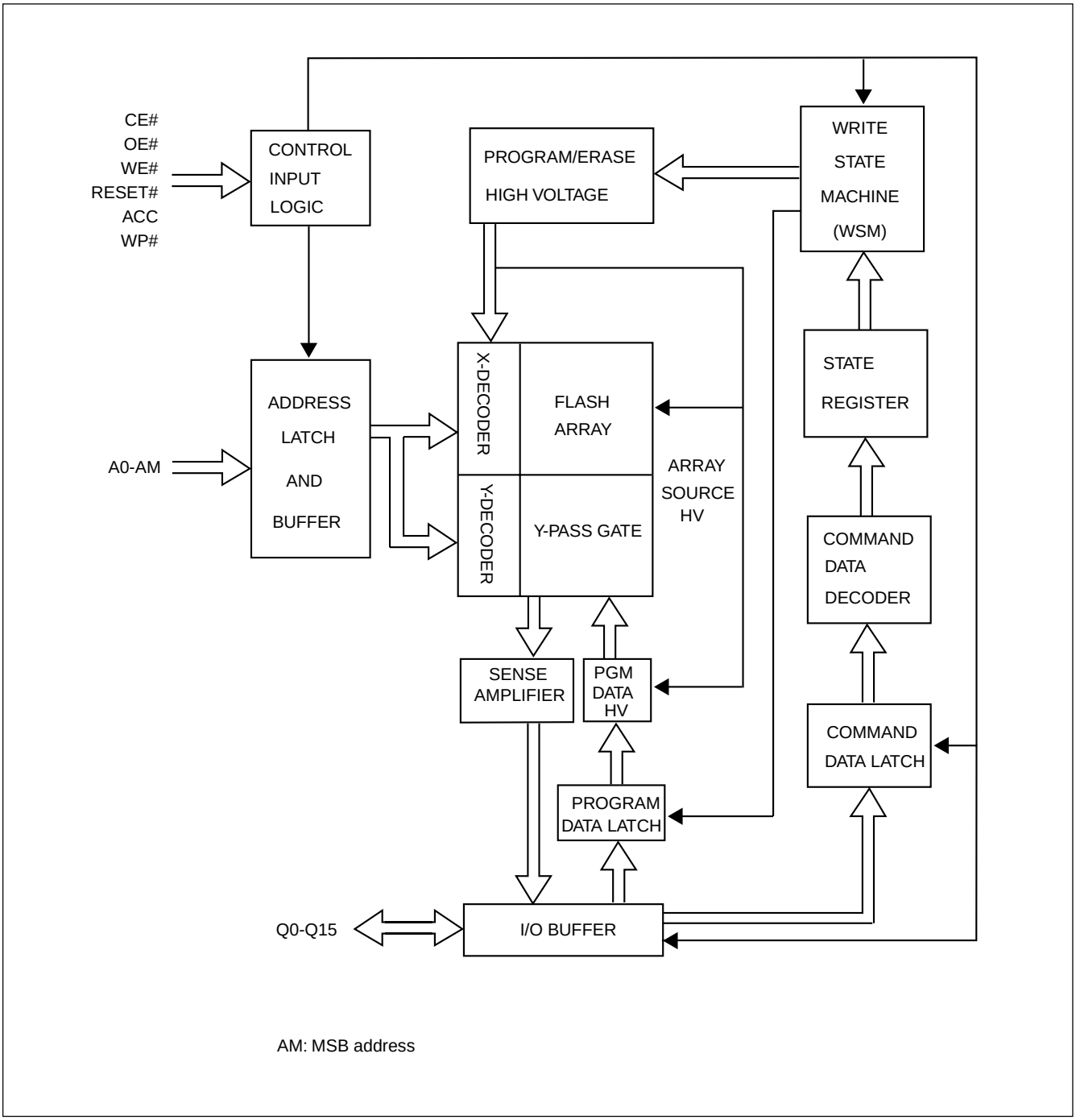


Table 1. BLOCK STRUCTURE

Sector	A21	A20	A19	A18	A17	A16	A15	16-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	000000-007FFF
SA1	0	0	0	0	0	0	1	008000-00FFFF
SA2	0	0	0	0	0	1	0	010000-017FFF
SA3	0	0	0	0	0	1	1	018000-01FFFF
SA4	0	0	0	0	1	0	0	020000-027FFF
SA5	0	0	0	0	1	0	1	028000-02FFFF
SA6	0	0	0	0	1	1	0	030000-037FFF
SA7	0	0	0	0	1	1	1	038000-03FFFF
SA8	0	0	0	1	0	0	0	040000-047FFF
SA9	0	0	0	1	0	0	1	048000-04FFFF
SA10	0	0	0	1	0	1	0	050000-057FFF
SA11	0	0	0	1	0	1	1	058000-05FFFF
SA12	0	0	0	1	1	0	0	060000-067FFF
SA13	0	0	0	1	1	0	1	068000-06FFFF
SA14	0	0	0	1	1	1	0	070000-077FFF
SA15	0	0	0	1	1	1	1	078000-07FFFF
SA16	0	0	1	0	0	0	0	080000-087FFF
SA17	0	0	1	0	0	0	1	088000-08FFFF
SA18	0	0	1	0	0	1	0	090000-097FFF
SA19	0	0	1	0	0	1	1	098000-09FFFF
SA20	0	0	1	0	1	0	0	0A0000-0A7FFF
SA21	0	0	1	0	1	0	1	0A8000-0AFFFF
SA22	0	0	1	0	1	1	0	0B0000-0B7FFF
SA23	0	0	1	0	1	1	1	0B8000-0BFFFF
SA24	0	0	1	1	0	0	0	0C0000-0C7FFF
SA25	0	0	1	1	0	0	1	0C8000-0CFFFF
SA26	0	0	1	1	0	1	0	0D0000-0D7FFF
SA27	0	0	1	1	0	1	1	0D8000-0DFFFF
SA28	0	0	1	1	1	0	0	0E0000-0E7FFF
SA29	0	0	1	1	1	0	1	0E8000-0EFFFF
SA30	0	0	1	1	1	1	0	0F0000-0F7FFF
SA31	0	0	1	1	1	1	1	0F8000-0FFFFF
SA32	0	1	0	0	0	0	0	100000-10FFFF
SA33	0	1	0	0	0	0	1	108000-10FFFF
SA34	0	1	0	0	0	1	0	110000-117FFF
SA35	0	1	0	0	0	1	1	118000-11FFFF
SA36	0	1	0	0	1	0	0	120000-127FFF
SA37	0	1	0	0	1	0	1	128000-12FFFF

Sector	A21	A20	A19	A18	A17	A16	A15	16-bit Address Range (in hexadecimal)
SA38	0	1	0	0	1	1	0	130000-137FFF
SA39	0	1	0	0	1	1	1	138000-13FFFF
SA40	0	1	0	1	0	0	0	140000-147FFF
SA41	0	1	0	1	0	0	1	148000-14FFFF
SA42	0	1	0	1	0	1	0	150000-157FFF
SA43	0	1	0	1	0	1	1	158000-15FFFF
SA44	0	1	0	1	1	0	0	160000-167FFF
SA45	0	1	0	1	1	0	1	168000-16FFFF
SA46	0	1	0	1	1	1	0	170000-177FFF
SA47	0	1	0	1	1	1	1	178000-17FFFF
SA48	0	1	1	0	0	0	0	180000-187FFF
SA49	0	1	1	0	0	0	1	188000-18FFFF
SA50	0	1	1	0	0	1	0	190000-197FFF
SA51	0	1	1	0	0	1	1	198000-19FFFF
SA52	0	1	1	0	1	0	0	1A0000-1A7FFF
SA53	0	1	1	0	1	0	1	1A8000-1AFFFF
SA54	0	1	1	0	1	1	0	1B0000-1B7FFF
SA55	0	1	1	0	1	1	1	1B8000-1BFFFF
SA56	0	1	1	1	0	0	0	1C0000-1C7FFF
SA57	0	1	1	1	0	0	1	1C8000-1CFFFF
SA58	0	1	1	1	0	1	0	1D0000-1D7FFF
SA59	0	1	1	1	0	1	1	1D8000-1DFFFF
SA60	0	1	1	1	1	0	0	1E0000-1E7FFF
SA61	0	1	1	1	1	0	1	1E8000-1EFFFF
SA62	0	1	1	1	1	1	0	1F0000-1F7FFF
SA63	0	1	1	1	1	1	1	1F8000-1FFFFF
SA64	1	0	0	0	0	0	0	200000-207FFF
SA65	1	0	0	0	0	0	1	208000-20FFFF
SA66	1	0	0	0	0	1	0	210000-217FFF
SA67	1	0	0	0	0	1	1	218000-21FFFF
SA68	1	0	0	0	1	0	0	220000-227FFF
SA69	1	0	0	0	1	0	1	228000-22FFFF
SA70	1	0	0	0	1	1	0	230000-237FFF
SA71	1	0	0	0	1	1	1	238000-23FFFF
SA72	1	0	0	1	0	0	0	240000-247FFF
SA73	1	0	0	1	0	0	1	248000-24FFFF
SA74	1	0	0	1	0	1	0	250000-257FFF
SA75	1	0	0	1	0	1	1	258000-25FFFF
SA76	1	0	0	1	1	0	0	260000-267FFF
SA77	1	0	0	1	1	0	1	268000-26FFFF

Sector	A21	A20	A19	A18	A17	A16	A15	16-bit Address Range (in hexadecimal)
SA78	1	0	0	1	1	1	0	270000-277FFF
SA79	1	0	0	1	1	1	1	278000-27FFFF
SA80	1	0	1	0	0	0	0	280000-287FFF
SA81	1	0	1	0	0	0	1	288000-28FFFF
SA82	1	0	1	0	0	1	0	290000-297FFF
SA83	1	0	1	0	0	1	1	298000-29FFFF
SA84	1	0	1	0	1	0	0	2A0000-2A7FFF
SA85	1	0	1	0	1	0	1	2A8000-2AFFFF
SA86	1	0	1	0	1	1	0	2B0000-2B7FFF
SA87	1	0	1	0	1	1	1	2B8000-2BFFFF
SA88	1	0	1	1	0	0	0	2C0000-2C7FFF
SA89	1	0	1	1	0	0	1	2C8000-2CFFFF
SA90	1	0	1	1	0	1	0	2D0000-2D7FFF
SA91	1	0	1	1	0	1	1	2D8000-2DFFFF
SA92	1	0	1	1	1	0	0	2E0000-2E7FFF
SA93	1	0	1	1	1	0	1	2E8000-2EFFFF
SA94	1	0	1	1	1	1	0	2F0000-2F7FFF
SA95	1	0	1	1	1	1	1	2F8000-2FFFFF
SA96	1	1	0	0	0	0	0	300000-307FFF
SA97	1	1	0	0	0	0	1	308000-30FFFF
SA98	1	1	0	0	0	1	0	310000-317FFF
SA99	1	1	0	0	0	1	1	318000-31FFFF
SA100	1	1	0	0	1	0	0	320000-327FFF
SA101	1	1	0	0	1	0	1	328000-32FFFF
SA102	1	1	0	0	1	1	0	330000-337FFF
SA103	1	1	0	0	1	1	1	338000-33FFFF
SA104	1	1	0	1	0	0	0	340000-347FFF
SA105	1	1	0	1	0	0	1	348000-34FFFF
SA106	1	1	0	1	0	1	0	350000-357FFF
SA107	1	1	0	1	0	1	1	358000-35FFFF
SA108	1	1	0	1	1	0	0	360000-367FFF
SA109	1	1	0	1	1	0	1	368000-36FFFF
SA110	1	1	0	1	1	1	0	370000-377FFF
SA111	1	1	0	1	1	1	1	378000-37FFFF
SA112	1	1	1	0	0	0	0	380000-387FFF
SA113	1	1	1	0	0	0	1	388000-38FFFF
SA114	1	1	1	0	0	1	0	390000-397FFF
SA115	1	1	1	0	0	1	1	398000-39FFFF
SA116	1	1	1	0	1	0	0	3A0000-3A7FFF
SA117	1	1	1	0	1	0	1	3A8000-3AFFFF

Sector	A21	A20	A19	A18	A17	A16	A15	16-bit Address Range (in hexadecimal)
SA118	1	1	1	0	1	1	0	3B0000-3B7FFF
SA119	1	1	1	0	1	1	1	3B8000-3BFFFF
SA120	1	1	1	1	0	0	0	3C0000-3C7FFF
SA121	1	1	1	1	0	0	1	3C8000-3CFFFF
SA122	1	1	1	1	0	1	0	3D0000-3D7FFF
SA123	1	1	1	1	0	1	1	3D8000-3DFFFF
SA124	1	1	1	1	1	0	0	3E0000-3E7FFF
SA125	1	1	1	1	1	0	1	3E8000-3EFFFF
SA126	1	1	1	1	1	1	0	3F0000-3F7FFF
SA127	1	1	1	1	1	1	1	3F8000-3FFFFF

Table 2. BUS OPERATION--1

Mode Select	RE-SET#	CE#	WE#	OE#	Address	Data (I/O) Q0~Q15	ACC	WP#
Device Reset	L	X	X	X	X	HighZ	X	X
Standby Mode	Vcc± 0.3V	Vcc± 0.3V	X	X	X	HighZ	H	X
Output Disable	H	L	H	H	X	HighZ	X	X
Read Mode	H	L	H	L	AIN	DOUT	X	X
Write (Note1)	H	L	L	H	AIN	DIN	X	Note3
Accelerate Program	H	L	L	H	AIN	DIN	Vhv	Note3
Temporary Sector-Group Unprotect	Vhv	X	X	X	AIN	DIN	X	H
Sector-Group Protect (Note2)	Vhv	L	L	H	Sector Address, A6=L, A1=H, A0=L	DIN, DOUT	X	H
Chip Unprotect (Note2)	Vhv	L	L	H	Sector Address, A6=H, A1=H, A0=L	DIN, DOUT	X	H

Notes:
1. All sectors will be unprotected if WP#/ACC=Vhv.
2. The first sector is protected if WP#/ACC=Vil.
3. When WP#/ACC = Vih, the protection conditions of the first sector depend on previous protection conditions."Sector/ Sector Block Protection and Unprotection" describes the protect and unprotect method.
4. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
5. In Word Mode, the addresses are AM to A0.
6. AM: MSB of address.

BUS OPERATION--2

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	Q0~Q15
	CE#	WE#	OE#									
Sector Lock Status Verification	L	H	L	SA	x	V_{hv}	x	L	x	H	L	01h or 00h (Note1)
Read Silicon ID Manufacturer Code	L	H	L	x	x	V_{hv}	x	L	x	L	L	C2H
Read Silicon ID Device Code	L	H	L	x	x	V_{hv}	x	L	x	L	H	22D7H
Read Indicator Bit (Q7) For Security Sector	L	H	L	x	x	V_{hv}	x	L	x	H	H	(Note2)

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: WP# protects highest address sector: XX98H
   WP# protects lowest address sector: XX88H
   Factory unlocked code: WP# protects highest address sector: XX18H
   WP# protects lowest address sector: XX08H
3. AM: MSB of address.

WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CE# and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in the array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped temporarily after a period of time no more than Tready and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased.

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.

2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

ACCELERATED PROGRAM OPERATION

he device offers accelerated program operations through
the ACC function. This is one of two functions provided by the ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts VHH on this pin, the device automatically enters the aforementioned accelerated program mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. Removing VHH from the ACC pin must not be at VHH for operations other than accelerated programming, or device damage may result.

RESET# OPERATION

Driving RESET# pin low for a period more than Trp will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of Tready for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at GND±0.3V, the device consumes standby current(Isb).However, device draws larger current if RESET# pin is held at Vil but not within GND±0.3V.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read boot code from flash memory.

SECTOR GROUP PROTECT OPERATION

When a sector group is protected, program or erase operation will be disabled on these sectors. MX29LV640BU provides two methods for sector group protection.

Once the sector group is protected, the sector group remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at Vhv. Refer to temporary sector group unprotect operation for further details.

The first method is by applying Vhv on RESET# pin. Refer to Figure 13 for timing diagram and Figure 14 for the algorithm for this method.

The other method is asserting Vhv on A9 and OE# pins, with A6 and CE# at Vil. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

CHIP UNPROTECT OPERATION

MX29LV640BU provides two methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sectors groups are unprotected when shipped from the factory.

The first method is by applying Vhv on RESET# pin. Refer to Figure 13 for timing diagram and Figure 14 for algorithm of the operation.

The other method is asserting Vhv on A9 and OE# pins, with A6 at Vih and CE# at Vil (see Table 2). The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

TEMPORARY SECTOR GROUP UNPROTECT OPERATION

System can apply RESET# pin at Vhv to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The devices returns to normal operation once Vhv is removed from RESET# pin and previously protected sectors are again protected.

WRITE PROTECT (WP#)

This Write Protect function provides a hardware protection method on the first sector without using VID.

If the system asserts VIL on the WP# pin, the device disable program and erase function in the first sector independently of whether those sectors were protected or unprotect using the method described in "Sector Group Protection and Unprotect".

If the system asserts VIH on the WP# pin, the device reverts to whether the first sector was previously set to be protected or unprotected using the method described in "Sector Group Protection and Unprotect".

AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2H. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE#, A6 and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

VERIFY SECTOR GROUP PROTECT STATUS OPERATION

MX29LV640BU provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires V_{hv} on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A12 to A21 pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is not protected.

SECURITY SECTOR FLASH MEMORY REGION

The Security Sector region is an extra memory space of 128 words in length. The security sectors can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Factory Protect Verify and/or Security Sector Protect Verify to query the lock status of the device.

In factory-locked device, security sector region is protected when shipped from factory and the security silicon sector indicator bit is set to "1". In customer lockable device, security sector region is unprotected when shipped from factory and the security silicon indicator bit is set to "0".

Factory Locked: Security Sector Programmed and Protected at the Factory

In a factory locked device, the security silicon region is permanently locked after shipping from factory. The device will have a 8-word ESN in the security region. In uniform device : 000000h - 000007h (for MX29LV640BU).

Customer Lockable: Security Sector NOT Programmed or Protected at the Factory

When the security feature is not required, the security region can act as an extra memory space. The security silicon sector can be read, programmed, or erased just as normal sectors with the same endurance limitations.

Security silicon sector can also be protected by two methods. Note that once the security silicon sector is protected, there is no way to unprotect the security silicon sector and the content of it can no longer be altered.

The first method is to write a three-cycle command of Enter Security Region, and then follow the sector group protect algorithm as illustrated in Figure 14, except that RESET# pin may at either Vih or Vhv.

The other method is to write a three-cycle command of Enter Security Region, and then follow the alternate method of sector protect with A9, OE# at Vhv.

After the security silicon is locked and verified, system must write Exit Security Sector Region or go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously altered. The device automatically resets itself when Vcc is lower than VLKO and write cycles are ignored until Vcc is greater than VLKO. System must provide proper signals on control pins after Vcc is larger than VLKO to avoid unintentional program or erase operation

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, MX29LV640BU is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

TABLE 3. MX29LV640BU COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select				Enter Security Sector Region	Exit Security Sector
				Silicon ID	Device ID	Sector Factory	Protect Verify		
1st Bus Cyc	Addr	Addr	XXX	555	555	555	555	555	555
	Data	Data	F0	AA	AA	AA	AA	AA	AA
2nd Bus Cyc	Addr			2AA	2AA	2AA	2AA	2AA	2AA
	Data			55	55	55	55	55	55
3rd Bus Cyc	Addr			555	555	555	555	555	555
	Data			90	90	90	90	88	90
4th Bus Cyc	Addr			X00	X01	X03	(Sector) X02		XXX
	Data			C2H	22D7H	(Note1)	00/01		0
5th Bus Cyc	Addr								
	Data								
6th Bus Cyc	Addr								
	Data								

Command		Program	Chip Erase	Sector Erase	CFI Read	Erase Suspend	Erase Resume
1st Bus Cyc	Addr	555	555	555	55	XX	XX
	Data	AA	AA	AA	98	B0	30
2nd Bus Cyc	Addr	2AA	2AA	2AA			
	Data	55	55	55			
3rd Bus Cyc	Addr	555	555	555			
	Data	A0	80	80			
4th Bus Cyc	Addr	Addr	555	555			
	Data	Data	AA	AA			
5th Bus Cyc	Addr		2AA	2AA			
	Data		55	55			
6th Bus Cyc	Addr		555	Sector			
	Data		10	30			

Notes:
1. Factory locked code: WP# protects highest address sector: XX98H
   WP# protects lowest address sector: XX88H
   Factory unlocked code: WP# protects highest address sector: XX18H
   WP# protects lowest address sector: XX08H

RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not secured silicon is locked and whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

	Address	Data (Hex)	Representation
Manufacturer ID	X00	C2	
Device ID	X01	22D7	Top/Bottom Boot Sector
Secured Silicon	X03	98/18, 88/08	Factory locked/unlocked
Sector Protect Verify	(Sector address) X 02	00/01	Unprotected/protected

There is an alternative method to that shown in Table 2, which is intended for EPROM programmers and requires Vhv on address bit A9.

AUTOMATIC PROGRAMMING

The MX29LV640BU can provide the user program function by the form of Word-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming. With the internal write state controller, the device requires the user to write the program command and data only.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

The typical chip program time at room temperature of the MX29LV640BU is less than 45 seconds.

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	RY/BY#*2
In progress*1	Q7#	Toggling	0	0
Finished	Q7	Stop toggling	0	1
Exceed time limit	Q7#	Toggling	1	0

*1: The status "in progress" means both program mode and erase-suspended program mode.
*2: RY/BY# is an open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us or less and the device returns to read array state without programing the data in the protected sector.
*4: The Q5 failure condition may appear if the system tries to program a to a "1" location that is previously programmed to "0". Only an erase operation can change a "0" back to a "1".

CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware reset or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#
In progress	0	Toggling	0	Toggling	0
Finished	1	1	1	1	1
Exceed time limit	0	Toggling	1	Toggling	0

SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector erase or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status		Q7	Q6	Q5	Q3	Q2	RY/BY#*2
Time-out period		0	Toggling	0	0	Toggling	0
In progress	read in erase sector	0	Toggling	0	1	Toggling	0
	read in non-erase sector	0	Toggling	0	1	Stop Toggling	0
Finished		1	1	1	1	1	1
Exceed time limit		0	Toggling	1	1	Toggling	0

*1: The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptible to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.
*2: RY/BY# is open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to erase a protected sector, Q7 will output its complement data or Q6 continues to toggle for 100us or less and the device returned to read array status without erasing the data in the protected sector.

SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1 (<=20us) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, Q7, and RY/BY#.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of Taa; while reading the sector in erase-suspend mode, device will output its status. User can use Q6 and Q2 to judge the sector is erasing or the erase is suspended.

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	Toggle	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 4mS interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV640BU features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, word configuration, operating voltages and timing information of this device by CFI mode. The device enters the CFI Query mode when the system writes the CFI Query command, 98H, to address 55H any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4. A reset command is required to exit CFI mode and go back to ready array mode or erase suspend mode. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address (h) (Word Mode)	Data (h)
Query-unique ASCII string "QRY"	10	0051
	11	0052
	12	0059
Primary vendor command set and control interface ID code	13	0002
	14	0000
Address for primary algorithm extended query table	15	0040
	16	0000
Alternate vendor command set and control interface ID code	17	0000
	18	0000
Address for alternate algorithm extended query table	19	0000
	1A	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address (h) (Word Mode)	Data (h)
Vcc supply minimum program/erase voltage	1B	0027
Vcc supply maximum program/erase voltage	1C	0036
VPP supply minimum program/erase voltage	1D	0000
VPP supply maximum program/erase voltage	1E	0000
Typical timeout per single word write, 2^n us	1F	0004
Typical timeout for maximum-size buffer write, 2^n us	20	0000
Typical timeout per individual block erase, 2^n ms	21	000A
Typical timeout for full chip erase, 2^n ms	22	0000
Maximum timeout for word write, 2^n times typical	23	0005
Maximum timeout for buffer write, 2^n times typical	24	0000
Maximum timeout per individual block erase, 2^n times typical	25	0004
Maximum timeout for chip erase, 2^n times typical	26	0000

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address (h) (Word Mode)	Data (h)
Device size = 2^n in number of bytes	27	0017
Flash device interface description (02=asynchronous x8/x16)	28	0002
	29	0000
Maximum number of bytes in buffer write = 2^n (not support)	2A	0000
	2B	0000
Number of erase regions within device	2C	0002
Index for Erase Bank Area 1	2D	0007
[2E,2D] = # of same-size sectors in region 1-1	2E	0000
[30, 2F] = sector size in multiples of 256-bytes	2F	0020
	30	0000
Index for Erase Bank Area 2	31	007E
	32	0000
	33	0000
	34	0001
Index for Erase Bank Area 3	35	0000
	36	0000
	37	0000
	38	0000
Index for Erase Bank Area 4	39	0000
	3A	0000
	3B	0000
	3C	0000

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Word Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40	0050
	41	0052
	42	0049
Major version number, ASCII	43	0031
Minor version number, ASCII	44	0031
Unlock recognizes address (0= recognize, 1= don't recognize)	45	0000
Erase suspend (2= to both read and program)	46	0002
Sector protect (N= # of sectors/group)	47	0004
Temporary sector unprotect (1=supported)	48	0001
Sector protect/Chip unprotect scheme	49	0004
Simultaneous R/W operation (0=not supported)	4A	0000
Burst mode (0=not supported)	4B	0000
Page mode (0=not supported)	4C	0000
Maximum acceleration supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4D	00B5
Minimum acceleration supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4E	00C5
Top/Bottom boot block indicator 02h=bottom boot device 03h=top boot device	4F	0002/ 0003

ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage Range
Vcc . . . . . -0.5 V to +4.0 V
A9, OE#, ACC and RESET# . . . . . -0.5 V to +12.5 V
The other pins. . . . . -0.5 V to Vcc +0.5 V
Output Short Circuit Current (less than one second) . . . . . 200 mA

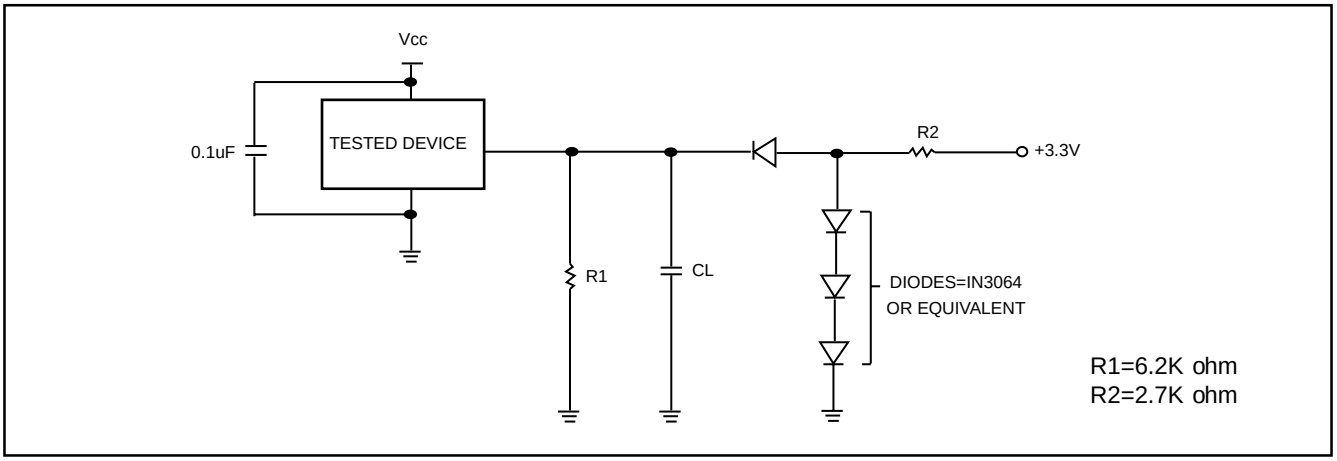
OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade
Surrounding Temperature (T_A). . . . . 0°C to +70°C
Industrial (I) Grade
Surrounding Temperature (T_A). . . . . -40°C to +85°C
V_{CC} Supply Voltages
V_{CC} range. . . . . +2.7 V to 3.6 V

DC CHARACTERISTICS

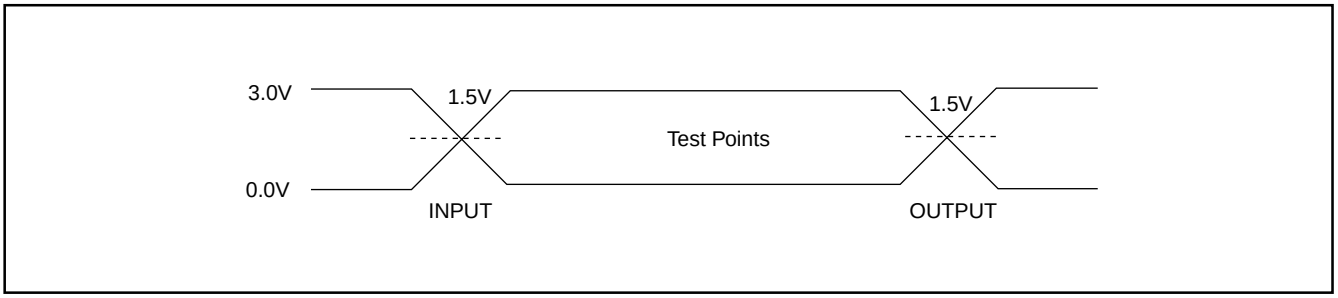
Symbol	Description	Min	Typ	Max	Remark
Iilk	Input Leak			±1.0uA	
Iilk9	A9 Leak			35uA	A9=12.5V
Iolk	Output Leak			±1.0uA	
Icr1	Read Current(5MHz)		9mA	16mA	CE#=Vil, OE#=Vih
Icr2	Read Current(1MHz)		2mA	4mA	CE#=Vil, OE#=Vih
Icw	Write Current		26mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		0.2uA	15uA	Vcc=Vcc max, other pin disable
Isbr	Reset Current		0.2uA	15uA	Vcc=Vccmax, Reset# enable, other pin disable
Isbs	Sleep Mode Current		0.2uA	15uA	
Icp1	Accelerated Pgm Current, ACC pin		5mA	10mA	CE#=Vil, OE#=Vih,
Icp2	Accelerated Pgm Current, Vcc pin		15mA	30mA	CE#=Vil, OE#=Vih,
Vil	Input Low Voltage	-0.5V		0.8V	
Vih	Input High Voltage	0.7xVcc		Vcc+0.3V	
Vhv	Very High Voltage for hardware Protect/Unprotect/Accelerated Program/Auto Select/Temporary Unprotect	11.5V		12.5V	
Vol	Output Low Voltage			0.45V	Iol=4.0mA
Voh1	Ouput High Voltage	0.85xVcc			Ioh1=-2mA
Voh2	Ouput High Voltage	Vcc-0.4V			Ioh2=-100uA
Vlko	Low VCC Lock-Out Voltage	1.5V			

SWITCHING TEST CIRCUITS



Test Condition
Output Load : 1 TTL gate
Output Load Capacitance,CL : 30pF
Rise/Fall Times : 5ns
In/Out reference levels :1.5V

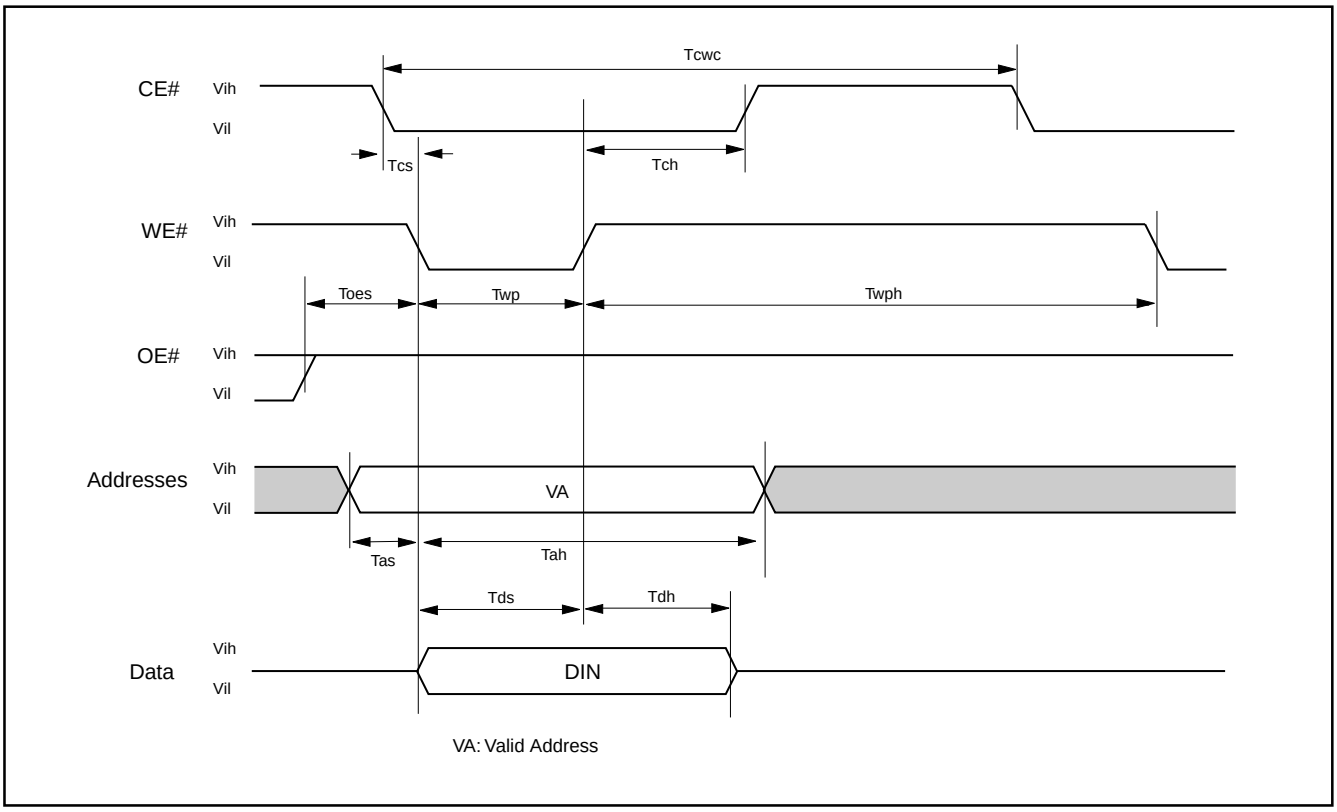
SWITCHING TEST WAVEFORMS



AC CHARACTERISTICS

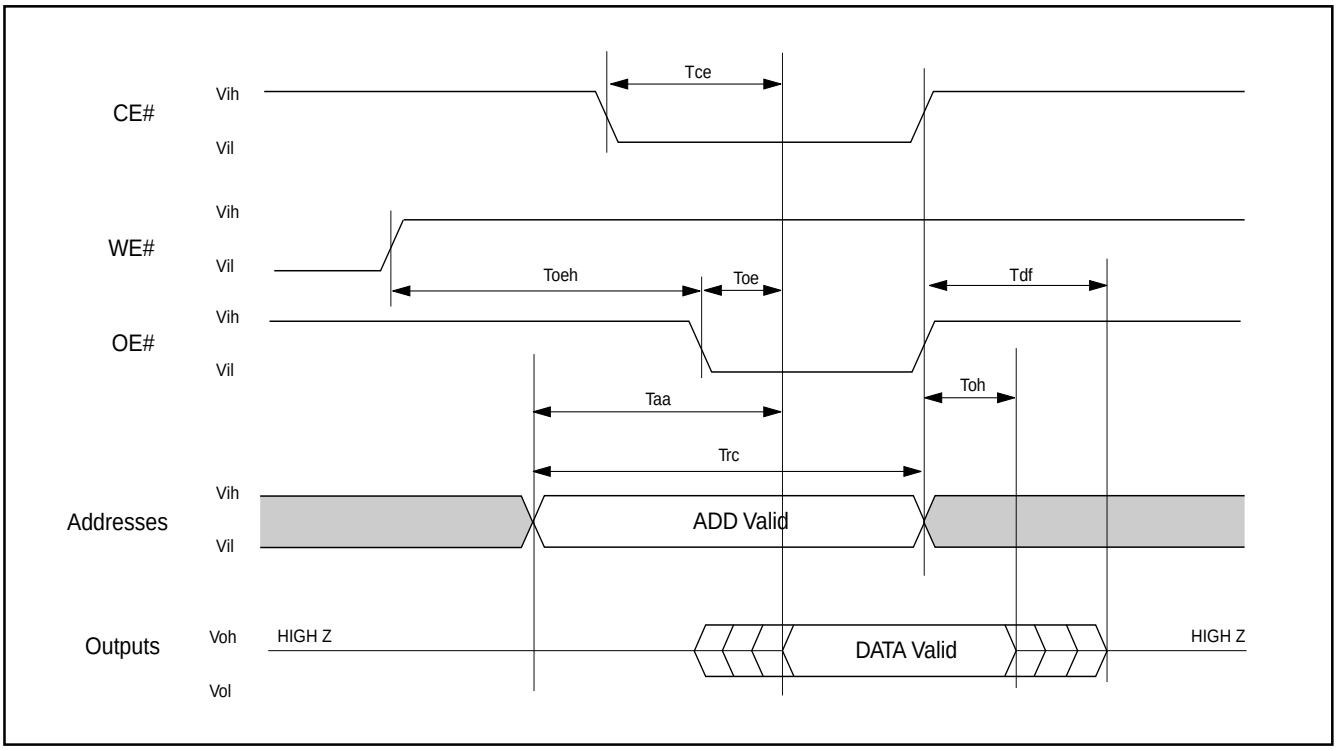
Symbol	Description		Min	Typ	Max	Unit
Taa	Valid data output after address				90/120	ns
Tce	Valid data output after CE# low				90/120	ns
Toe	Valid data output after OE# low				35/50	ns
Tdf	Data output floating after OE# high				30/30	ns
Toh	Output hold time from the earliest rising edge of address, CE#, OE#		0			ns
Trc	Read period time		90/120			ns
Twc	Write period time		90/120			ns
Tcwc	Command write period time		90/120			ns
Tas	Address setup time		0			ns
Tah	Address hold time		45/50			ns
Tds	Data setup time		45/50			ns
Tdh	Data hold time		0			ns
Tvcs	Vcc setup time		50			us
Tcs	Chip enable Setup time		0			ns
Tch	Chip enable hold time		0			ns
Toes	Output enable setup time		0			ns
Toeh	Output enable hold time	Read	0			ns
Toeh		Toggle & Data# Polling	10			ns
Tws	WE# setup time		0			ns
Twh	WE# hold time		0			ns
Tcep	CE# pulse width		45/50			ns
Tceph	CE# pulse width high		30			ns
Twp	WE# pulse width		35/50			ns
Twph	WE# pulse width high		30			ns
Tbusy	Program/Erase active time by RY/BY#				90	ns
Tghwl	Read recover time before write		0			ns
Tghel	Read recover time before write		0			ns
Twhwh1	Program operation			11		us
Twhwh1	Acc Program operation			7		us
Twhwh2	Sector Erase Operation			1.6		sec
Tbal	Sector Add hold time				50	us

Figure 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

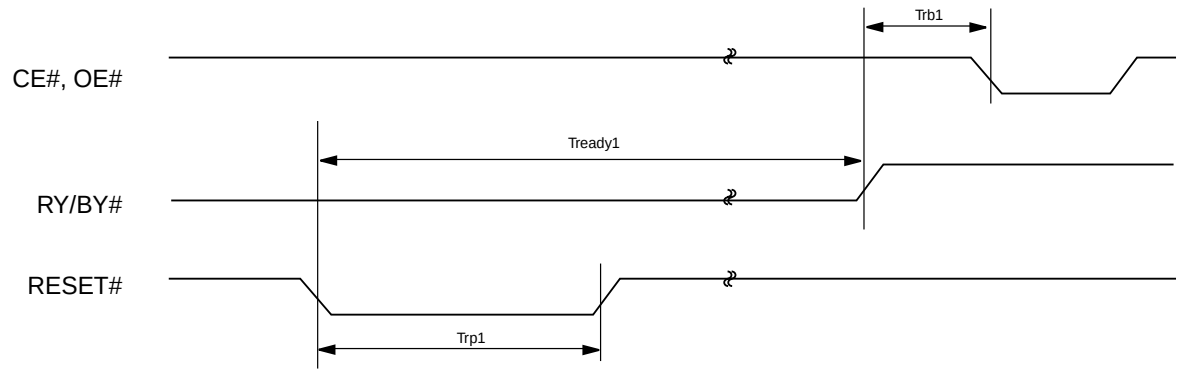
Figure 2. READ TIMING WAVEFORMS



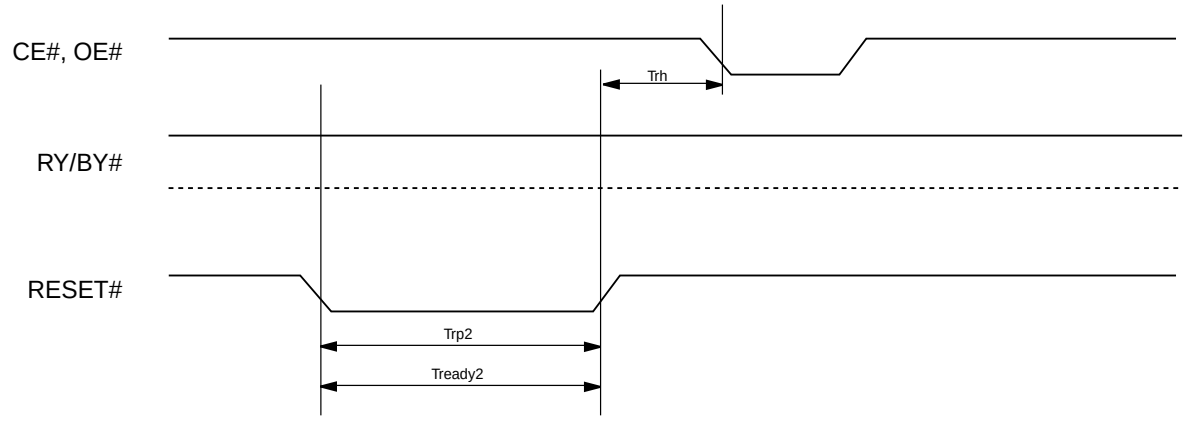
AC CHARACTERISTICS

Item	Description	Setup	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	10	us
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
Trh	RESET# High Time Before Read	MIN	50	ns
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	ns
Tready1	RESET# PIN Low (During Automatic Algorithms) to Read or Write	MAX	20	us
Tready2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write	MAX	500	ns

Figure 3. RESET# TIMING WAVEFORM



Reset Timing during Automatic Algorithms



Reset Timing NOT during Automatic Algorithms

ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

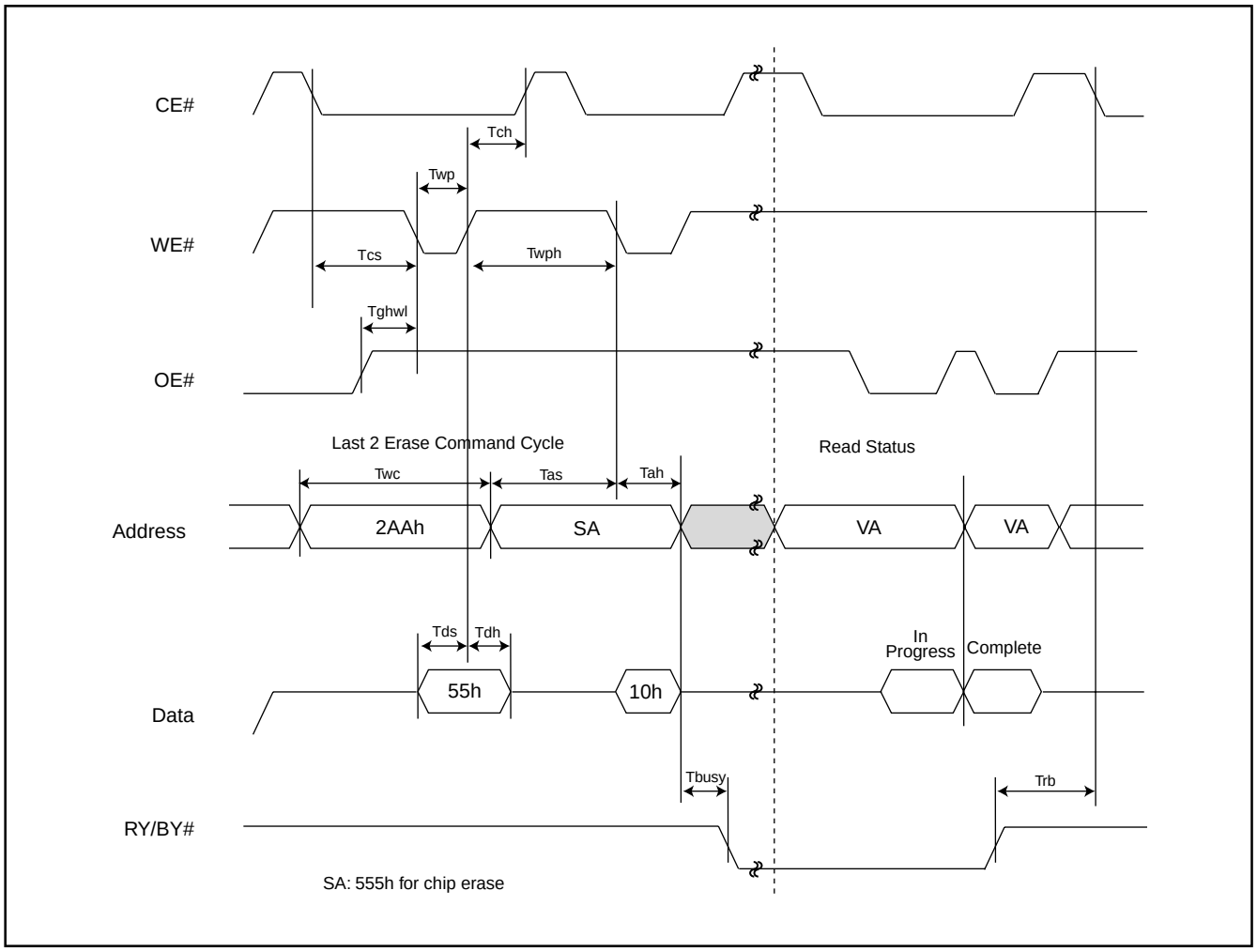


Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

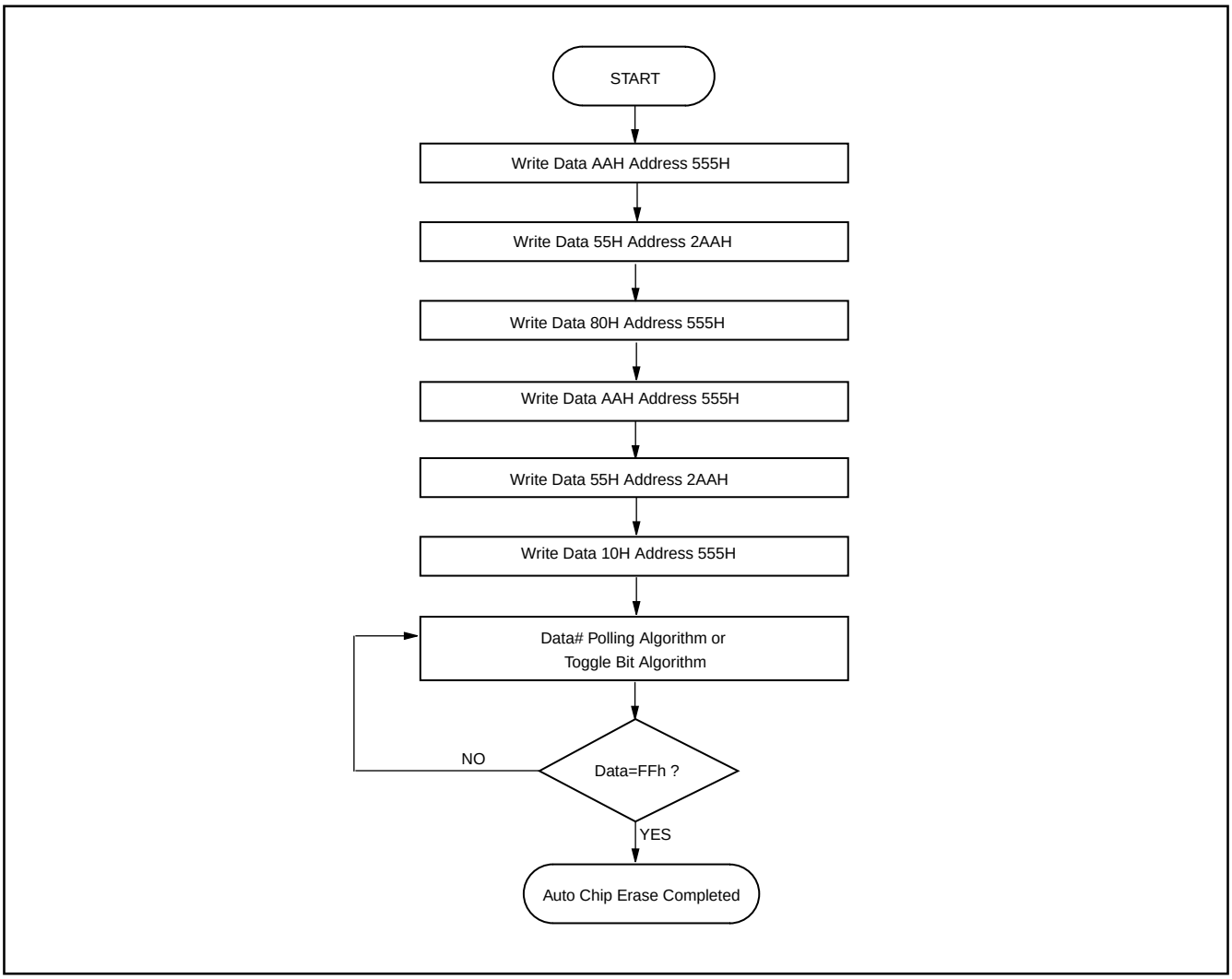


Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

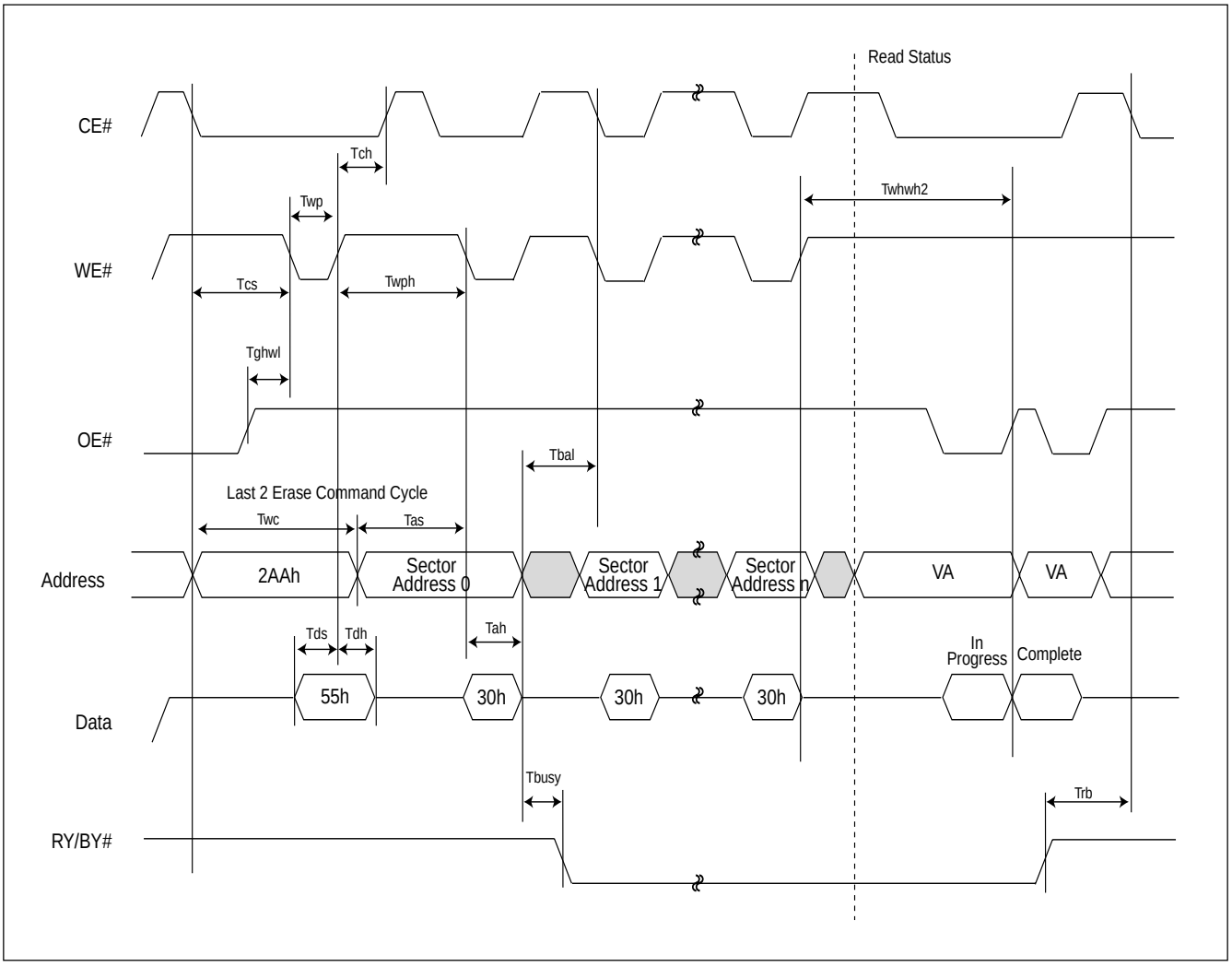


Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

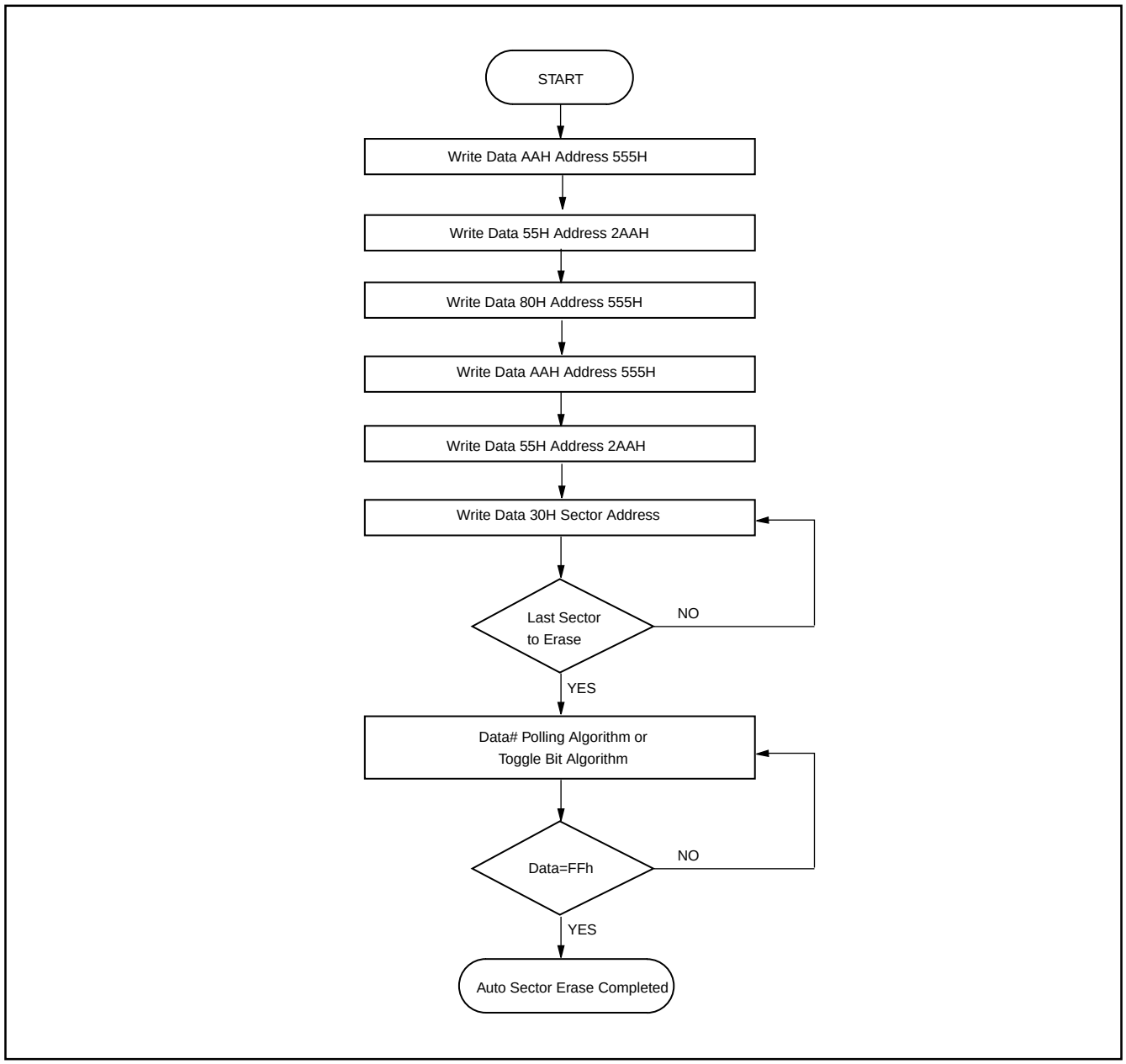


Figure 8. ERASE SUSPEND/RESUME FLOWCHART

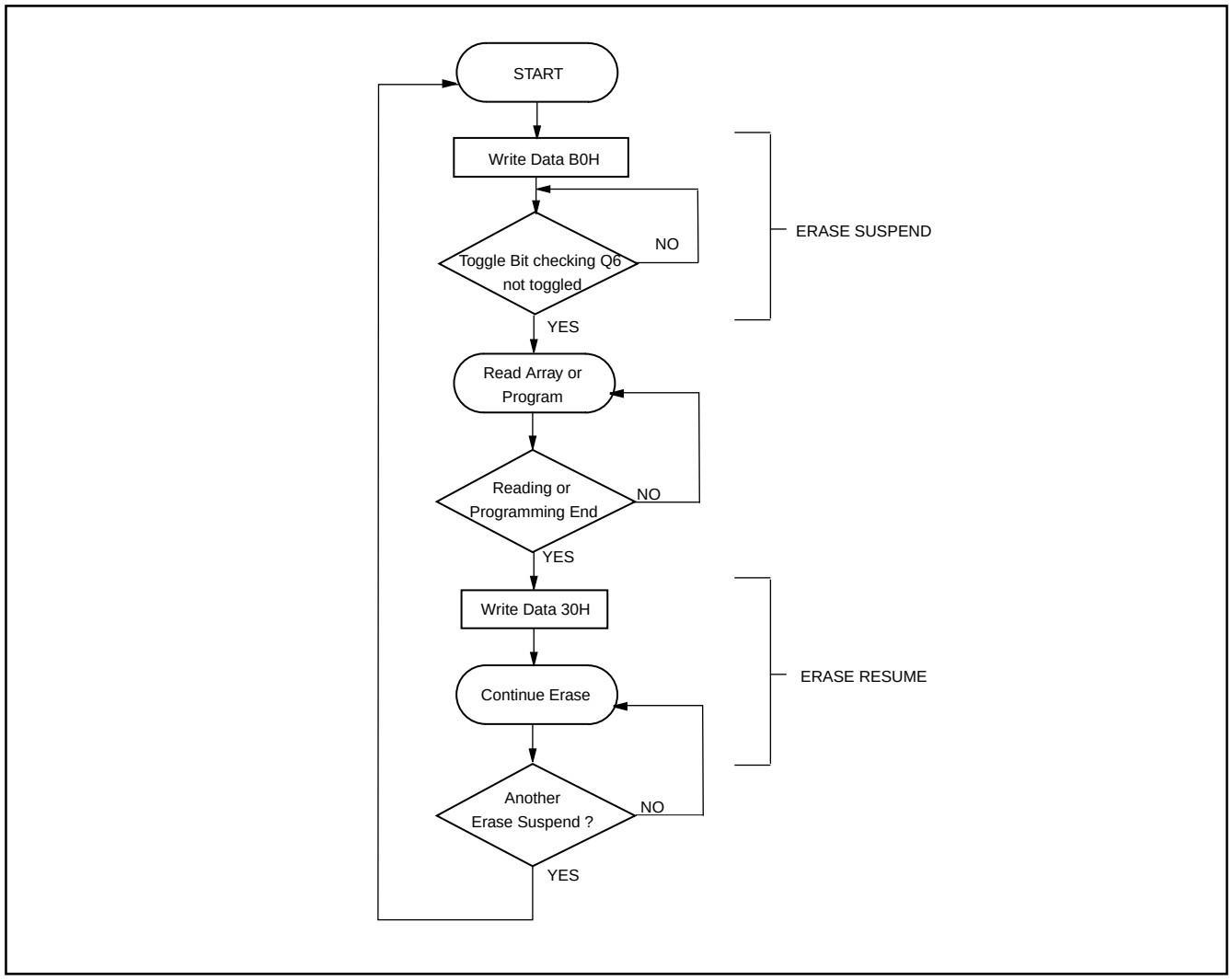


Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS

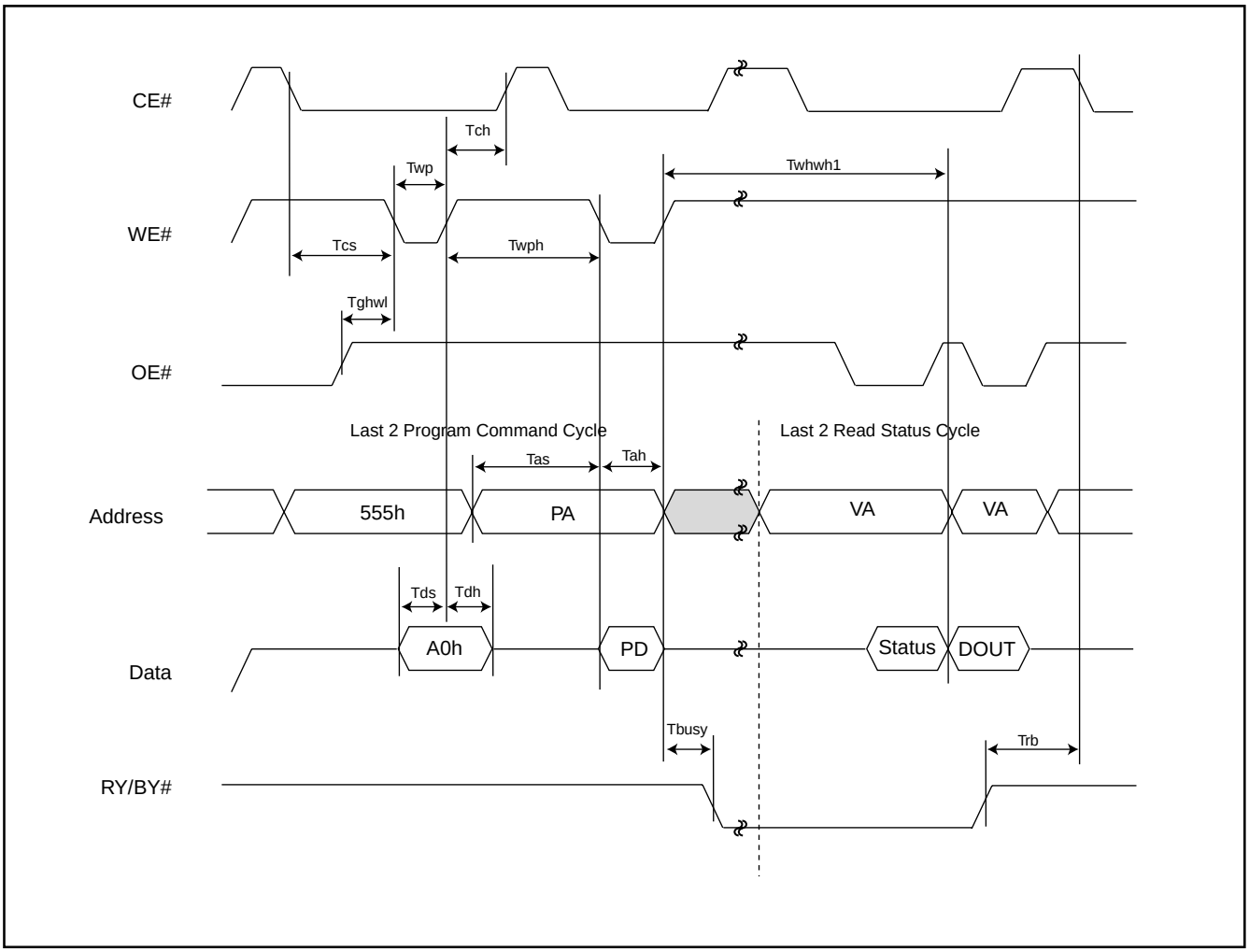


Figure 10. Accelerated Program Timing Diagram

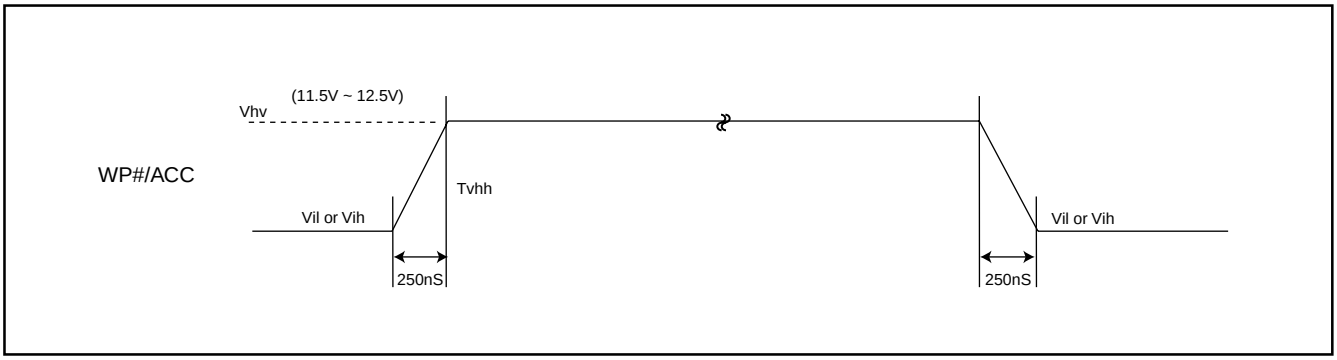


Figure 11. CE# CONTROLLED WRITE TIMING WAVEFORM

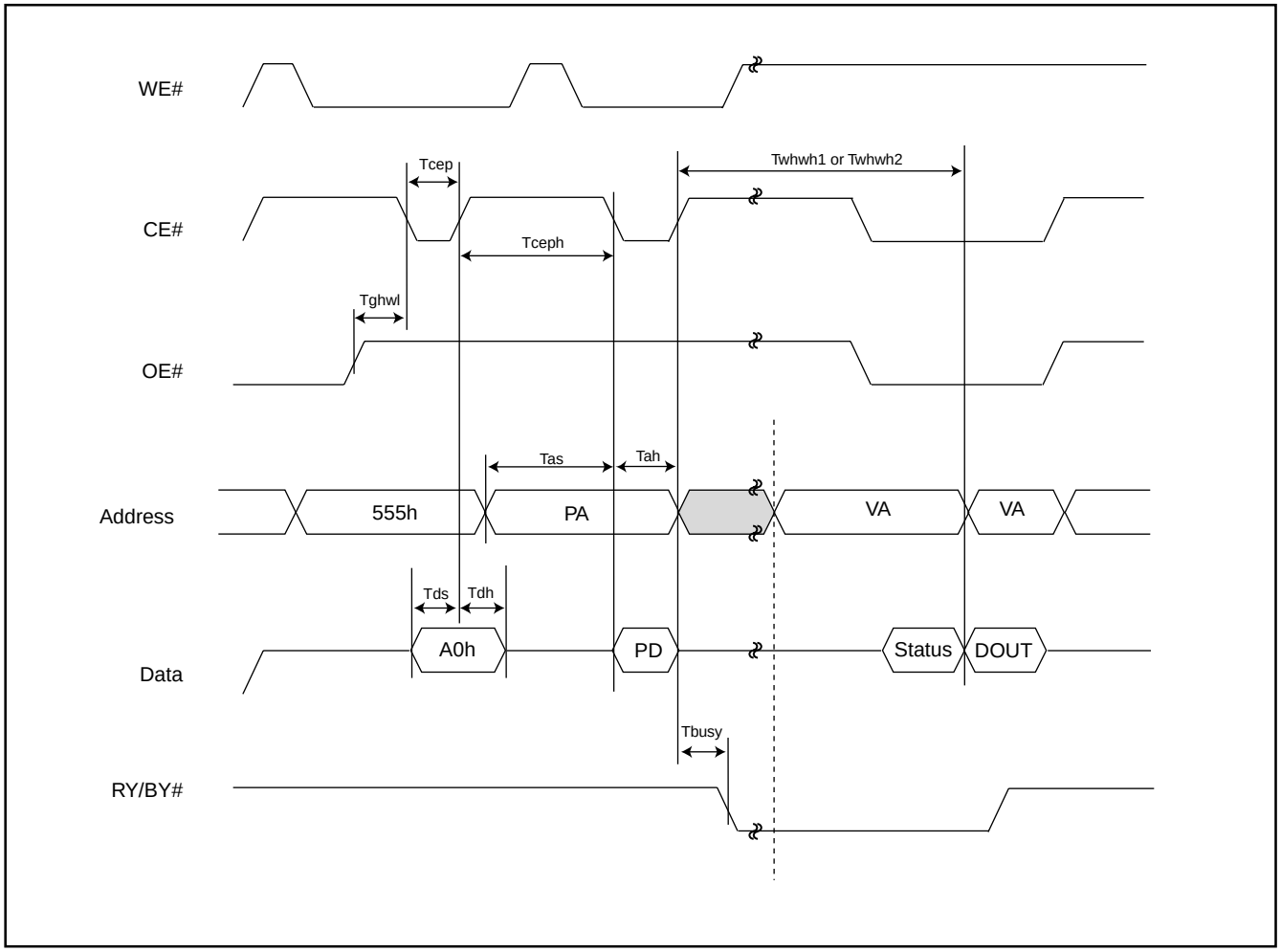
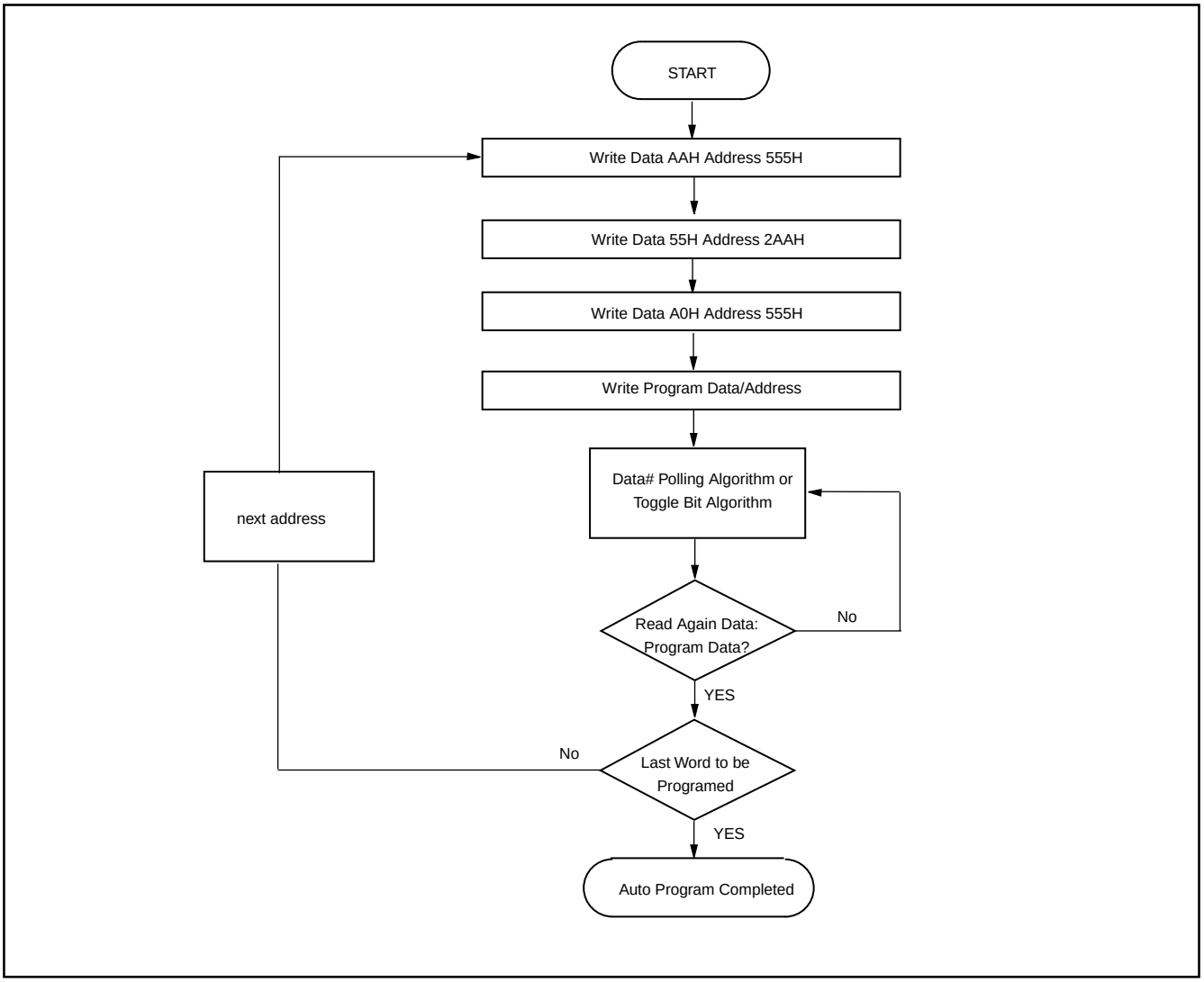


Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



SECTOR GROUP PROTECT/CHIP UNPROTECT

Figure 13. SECTOR GROUP PROTECT/CHIP UNPROTECT WAVEFORM (RESET# Control)

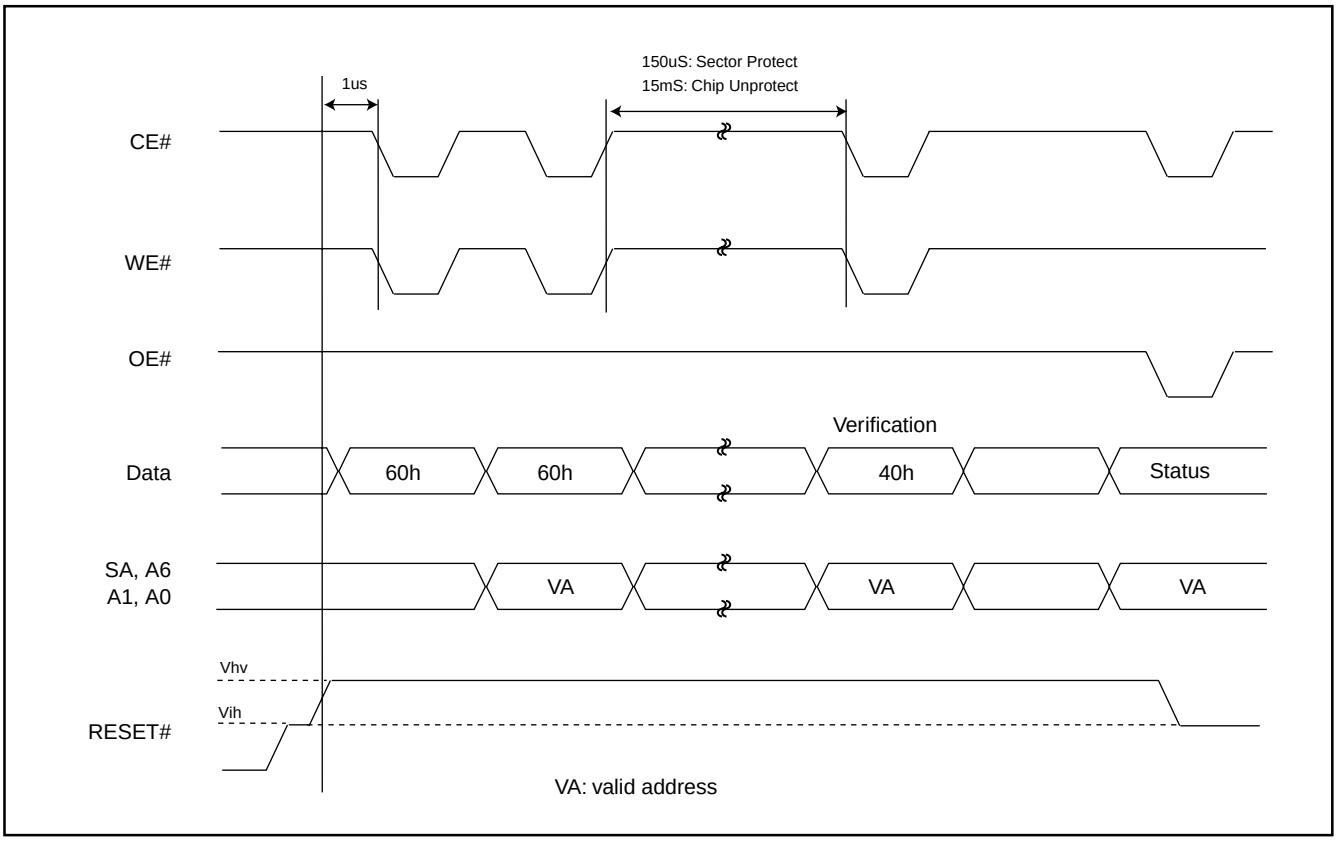


Figure 14-1. IN-SYSTEM SECTOR GROUP PROTECT WITH RESET#=Vhv

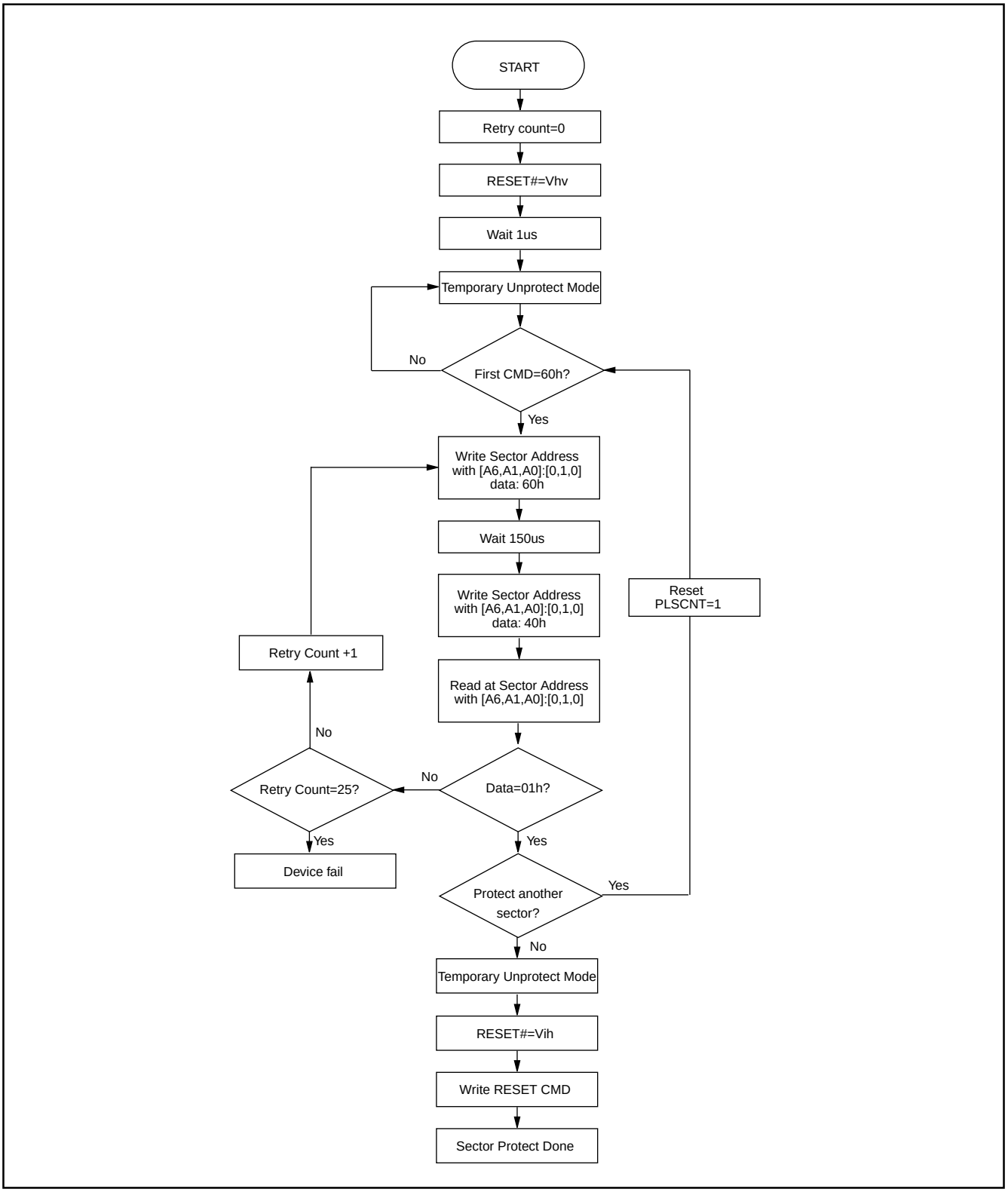


Figure 14-2. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv

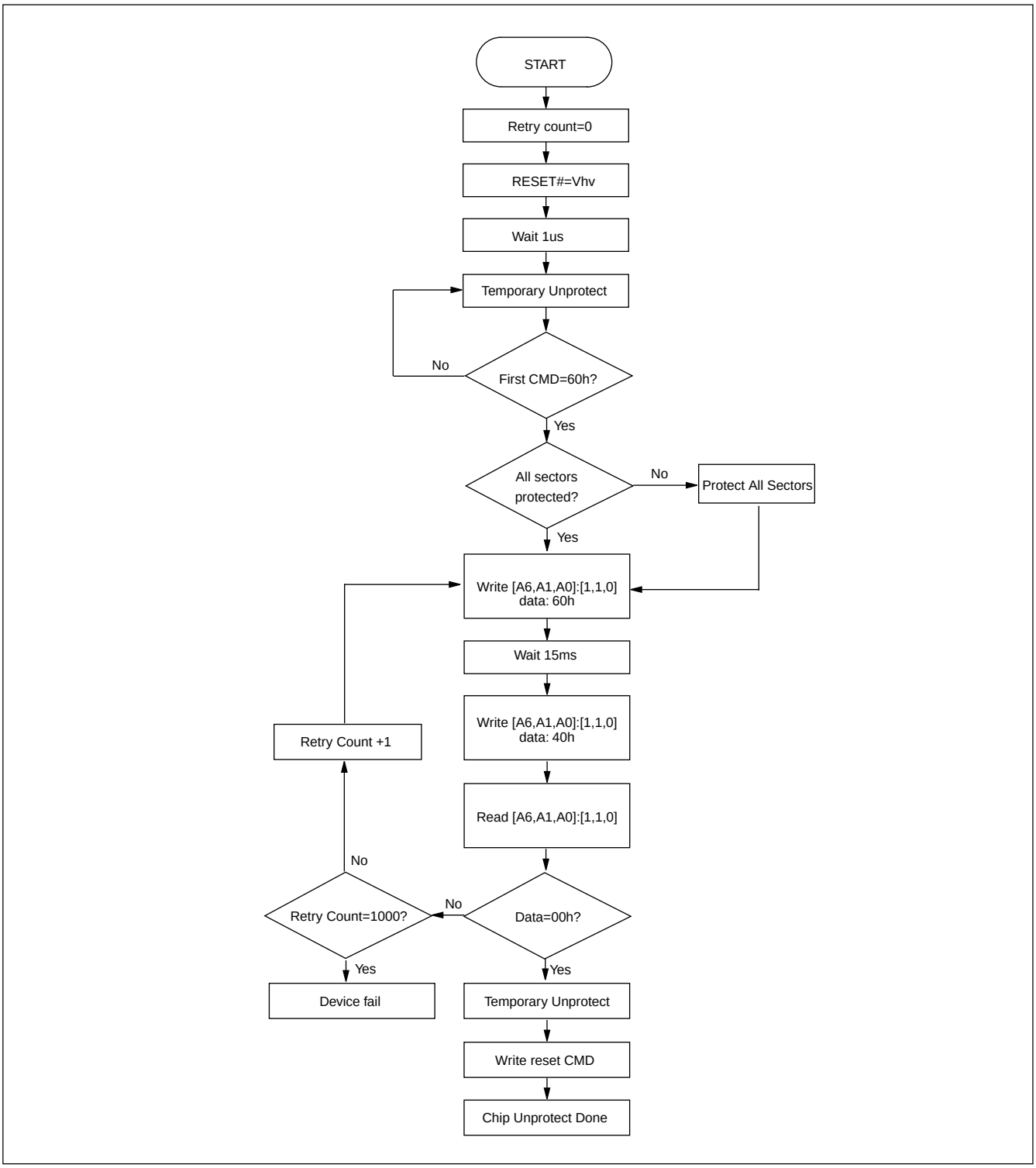


Table 5. TEMPORARY SECTOR GROUP UNPROTECT

Parameter	Alt	Description	Condition	Speed	Unit
Trpvhh	Tvidr	RESET# Rise Time to Vhv and Vhv Fall Time to RESET#	MIN	500	ns
Tvhhwl	Trsp	RESET# Vhv to WE# Low	MIN	4	us

Figure 15. TEMPORARY SECTOR GROUP UNPROTECT WAVEFORMS

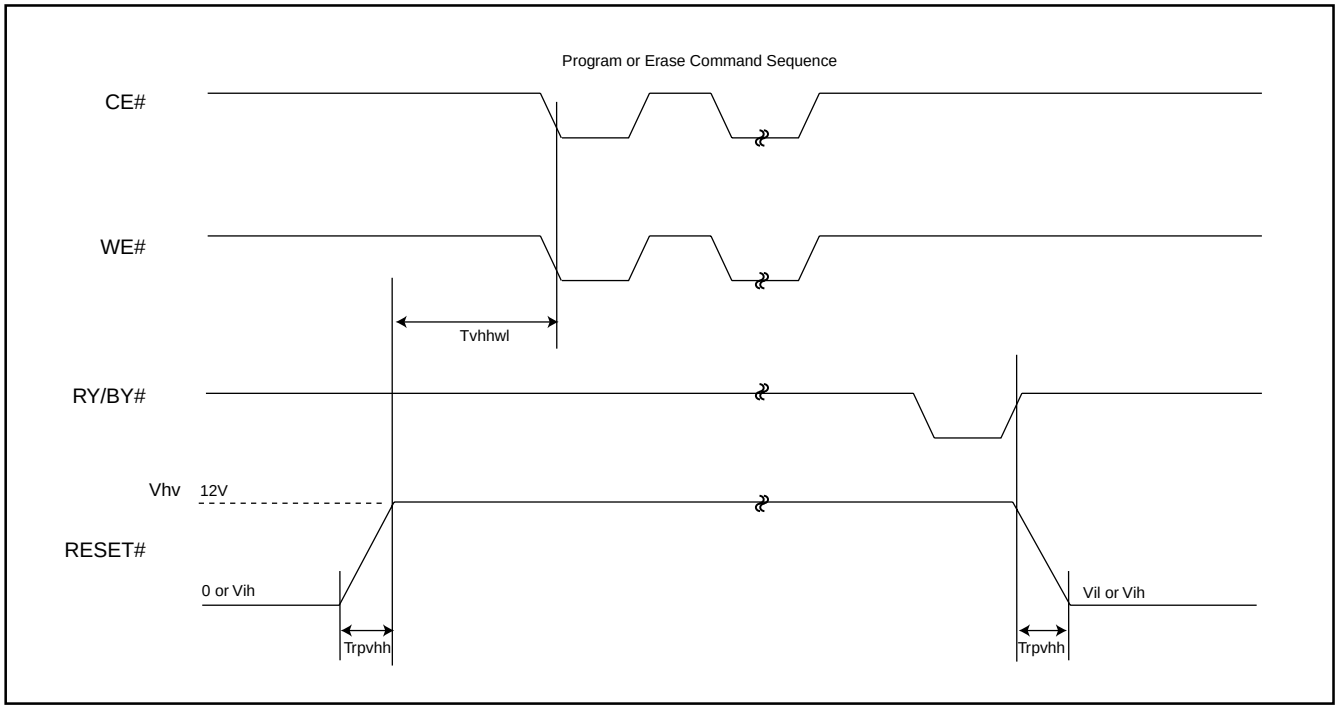
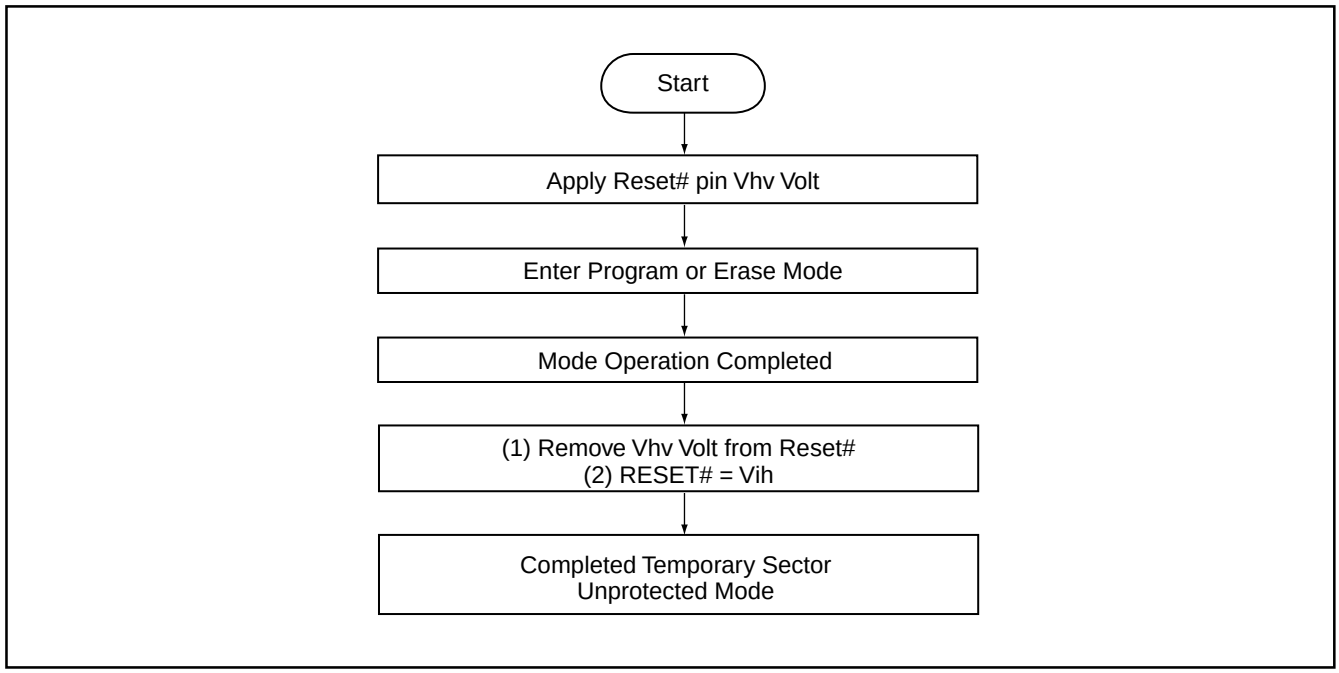
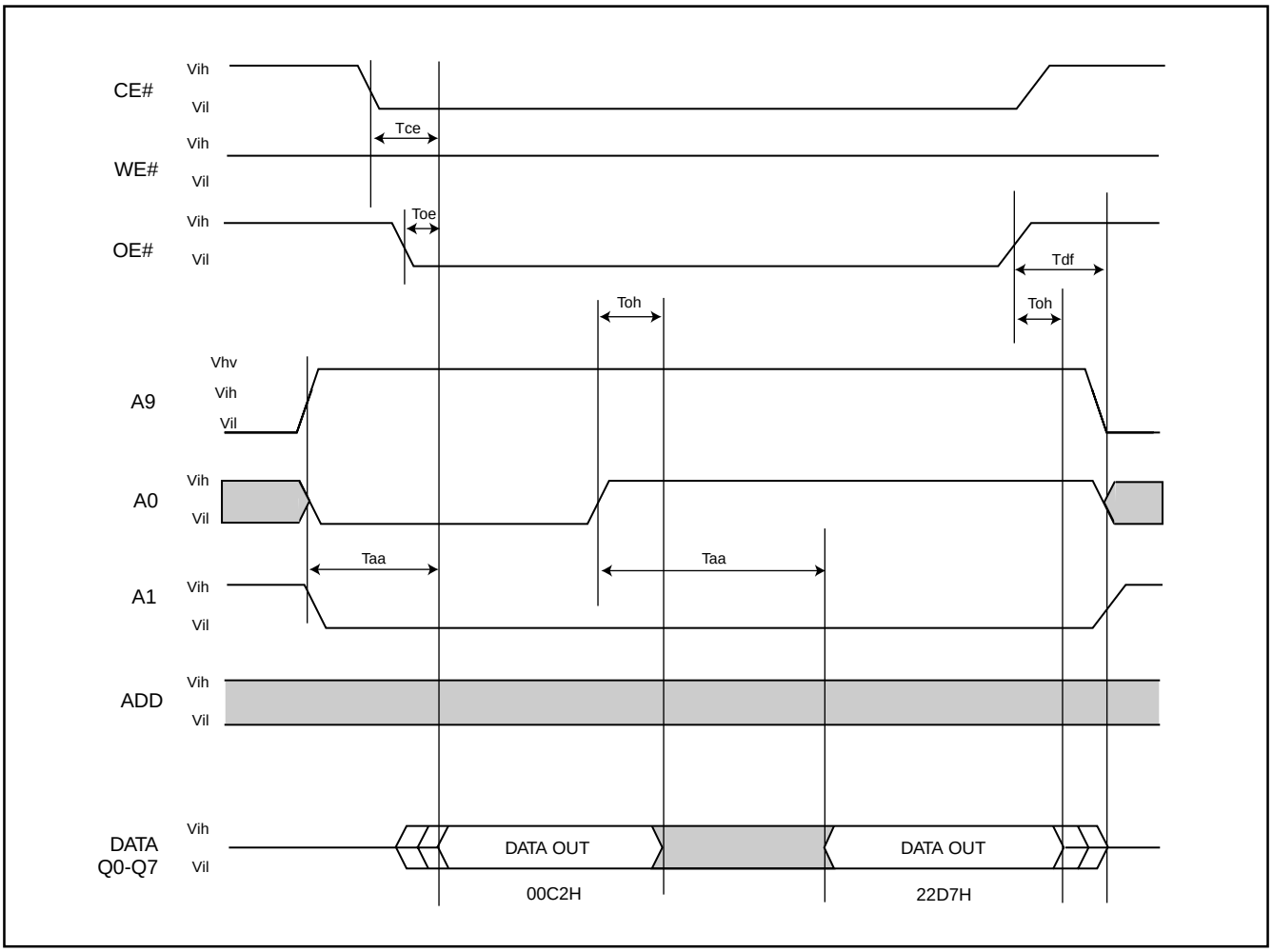


Figure 16. TEMPORARY SECTOR GROUP UNPROTECT FLOWCHART



Notes:
1. Temporary unprotect all protected sectors Vhv=11.5~12.5V.
2. After leaving temporary unprotect mode, the previously protected sectors are again protected.

Figure 17. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

Figure 18. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

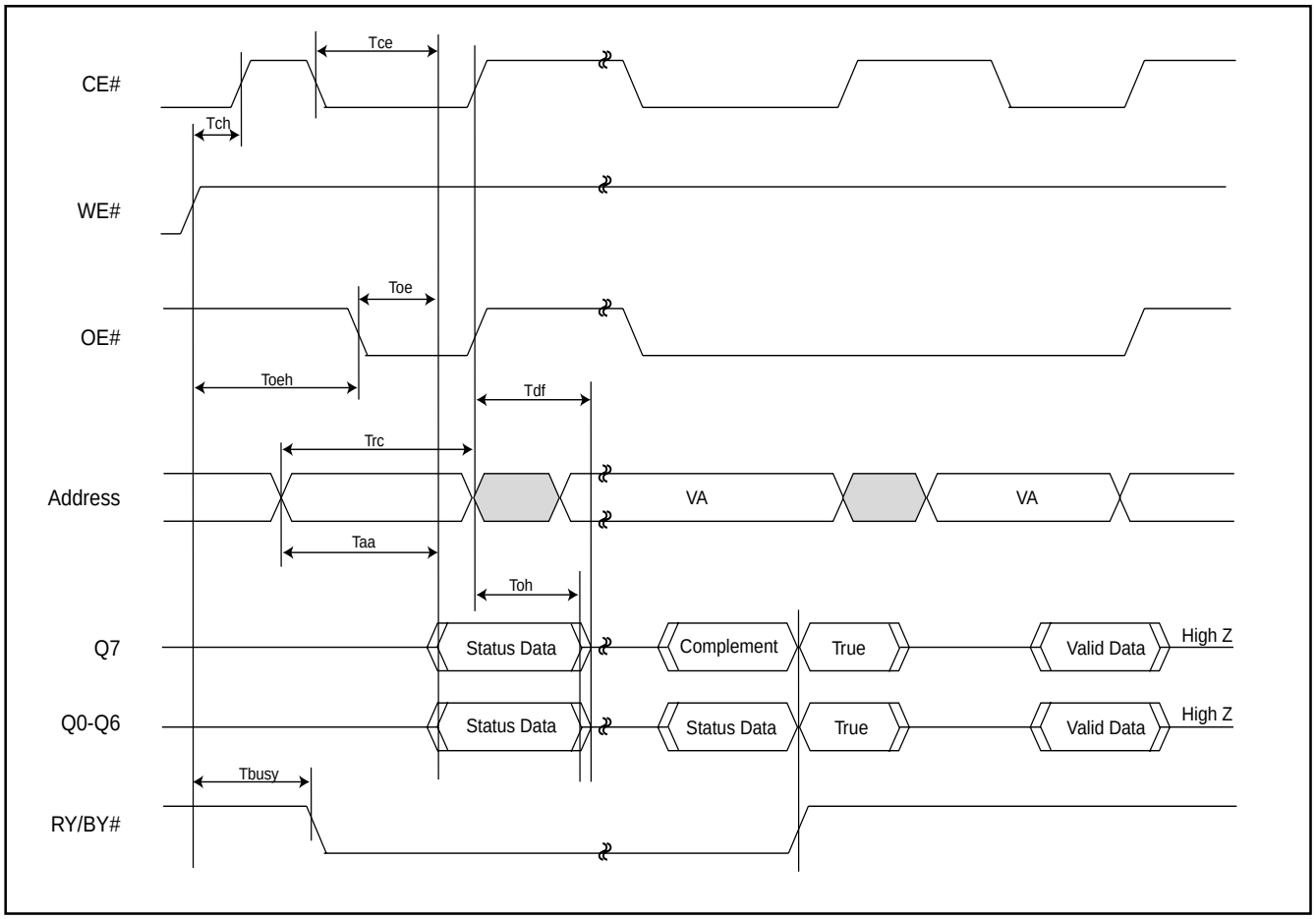
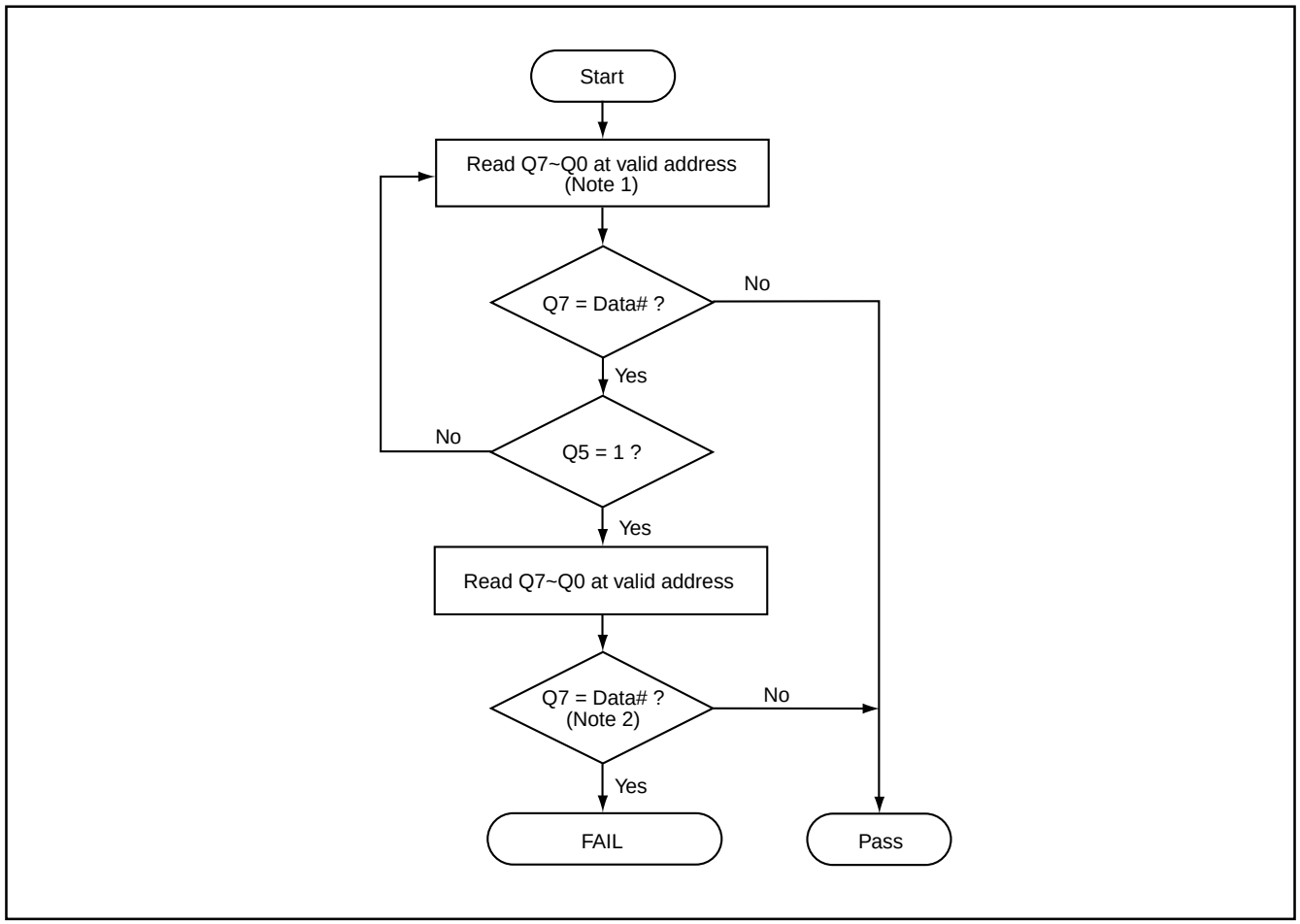


Figure 19. DATA# POLLING ALGORITHM



Notes:
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 20. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

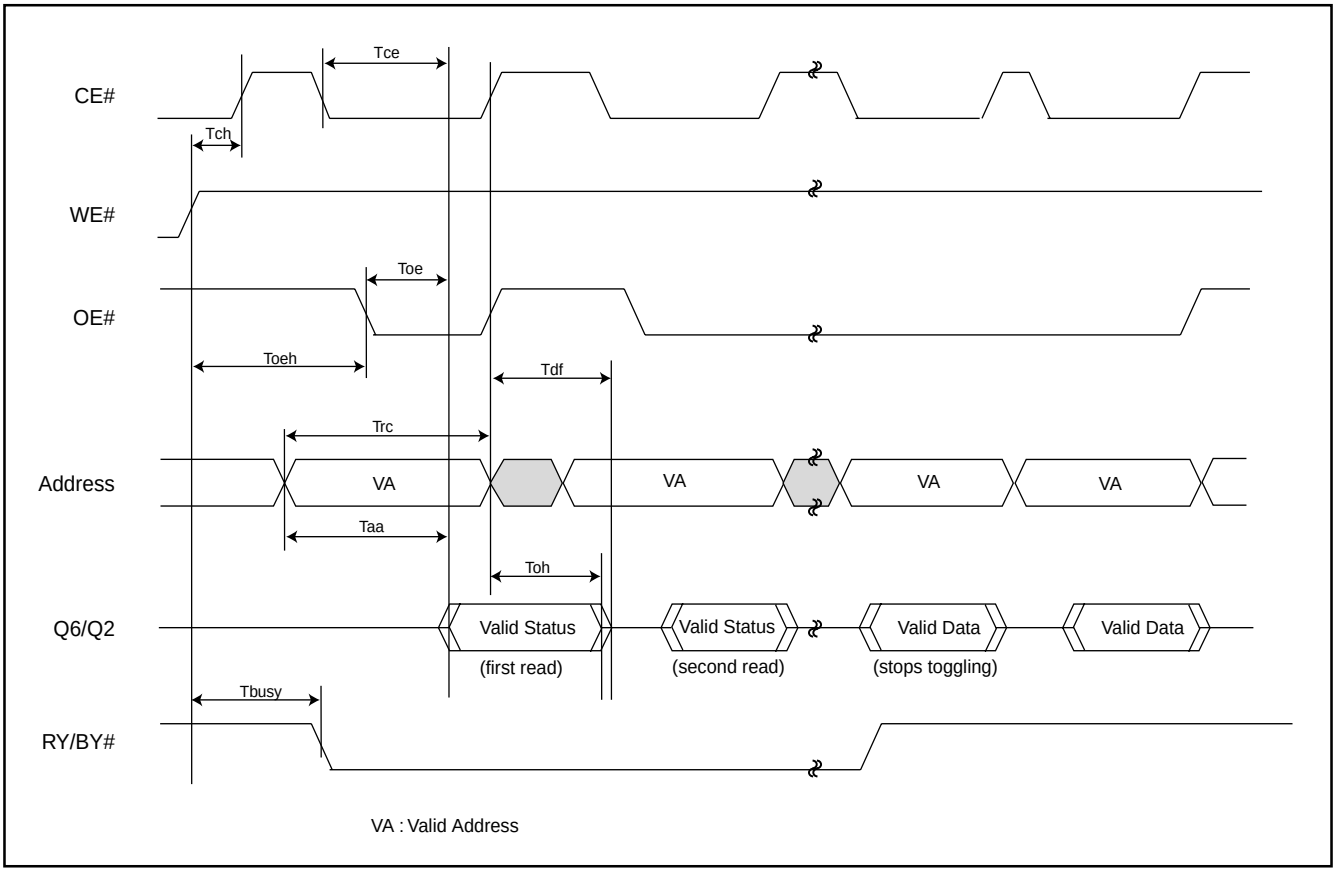
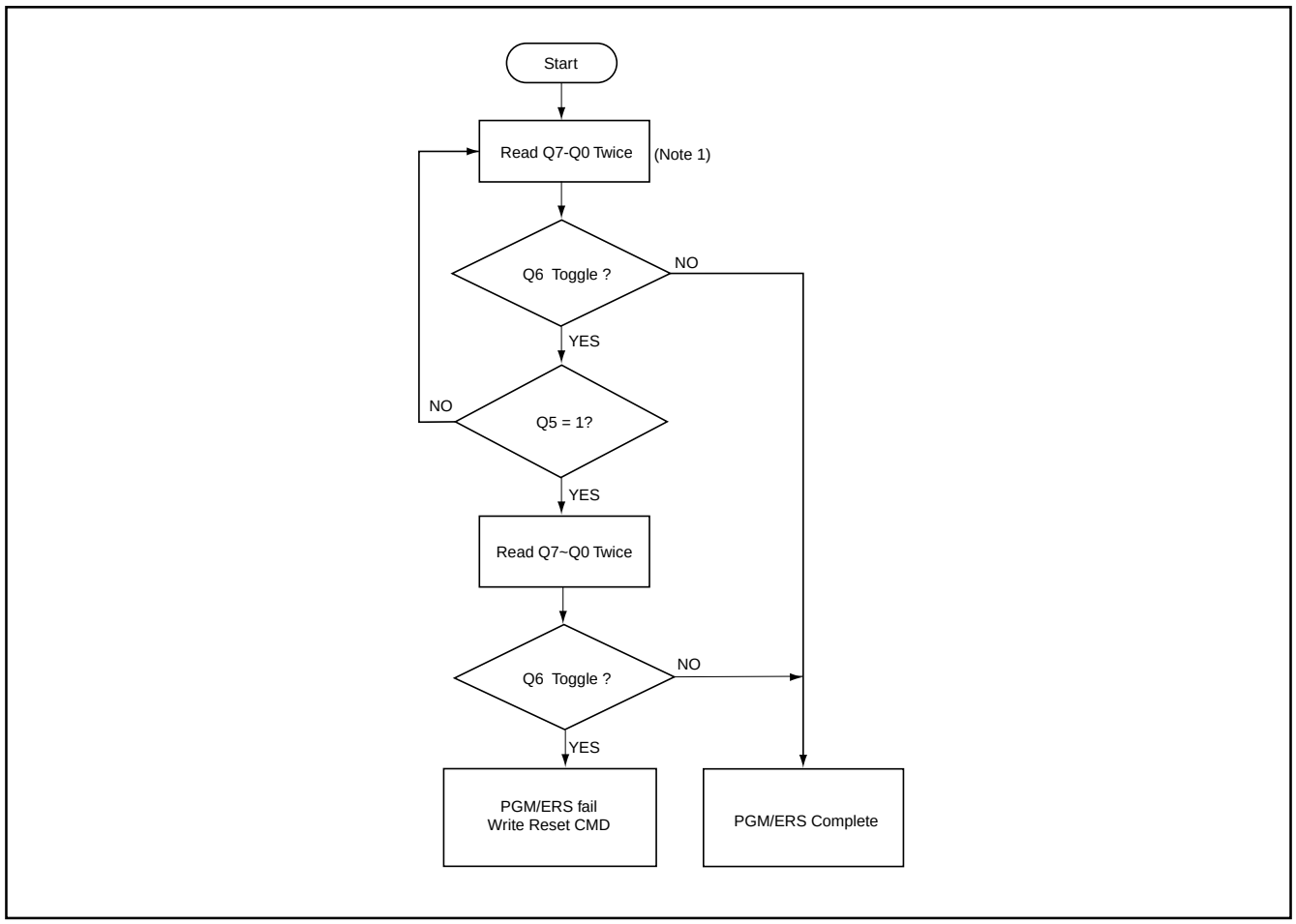


Figure 21. TOGGLE BIT ALGORITHM



Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

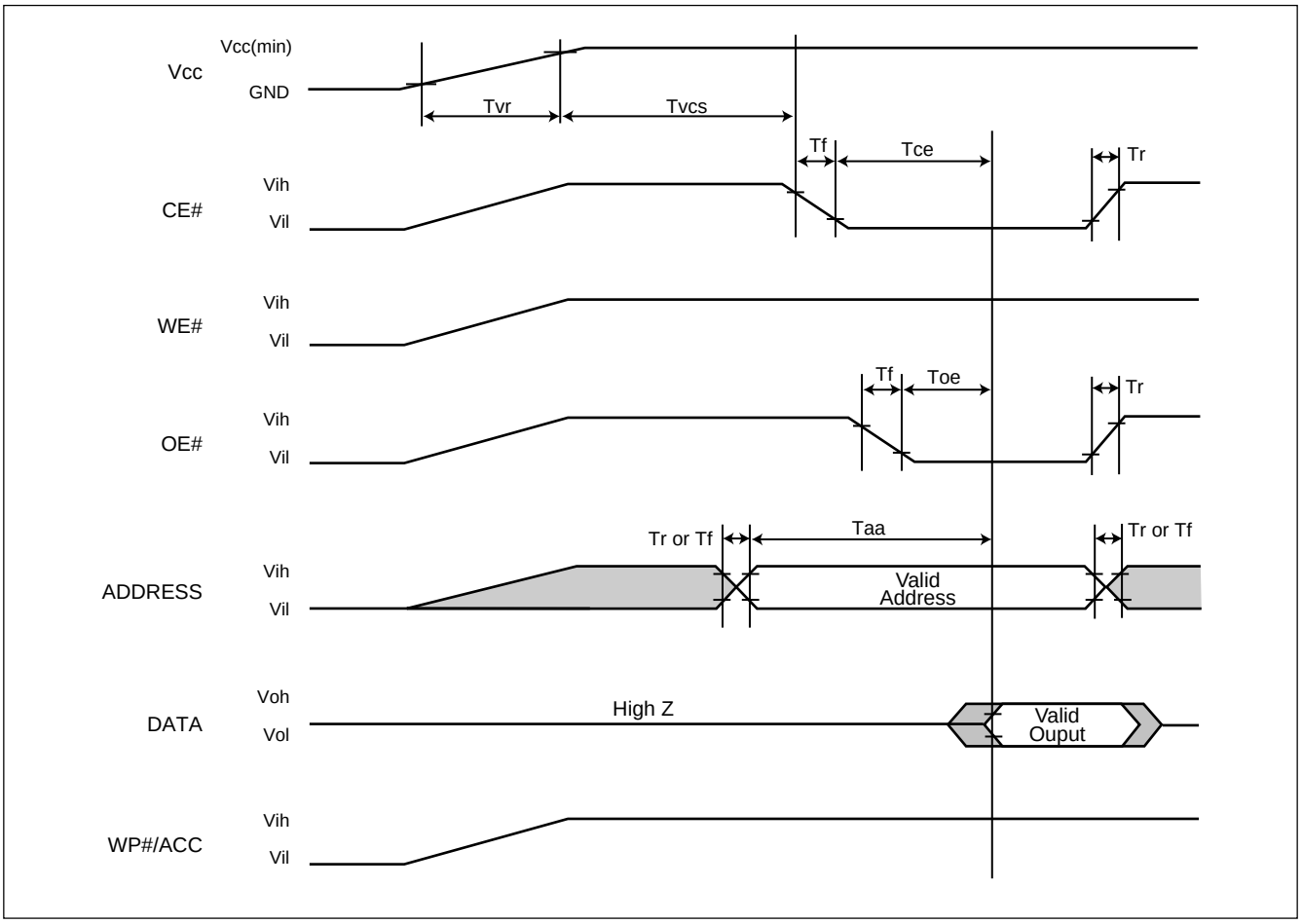


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	us/V
Tr	Input Signal Rise Time		20	us/V
Tf	Input Signal Fall Time		20	us/V

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
Chip Erase Time		45	65	sec
Sector Erase Time		0.9	15	sec
Erase/Program Cycles	100,000			Cycles
Chip Programming Time		45	140	sec
Accelerated Word Program Time		7	210	us
Word Program Time		11	300	us

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage voltage difference with GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage voltage difference with GND on all I/O pins	-1.0V	Vcc + 1.0V
Vcc Current	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing		

TSOP PIN CAPACITANCE

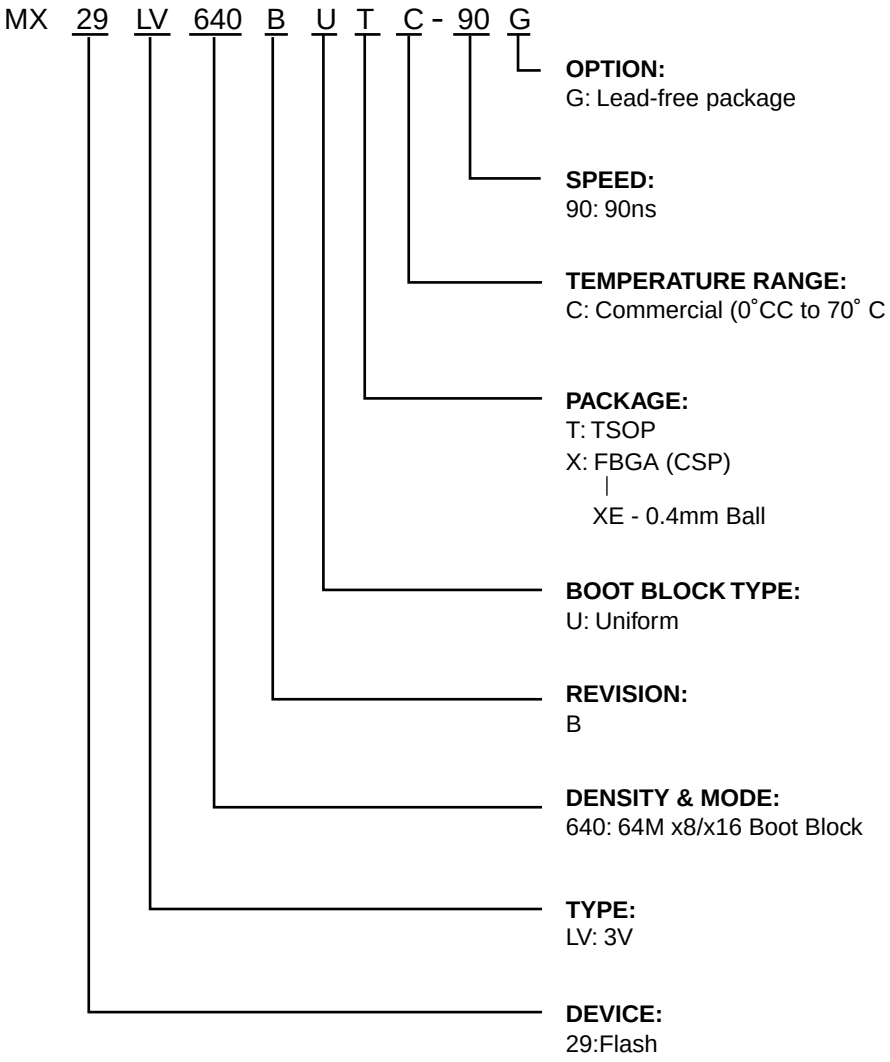
Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	Ball Pitch/ Ball size	PACKAGE	Remark
MX29LV640BUTC-90	90		48 Pin TSOP (Normal Type)	Commercial grade Note 1
MX29LV640BUTC-12	120		48 Pin TSOP (Normal Type)	Commercial grade Note 1
MX29LV640BUTI-90	90		48 Pin TSOP (Normal Type)	Industrial grade Note 1
MX29LV640BUTI-12	120		48 Pin TSOP (Normal Type)	Industrial grade Note 1
MX29LV640BUXBC-90	90	0.8mm/0.3mm	63 Ball CSP	Commercial grade Note 1
MX29LV640BUXBC-12	120	0.8mm/0.3mm	63 Ball CSP	Commercial grade Note 1
MX29LV640BUXBI-90	90	0.8mm/0.3mm	63 Ball CSP	Industrial grade Note 1
MX29LV640BUXBI-12	120	0.8mm/0.3mm	63 Ball CSP	Industrial grade Note 1
MX29LV640BUTC-90G	90		48 Pin TSOP (Normal Type)	Commercial grade Pb-free
MX29LV640BUTC-12G	120		48 Pin TSOP (Normal Type)	Commercial grade Pb-free
MX29LV640BUTI-90G	90		48 Pin TSOP (Normal Type)	Industrial grade Pb-free
MX29LV640BUTI-12G	120		48 Pin TSOP (Normal Type)	Industrial grade Pb-free
MX29LV640BUXBC-90G	90	0.8mm/0.3mm	63 Ball CSP	Commercial grade Pb-free
MX29LV640BUXBC-12G	120	0.8mm/0.3mm	63 Ball CSP	Commercial grade Pb-free
MX29LV640BUXBI-90G	90	0.8mm/0.3mm	63 Ball CSP	Industrial grade Pb-free
MX29LV640BUXBI-12G	120	0.8mm/0.3mm	63 Ball CSP	Industrial grade Pb-free

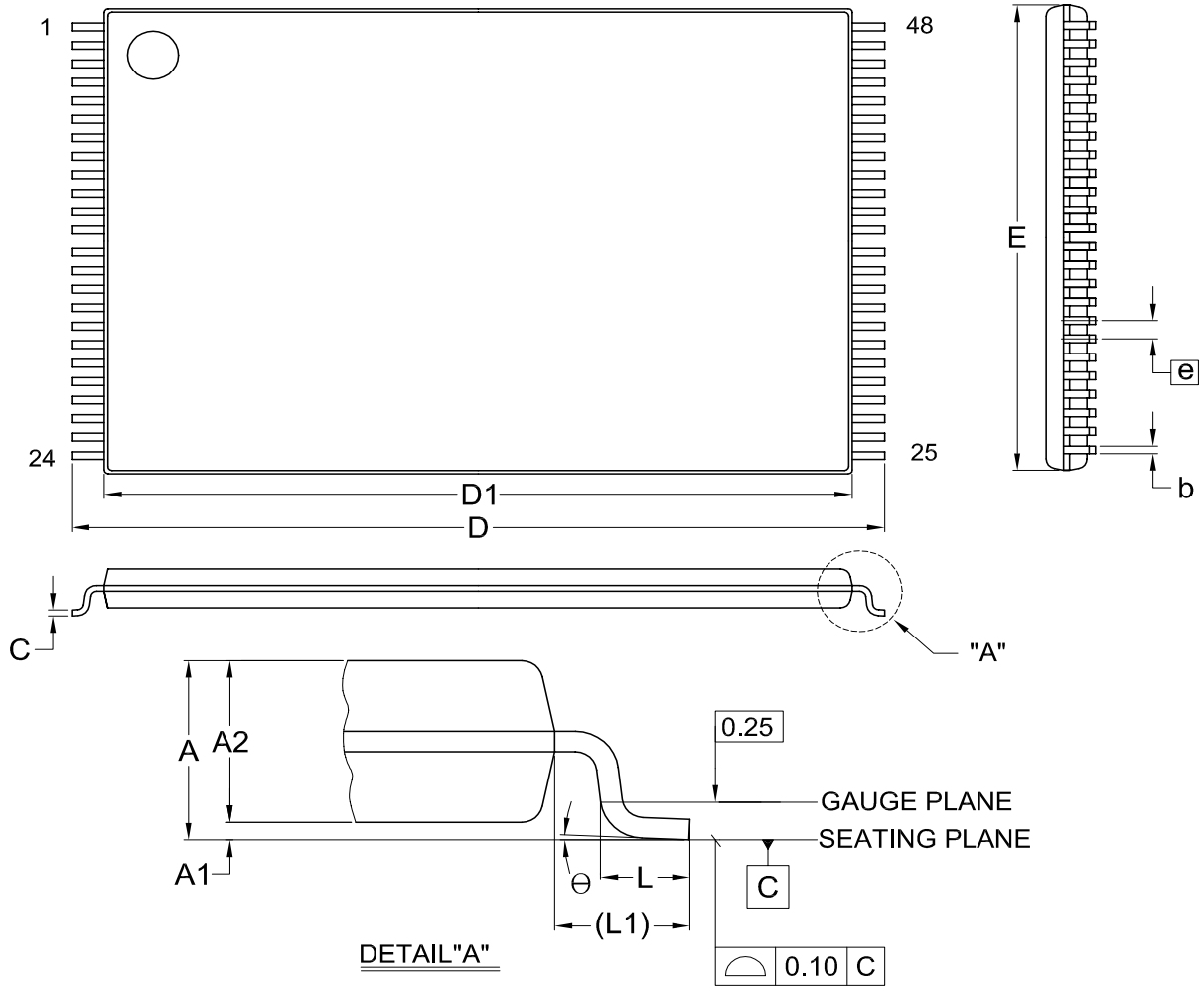
Note 1: The part no. is not recommended for new design in.

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM

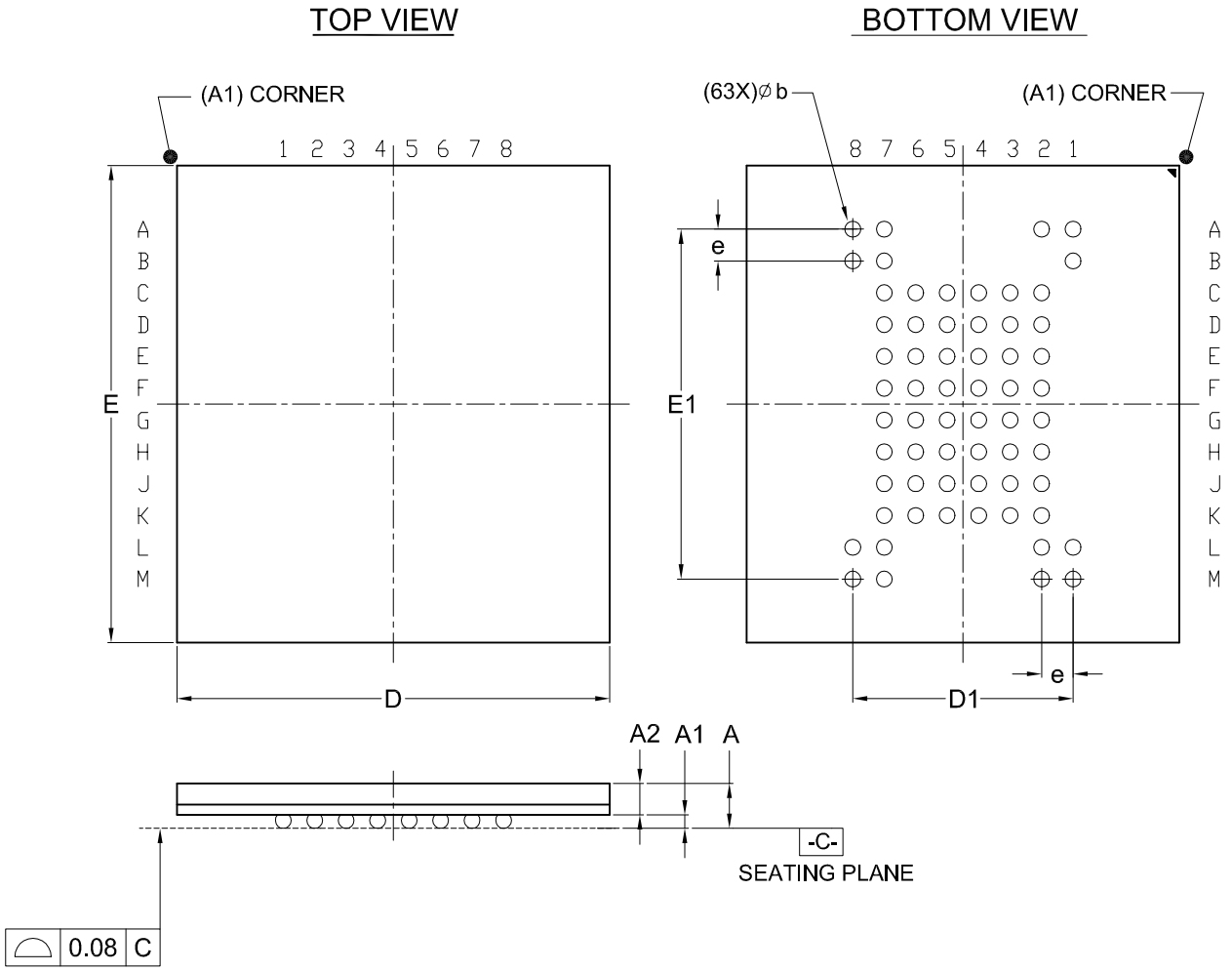


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90	---	0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10	---	0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469	---	0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476	---	0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	8	MO-142			2007/08/03

Title: **Package Outline for CSP 63BALL(11X12X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.3MM)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.18	0.65	0.25	10.90		11.90		
	Nom.	---	0.23	---	0.30	11.00	5.60	12.00	8.80	0.80
	Max.	1.20	0.28	---	0.35	11.10		12.10		
Inch	Min.	---	0.007	0.026	0.010	0.429		0.469		
	Nom.	---	0.009	---	0.012	0.433	0.220	0.472	0.346	0.031
	Max.	0.047	0.011	---	0.014	0.437		0.476		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4226	6	MO-210			03-29-'06

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Preliminary"	P1	MAR/08/2005
1.1	1. Datasheet format changed	All	AUG/15/2006
1.2	1. Data modification	All	AUG/24/2006
1.3	1. Added statement	P56	NOV/06/2006
1.4	1. Added recommedation for non RoHS compliant devices	P1,51	JAN/24/2007
	2. Modified sector erase resume: 400us --> 4ms	P20	
1.5	1. Modified Figure 11. CE# Controlled Write Timing Waveform	P37	FEB/26/2008

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MACRONIX INTERNATIONAL CO., LTD.

Headquarters
Macronix, Int'l Co., Ltd.
16, Li-Hsin Road, Science Park,
Hsinchu, Taiwan, R.O.C.
Tel: +886-3-5786688
Fax: +886-3-5632888

Taipei Office
Macronix, Int'l Co., Ltd.
19F, 4, Min-Chuan E. Road, Sec. 3,
Taipei, Taiwan, R.O.C.
Tel: +886-2-2509-3300
Fax: +886-2-2509-2200

Macronix America, Inc.
680 North McCarthy Blvd.
Milpitas, CA 95035, U.S.A.
Tel: +1-408-262-8887
Fax: +1-408-262-8810
Email: sales.northamerica@macronix.com

Macronix Europe N.V.
Koningin Astridlaan 59, Bus 1
1780 Wemmel Belgium
Tel: +32-2-456-8020
Fax: +32-2-456-8021

Macronix Japan Cayman Islands Ltd.
NKF Bldg. 5F, 1-2 Higashida-cho,
Kawasaki-ku Kawasaki-shi,
Kanagawa Pref. 210-0005, Japan
Tel: +81-44-246-9100
Fax: +81-44-246-9105

Singapore Office
Macronix Pte. Ltd.
1 Marine Parade Central
#11-03 Parkway Centre
Singapore 449408
Tel: +65-6346-5505
Fax: +65-6348-8096

Macronix (Hong Kong) Co., Limited.
702-703, 7/F, Building 9,
Hong Kong Science Park,
5 Science Park West Avenue, Sha Tin, N.T.
Tel: +86-852-2607-4289
Fax: +86-852-2607-4229

http : //www.macronix.com