AmZ8103 • AmZ8104

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- VCC – 1.15V VOH interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability
- AmZ8103 inverting transceivers
- AmZ8104 non-inverting transceivers
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20-pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

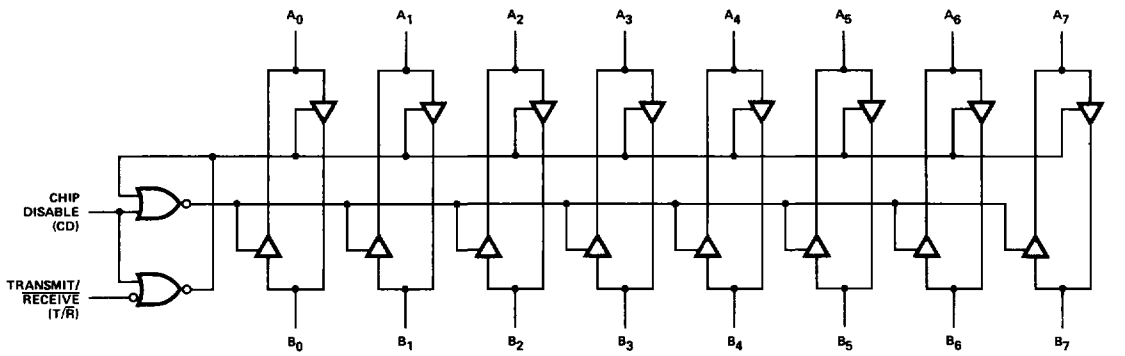
FUNCTIONAL DESCRIPTION

The AmZ8103 and AmZ8104 are 8-bit 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

The output high voltage (VOH) is specified at VCC – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

AmZ8104 LOGIC DIAGRAM



AmZ8103 has inverting transceivers.

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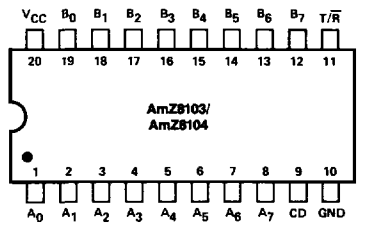
CONNECTION DIAGRAM Top View



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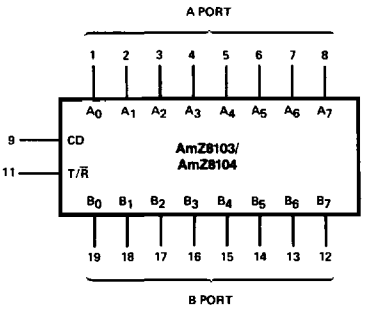
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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VCC = Pin 20
GND = Pin 10

AmZ8103 • AmZ8104

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL T_A = −55 to +125°C VCC MIN = 4.5V VCC MAX = 5.5V
COM'L T_A = 0 to 70°C VCC MIN = 4.75V VCC MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description		Test Conditions		Min	Typ (Note 1)	Max	Units
			A PORT (A0-A7)					
VIH	Logical "1" Input Voltage		CD = VIL MAX, T/R = 2.0V		2.0			Volts
VIL	Logical "0" Input Voltage		CD = VIL MAX, T/R = 2.0V	COM'L			0.8	Volts
				MIL			0.7	
VOH	Logical "1" Output Voltage		CD = VIL MAX, T/R = 0.8V	IOH = −0.4mA	VCC−1.15	VCC−0.7		Volts
				IOH = −3.0mA	2.7	3.95		
VOL	Logical "0" Output Voltage		CD = VIL MAX, T/R = 0.8V	IOL = 12mA		0.3	0.4	Volts
				COM'L, IOL = 24mA		0.35	0.50	
IOS	Output Short Circuit Current		CD = VIL MAX, T/R = 0.8V, VO = 0V, VCC = MAX, Note 2		−10	−38	−75	mA
IIH	Logical "1" Input Current		CD = VIL MAX, T/R = 2.0V, VI = 2.7V			0.1	80	μA
II	Input Current at Maximum Input Voltage		CD = 2.0V, VCC = MAX, VI = VCC MAX				1	mA
IIL	Logical "0" Input Current		CD = VIL MAX, T/R = 2.0V, VI = 0.4V			−70	−200	μA
VC	Input Clamp Voltage		CD = 2.0V, IIN = −12mA			−0.7	−1.5	Volts
IOD	Output/Input 3-State Current		CD = 2.0V	VO = 0.4V			−200	μA
				VO = 4.0V			80	
			B PORT (B0-B7)					
VIH	Logical "1" Input Voltage		CD = VIL MAX, T/R = VIL MAX		2.0			Volts
VIL	Logical "0" Input Voltage		CD = VIL MAX, T/R = VIL MAX	COM'L			0.8	Volts
				MIL			0.7	
VOH	Logical "1" Output Voltage		CD = VIL MAX, T/R = 2.0V	IOH = −0.4mA	VCC−1.15	VCC−0.8		Volts
				IOH = −5mA	2.7	3.9		
				IOH = −10mA	2.4	3.6		
VOL	Logical "0" Output Voltage		CD = VIL MAX, T/R = 2.0V	IOL = 20mA		0.3	0.4	Volts
				IOL = 48mA		.4	0.5	
IOS	Output Short Circuit Current		CD = VIL MAX, T/R = 2.0V, VO = 0V, VCC = MAX, Note 2		−25	−50	−150	mA
IIH	Logical "1" Input Current		CD = VIL MAX, T/R = VIL MAX, VI = 2.7V			0.1	80	μA
II	Input Current at Maximum Input Voltage		CD = 2.0V, VCC = MAX, VI = VCC MAX				1	mA
IIL	Logical "0" Input Current		CD = VIL MAX, T/R = VIL MAX, VI = 0.4V			−70	−200	μA
VC	Input Clamp Voltage		CD = 2.0V, IIN = −12mA			−0.7	−1.5	Volts
IOD	Output/Input 3-State Current		CD = 2.0V	VO = 0.4V			−200	μA
				VO = 4.0V			200	
			CONTROL INPUTS CD, T/R					
VIH	Logical "1" Input Voltage				2.0			Volts
VIL	Logical "0" Input Voltage			COM'L			0.8	Volts
				MIL			0.7	
IIH	Logical "1" Input Current		VI = 2.7V			0.5	20	μA
II	Input Current at Maximum Input Voltage		VCC = MAX, VI = VCC MAX				1.0	mA
IIL	Logical "0" Input Current		VI = 0.4V	T/R		−0.1	−.25	mA
				CD		−0.1	−0.25	
VC	Input Clamp Voltage		IIN = −12mA			−0.8	−1.5	Volts
			POWER SUPPLY CURRENT					
ICC	Power Supply Current	AmZ8103	CD =, VI = 2.0V, VCC = MAX			70	100	mA
			CD = 0.4V, VINA = T/R = 2V, VCC = MAX			100	150	
		AmZ8104	CD = 2.0V, VI = 0.4V, VCC = MAX			70	100	
			CD = VINA = 0.4V, T/R = 2V, VCC = MAX			90	140	

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AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V, T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
tPDHLA	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R1 = 1k, R2 = 5k, C1 = 30pF		8	12	ns
tPDLHA	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R1 = 1k, R2 = 5k, C1 = 30pF		11	16	ns
tPLZA	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S3 = 1, R5 = 1k, C4 = 15pF		10	15	ns
tPHZA	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S3 = 0, R5 = 1k, C4 = 15pF		8	15	ns
tPZLA	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S3 = 1, R5 = 1k, C4 = 30pF		20	30	ns
tPZHA	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S3 = 0, R5 = 5k, C4 = 30pF		19	30	ns
B PORT DATA/MODE SPECIFICATIONS						
tPDHLB	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R1 = 100Ω, R2 = 1k, C1 = 300pF		12	18	ns
		R1 = 667Ω, R2 = 5k, C1 = 45pF		7	12	
tPDLHB	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R1 = 100Ω, R2 = 1k, C1 = 300pF		15	20	ns
		R1 = 667Ω, R2 = 5k, C1 = 45pF		9	14	
tPLZB	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S3 = 1, R5 = 1k, C4 = 15pF		13	18	ns
tPHZB	Propagation Delay from A Logical "1" to 3-State from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S3 = 0, R5 = 1k, C4 = 15pF		8	15	ns
tPZLB	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S3 = 1, R5 = 100Ω, C4 = 300pF		25	35	ns
		S3 = 1, R5 = 667Ω, C4 = 45pF		16	25	
tPZHB	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S3 = 0, R5 = 1k, C4 = 300pF		22	35	ns
		S3 = 0, R5 = 5kΩ, C4 = 45pF		14	25	
TRANSMIT RECEIVE MODE SPECIFICATIONS						
tTRL	Propagation Delay from Transmit Mode to Receive a Logical "0," T/R to A Port	CD = 0.4V (Figure 2) S1 = 1, R4 = 100Ω, C3 = 5pF S2 = 1, R3 = 1k, C2 = 30pF		23	35	ns
tTRH	Propagation Delay from Transmit Mode to Receive a Logical "1," T/R to A Port	CD = 0.4V (Figure 2) S1 = 0, R4 = 100Ω, C3 = 5pF S2 = 0, R3 = 5k, C2 = 30pF		22	35	ns
tRTL	Propagation Delay from Receive Mode to Transmit a Logical "0," T/R to B Port	CD = 0.4V (Figure 2) S1 = 1, R4 = 100Ω, C3 = 300pF S2 = 1, R3 = 300Ω, C2 = 5pF		26	35	ns
tRTH	Propagation Delay from Receive Mode to Transmit a Logical "1," T/R to B Port	CD = 0.4V (Figure 2) S1 = 0, R4 = 1k, C3 = 300pF S2 = 0, R3 = 300Ω, C2 = 5pF		27	35	ns

Notes: 1. All typical values given are for VCC = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

FUNCTIONAL TABLE

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/$\overline{Receive}$	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

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AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V, T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
tPDHLA	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R1 = 1k, R2 = 5k, C1 = 30pF		14	18	ns
tPDLHA	Propagation Delay to a Logical "1" from B Port to A Port	CD =0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R1 = 1k, R2 = 5k, C1 = 30pF		13	18	ns
tPLZA	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S3 = 1, R5 = 1k, C4 = 15pF		11	15	ns
tPHZA	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S3 = 0, R5 = 1k, C4 = 15pF		8	15	ns
tPZLA	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S3 = 1, R5 = 1k, C4 = 30pF		27	35	ns
tPZHA	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S3 = 0, R5 = 5k, C4 = 30pF		19	25	ns
B PORT DATA/MODE SPECIFICATIONS						
tPDHLB	Propagation Delay to Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R1 = 100Ω, R2 = 1k, C1 = 300pF		18	23	ns
		R1 = 667Ω, R2 = 5k, C1 = 45pF		11	18	
tPDLHB	Propagation Delay to Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R1 = 100Ω, R2 = 1k, C1 = 300pF		16	23	ns
		R1 = 667Ω, R2 = 5k, C1 = 45pF		11	18	
tPLZB	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S3 = 1, R5 = 1k, C4 = 15pF		13	18	ns
tPHZB	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S3 = 0, R5 = 1k, C4 = 15pF		8	15	ns
tPZLB	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S3 = 1, R5 = 100Ω, C4 = 300pF		32	40	ns
		S3 = 1, R5 = 667Ω, C4 = 45pF		16	22	
tPZHB	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S3 = 0, R5 = 1k, C4 = 300pF		26	35	ns
		S3 = 0, R5 = 5kΩ, C4 = 45pF		14	22	
TRANSMIT RECEIVE MODE SPECIFICATIONS						
tTRL	Propagation Delay from Transmit Mode to Receive a Logical "0," T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S1 = 0, R4 = 100Ω, C3 = 5pF S2 = 1, R3 = 1k, C2 = 30pF		30	40	ns
tTRH	Propagation Delay from Transmit Mode to Receive a Logical "1," T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S1 = 1, R4 = 100Ω, C3 =5pF S2 = 0, R3 = 5k, C2 = 30pF		28	40	ns
tRTL	Propagation Delay from Receive Mode to Transmit a Logical "0," T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S1 = 1, R4 = 100Ω, C3 = 300pF S2 = 0, R3 = 300Ω, C2 = 5pF		31	40	ns
tRTH	Propagation Delay from Receive Mode to Transmit a Logical "1," T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S1 = 0, R4 = 1k, C3 = 300pF S2 = 1, R3 = 300Ω, C2 = 5pF		28	40	ns

Notes: 1. All typical values given are for VCC = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

DEFINITION OF FUNCTIONAL TERMS

A0-A7 A port inputs/outputs are receiver output drivers when T/$\overline{R}$ is LOW and are transmit inputs when T/$\overline{R}$ is HIGH.

B0-B7 B port inputs/outputs are transmit output drivers when T/$\overline{R}$ is HIGH and receiver inputs when T/$\overline{R}$ is LOW.

CD Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$).

T/$\overline{R}$ Transmit/$\overline{Receive}$ direction control determines whether A port or B port drivers are in 3-state. With T/$\overline{R}$ HIGH A port is the input and B port is the output. With T/$\overline{R}$ LOW A port is the output and B port is the input.

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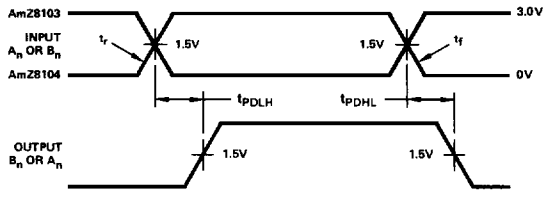
SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



$t_r = t_f < 10ns$
10% to 90%

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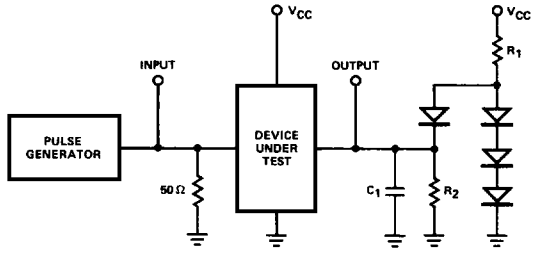

Note: C_1 includes test fixture capacitance.

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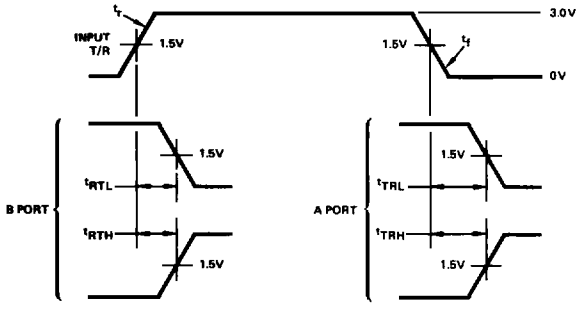
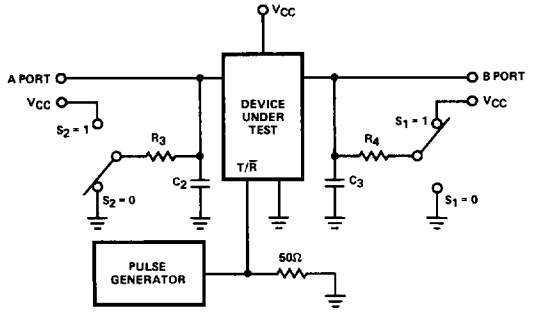
Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.



$t_r = t_f < 10ns$
10% to 90%

BLI-173



Note: C_2 and C_3 include test fixture capacitance.

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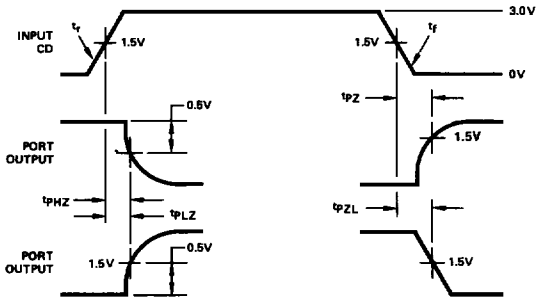
Figure 2. Propagation Delay from T/$\overline{R}$ to A Port or B Port.



$t_r = t_f < 10ns$
10% to 90%

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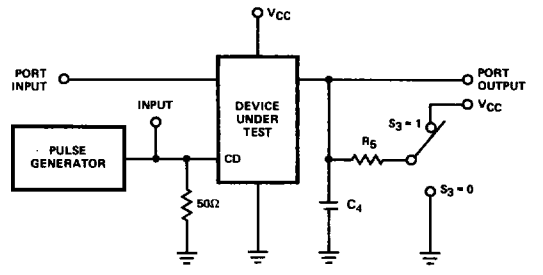

Note: C_4 includes test fixture capacitance.
Port input is in a fixed logical condition.

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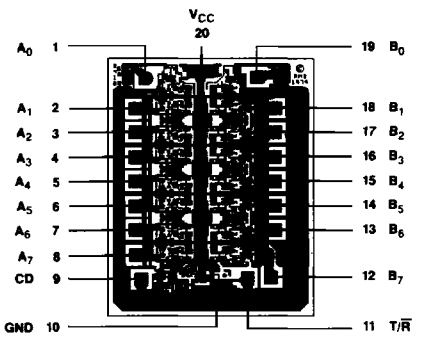
Figure 3. Propagation Delay from CD to A Port or B Port.

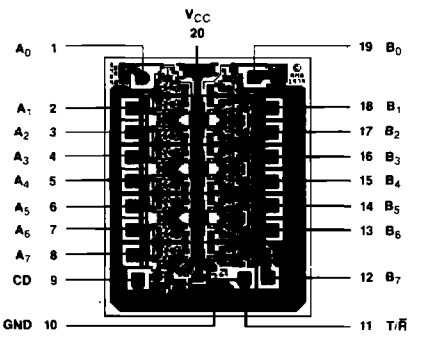
Metallization and Pad Layouts

AmZ8103



DIE SIZE .069" X .089"

AmZ8104



DIE SIZE .069" X .089"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

AmZ8103 Order Number	AmZ8104 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AMZ8103DC	AMZ8104DC	D-20	C	C-1
AMZ8103DCB	AMZ8104DCB	D-20	C	B-1
AMZ8103DM	AMZ8104DM	D-20	M	C-3
AMZ8103DMB	AMZ8104DMB	D-20	M	B-3
AMZ8103PC	AMZ8104PC	P-20	C	C-1
AMZ8103PCB	AMZ8104PCB	P-20	C	C-1

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flatpak. Number following letter is number of leads.
2. C = 0 to 70°C, VCC = 4.75V to 5.25V, M = −55 to +125°C, VCC = 4.50V to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

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