

SN54ABT657, SN74ABT657 OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

SCBS192A - JANUARY 1991 - REVISED JULY 1994

- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

description

The ABT657 transceivers contain eight non-inverting buffers with parity generator/checker circuits and control signals. The transmit/receive (T/R) input determines the direction of data flow. When T/R is high, data flows from the A port to the B port (transmit mode); when T/R is low, data flows from the B port to the A port (receive mode). When the output-enable (\overline{OE}) input is high, both the A and B ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level on the ODD/EVEN input. PARITY carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

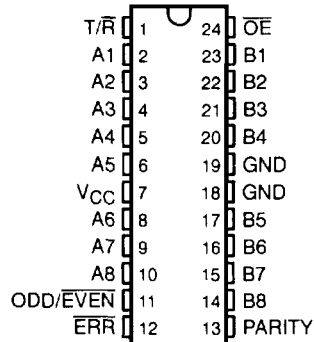
In the transmit mode, after the A bus is polled to determine the number of high bits, PARITY is set to the logic level that maintains the parity sense selected by the level at the ODD/EVEN input. For example, if ODD/EVEN is low (even parity selected) and there are five high bits on the A bus, PARITY is set to the logic high level so that an even number of the nine total bits (eight A-bus bits plus parity bit) are high.

In the receive mode, after the B bus is polled to determine the number of high bits, the error (\overline{ERR}) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if ODD/EVEN is high (odd parity selected), PARITY is high, and there are three high bits on the B bus, \overline{ERR} is low, indicating a parity error.

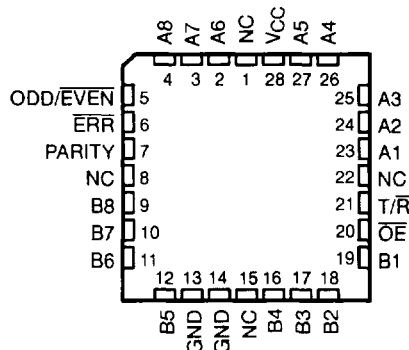
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT657 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

SN54ABT657 ... JT PACKAGE
SN74ABT657 ... DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT657 ... FK PACKAGE
(TOP VIEW)



NC - No internal connection

EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

**TEXAS
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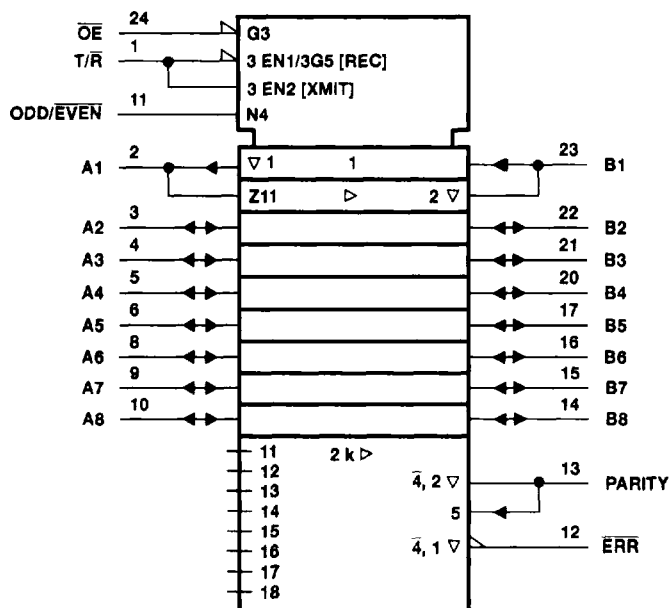
description (continued)

The SN54ABT657 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT657 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{\text{OE}}$	T/ $\overline{\text{R}}$	ODD/ $\overline{\text{EVEN}}$		$\overline{\text{ERR}}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

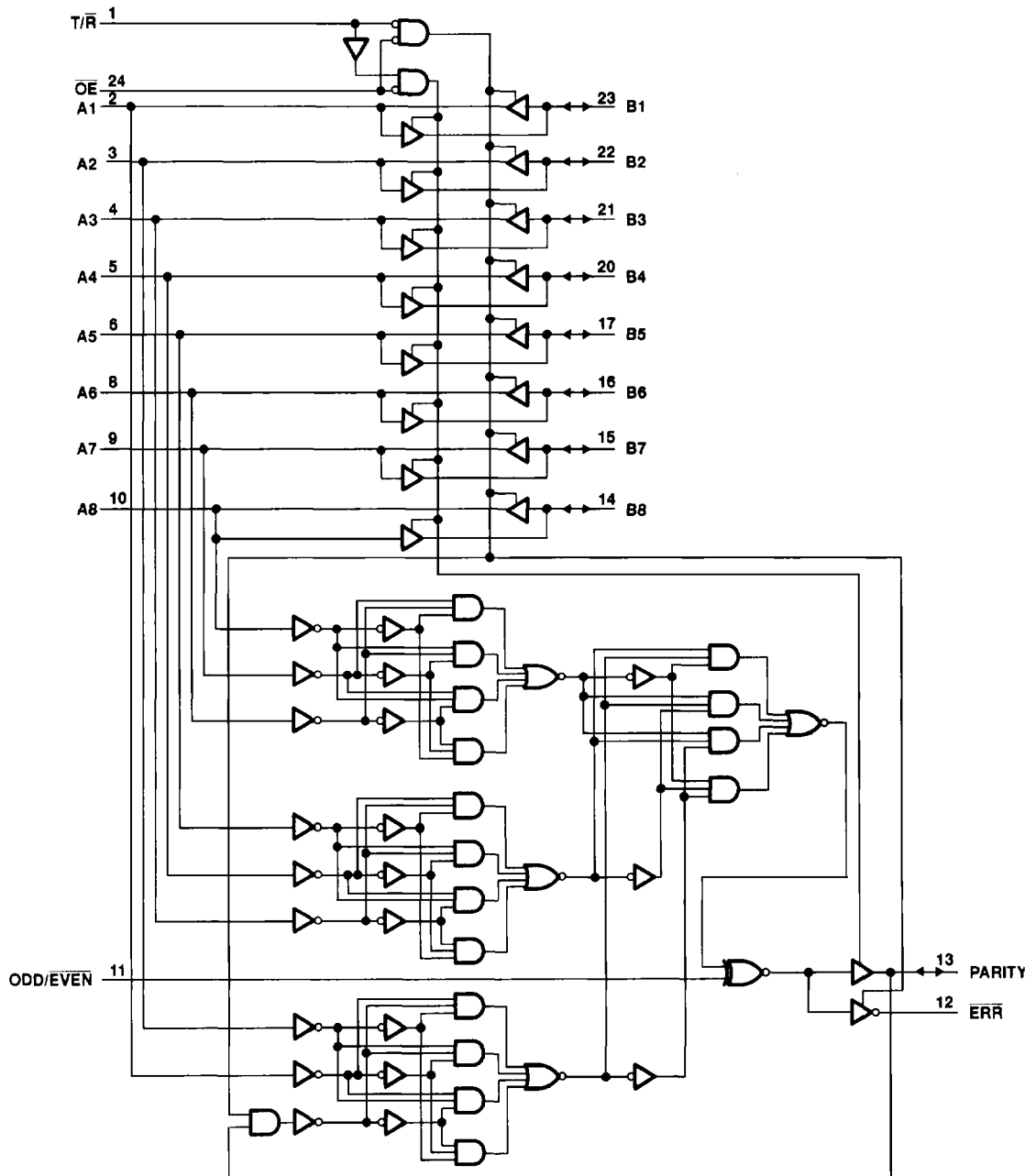


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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT657	96 mA
SN74ABT657	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.65 W
DW package	1.7 W
NT package	1.3 W
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		SN54ABT657		SN74ABT657		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT657		SN74ABT657		UNIT	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA				-1.2		-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA			2.5		2.5		2.5		V	
	V _{CC} = 5 V, I _{OH} = -3 mA			3		3		3			
	V _{CC} = 4.5 V	I _{OH} = -24 mA		2		2					
		I _{OH} = -32 mA		2*				2			
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA			0.55		0.55			V	
		I _{OL} = 64 mA			0.55*			0.55			
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND		Control inputs		±1		±1		±1	μA	
			A or B ports		±100		±100		±100		
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V				50		50		50	μA	
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V				-50		-50		-50	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V				±100				±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50		50	μA	
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V			-50	-100	-180	-50	-180	-50	-180	mA
I _{CC}	V _{CC} = 5.5 V, V _I = V _{CC} or GND, I _O = 0,		Outputs high		250		250		250	μA	
			Outputs low		30		30		30	mA	
			Outputs disabled		250		250		250	μA	
ΔI _{CC} ¶	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Data inputs	Outputs enabled		1		1.5		1	mA	
			Outputs disabled		0.05		0.05		0.05		
		Control inputs		1.5		1.5		1.5			
C _i	V _I = 2.5 V or 0.5 V		Control inputs							pF	
C _{io}	V _O = 2.5 V or 0.5 V		A or B ports							pF	

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

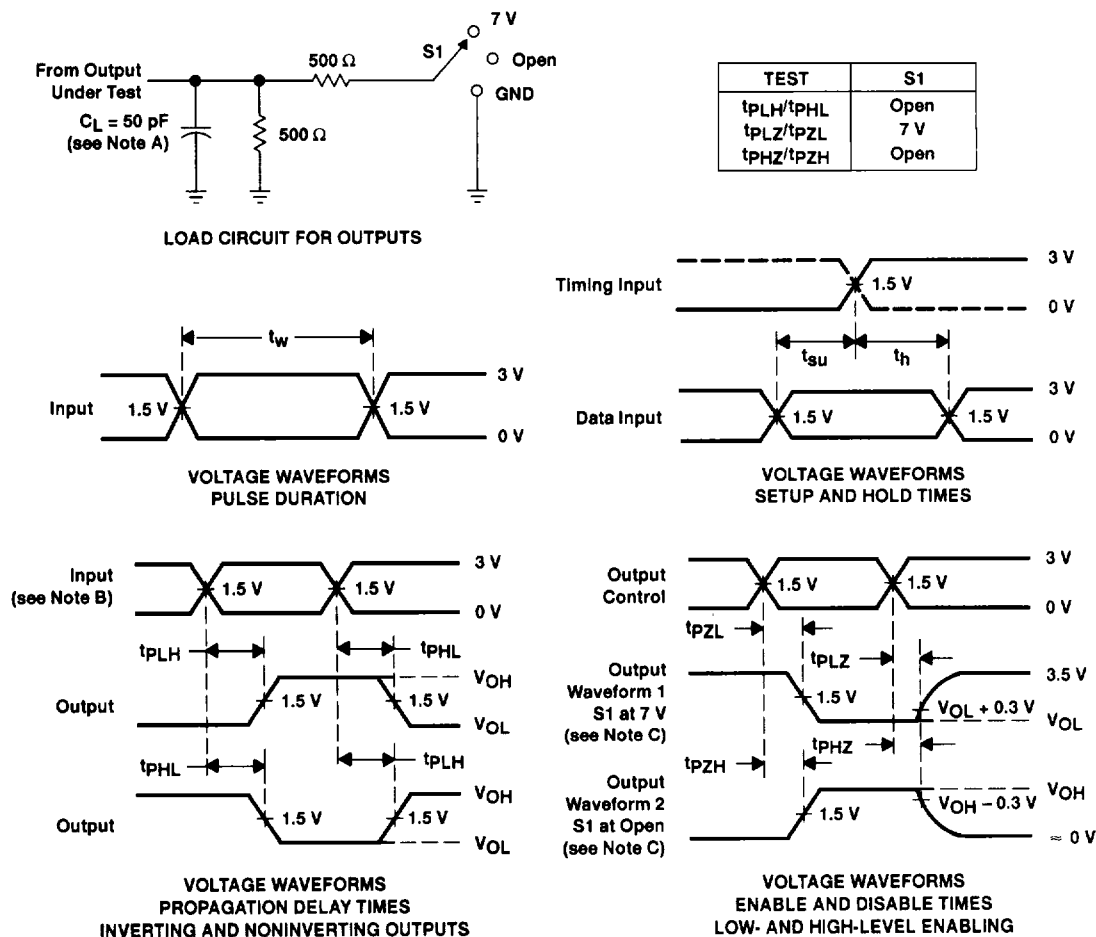
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT657		SN74ABT657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1.1	3.3	5	1.1		1.1	5.5	ns
t _{PHL}			1.2	3	4.3	1.2		1.2	4.8	
t _{PLH}	A	PARITY	2.6	6.5	8.7	2.6		2.6	10.1	ns
t _{PHL}			3.2	7	9.1	3.2		3.2	10.6	
t _{PLH}	ODD/EVEN	PARITY, $\overline{\text{ERR}}$	1.7	5	6.6	1.7		1.7	7.3	ns
t _{PHL}			1.9	5	6.6	1.9		1.9	7.3	
t _{PLH}	B	$\overline{\text{ERR}}$	5.3	9.2	11.7	5.3		5.3	13.8	ns
t _{PHL}			5.2	9.6	12.1	5.2		5.2	14.5	
t _{PLH}	PARITY	$\overline{\text{ERR}}$	2.8	6	7.6	2.8		2.8	9.4	ns
t _{PHL}			3.5	6.4	8	3.5		3.5	9.4	
t _{PZH}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$	1.3	3.8	5.6	1.3		1.3	6.6	ns
t _{PZL}			1.9	4.4	7	1.9		1.9	8.2	
t _{PHZ}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$	3.1	5.1	7	3.1		3.1	7.6	ns
t _{PLZ}			3.4	5.4	7.6	3.4		3.4	8.1	

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms