CY54/74FCT2373T
CY54/74FCT2573T
8-BIT LATCHES

FEATURES

- **Function and pinout compatible with the fastest bipolar logic**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **FCT-C speed at 4.7ns max. (Commercial) FCT-A speed at 5.2ns max. (Commercial)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **12mA sink current (Commercial), 12mA (Mil) 15mA source current (Commercial), 12mA (Mil)**

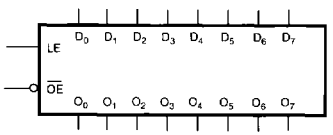
DESCRIPTION

The 'FCT2373T and 'FCT2573T are 8-bit, high-speed CMOS TTL-compatible buffered latches with 3-state outputs that are ideal for driving high-capacitance loads, such as memory and address buffers. On-chip 25Ω termination resistors have been added to the outputs to reduce system noise caused by reflections. 'FCT2373T can be used to replace 'FCT373, and 'FCT2573T to replace 'FCT573 to reduce noise in an existing design. 'FCT2573T is identical to 'FCT2373T except that all inputs are on one side of the package and the outputs on the other side.

When latch enable (LE) is high, the flip flops appear transparent to the data. Data that meets the required set-up times are latched when LE transitions from HIGH to LOW. Data appears on the bus when the output enable ($\overline{OE}$) is LOW. When output enable is HIGH, the bus output is in the high impedance state. In this mode, data can still be entered into the latches.

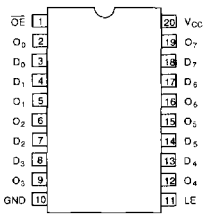
LOGIC SYMBOL

'FCT2373T & 'FCT2573T



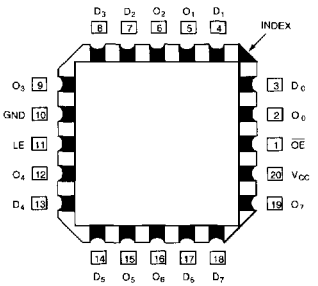
PIN CONFIGURATIONS

TOP VIEW



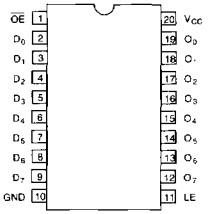
DIP(P5,D6), SOIC (S5), QSOP (Q5)

'FCT2373T TOP VIEW



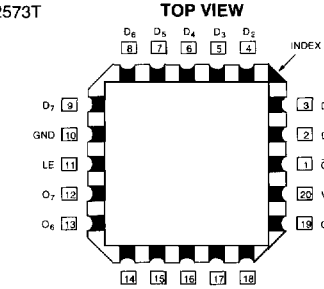
LCC (L61)

TOP VIEW



DIP P5, D6),SOIC(S5), QSOP (Q5)

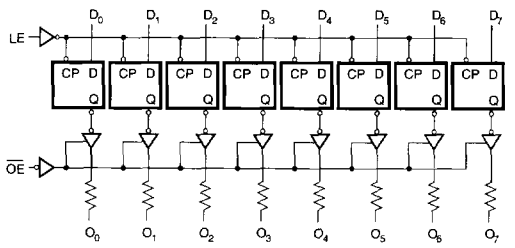
'FCT2573T TOP VIEW



LCC (L61)

LOGIC DIAGRAMS

'FCT2373T - 'FCT2573T



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	28	40	Ω	MIN	I_{OL} = 12mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			6	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[5]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \le 0.2V$, $V_{IN} \le V_{CC} - 0.2V$

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C
Supply Voltage (V_{CC})	**Min**	**Max**
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

FUNCTION TABLES (Each Latch)

Inputs			Outputs 'FCT2373T/'FCT2573T
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Voltage Level Z = HIGH Impedance
L = LOW Voltage Level Q_0 = previous state of flip flops (Q_{n-1})
X = Don't Care

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[3]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[6], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[7]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[9]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		5.2	14.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

Notes:

6. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
8. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS ('FCT2373T — 'FCT2573T)

Sym.	Parameter	'FCT2373T 'FCT2573T				'FCT2373AT 'FCT2573AT				'FCT2373CT 'FCT2573CT				Units	Fig. No*.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.		
t_{PLH} t_{PHL}	Prop Delay D_n to O_n	1.5	8.5	1.5	8.0	1.5	5.6	1.5	5.2	1.5	5.1	1.5	4.7	ns	1, 3
t_{PLH} t_{PHL}	Prop Delay LE to O_n	2.0	14.0	2.0	13.0	2.0	9.8	2.0	8.5	2.0	8.0	2.0	6.9	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	12.5	1.5	11.0	1.5	7.5	1.5	6.5	1.5	6.3	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.5	1.5	7.0	1.5	6.5	1.5	5.5	1.5	5.9	1.5	5.0	ns	
$t_s(H)$ $t_s(L)$	Setup Time, High to Low D_n to LE	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	ns	9
$t_n(H)$ $t_n(L)$	Hold Time, High to Low D_n to LE	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns	
$t_w(H)$	LE Pulse Width High	6.0	–	6.0	–	6.0	–	5.0	–	6.0	–	5.0	–	ns	5

Notes:

10. Minimum limits are guaranteed but not tested on Propagation Delays.

*Refer to the 'Parameter Measurement Information' section in this book. AC Characteristics guaranteed with C_L = 50 pF.

ORDERING INFORMATION