Quad registers

74F379/74F379A

74F379 — Quad parallel register with enable
74F379A — Quad parallel register with enable (light loading 74F379)

FEATURES

- Edge–triggered D–type inputs
- Buffered positive edge–triggered clock
- Buffered common enable input
- True and complementary outputs
- 74F379A offers light loading PNP inputs (I_{IL} = –20μA)

DESCRIPTION

The 74F379/379A are 4–bit registers with buffered common enable ($\overline{E}$). These devices are similar to the 74F175 but feature the common enable rather than common master reset.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F379	120MHz	28mA
74F379A	200MHz	29mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16–pin plastic DIP	N74F379N, N74F379AN
16–pin plastic SO	N74F379D, N74F379AD

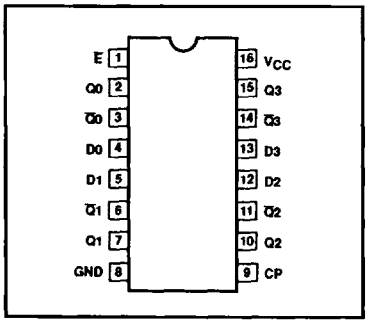
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

TYPE	PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F379	D0 – D3	Data inputs	1.0/1.0	20μA/0.6mA
	CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
	$\overline{E}$	Enable input (active low)	1.0/1.0	20μA/0.6mA
74F379A	D0 – D3	Data inputs	1.0/0.033	20μA/20μA
	CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
	$\overline{E}$	Enable input (active low)	1.0/0.033	20μA/20μA
	Q0 – Q3	True outputs	50/33	1.0mA/20mA
	$\overline{Q0}$ – $\overline{Q3}$	Complementary outputs	50/33	15mA/20mA

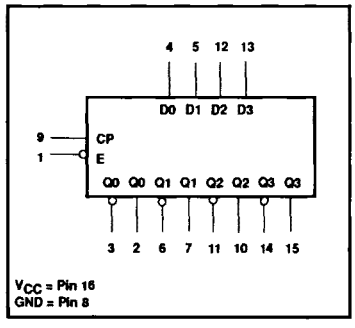
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

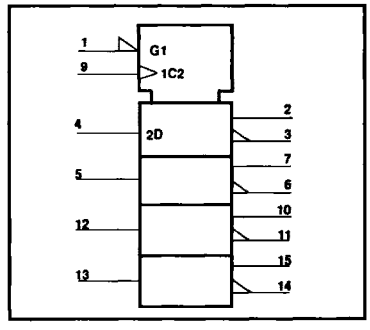
PIN CONFIGURATION



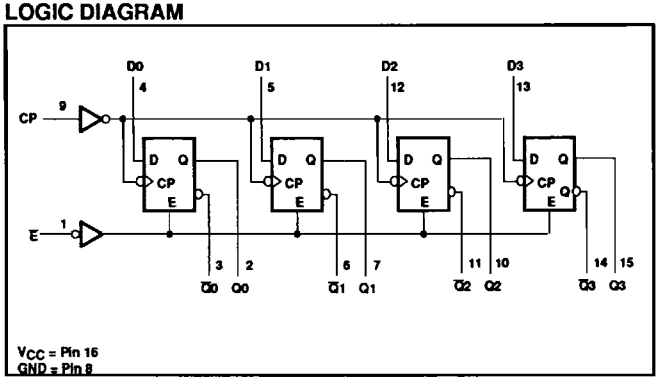
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	
$\overline{E}$	CP	Dn	Qn	$\overline{Q}n$
H	↑	X	NC	NC
L	↑	h	H	L
L	↑	l	L	H

Notes to function table

1. H = High–voltage level
2. h = High state must be present one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low state must be present one setup time before the low–to–high clock transition
5. NC = No change
6. X = Don't care
7. ↑ = Low–to–high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current	74F379	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
		74F379A					–20	µA
I_{OS}	Short–circuit output current3		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	74F379	V_{CC} = MAX			28	40	mA
		74F379A				29	42	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F379

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
f_{max}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Qn}$	Waveform 1	3.5 4.5	5.0 6.5	7.0 8.5	3.5 4.5	8.0 9.5	ns

AC SETUP REQUIREMENTS FOR 74F379

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low level $\overline{E}$ to CP	Waveform 2	6.0 6.0			6.0 6.0		ns
t_h (H) t_h (L)	Hold time, high or low level $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	Waveform 1	4.0 5.0			4.0 5.0		ns

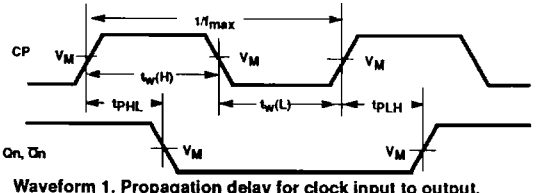
AC ELECTRICAL CHARACTERISTICS FOR 74F379A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	175	200		155		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Q}$n	Waveform 1	2.0 4.0	3.5 5.5	6.5 8.0	2.0 3.5	7.0 8.5	ns

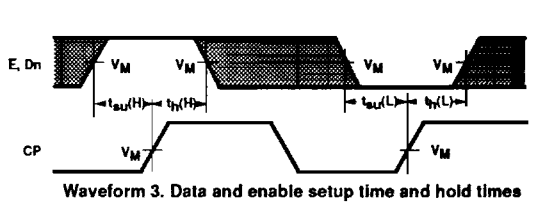
AC SETUP REQUIREMENTS FOR 74F379A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to CP	Waveform 2	3.0 3.0			3.5 3.5		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to CP	Waveform 2	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low level $\overline{E}$ to CP	Waveform 2	4.0 3.5			4.5 4.0		ns
t_h (H) t_h (L)	Hold time, high or low level $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	Waveform 1	3.5 4.5			3.5 4.5		ns

AC WAVEFORMS



Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency

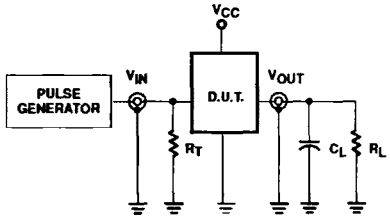


Waveform 3. Data and enable setup time and hold times

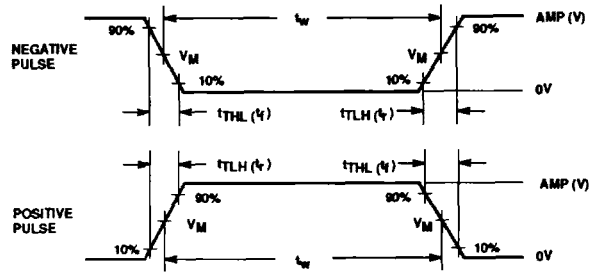
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	v_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.