



# High-Speed CMOS 8-Bit Register with Clock Enable

QS54/74FCT377T  
QS54/74FCT2377T

## FEATURES/BENEFITS

- Pin and function compatible to the 74F377 74FCT377 and 74FCT377T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, LCC
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

### FCT-T 377T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A and C speed grades with 5.2ns tPD for C
- Iol = 48 mA Com., 32 mA Mil.

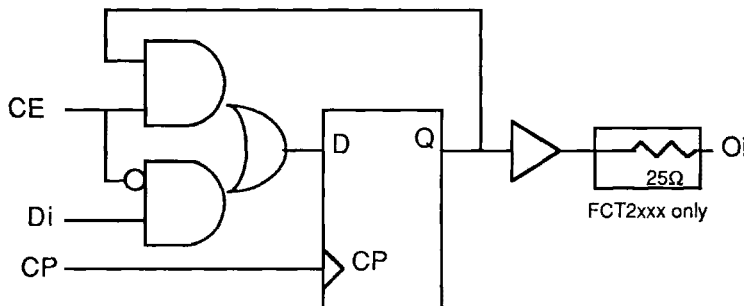
### FCT-T 2377T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A & C speed grades with 5.2ns tPD for C
- Iol = 12mA Com.

## DESCRIPTION

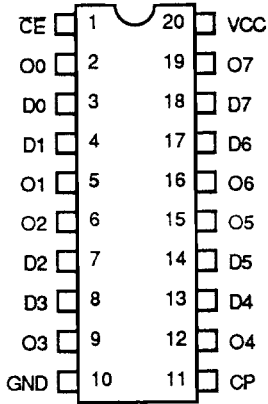
The QSFCT377T and QSFCT2377T are high speed CMOS TTL-compatible registers. They are eight-bit registers with a buffered common clock, a buffered output drive and a synchronous clock enable. The QSFCT2377T is a 25Ω resistor output version useful for driving transmission lines and reducing system noise. Data is stored in the register on the rising edge of the clock if the clock enable input is active. The high output current Iol and loh drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM

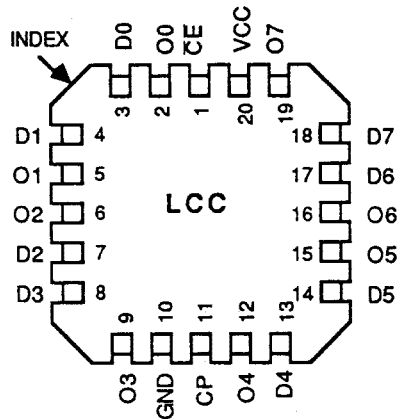
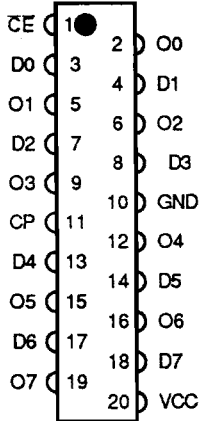


**PIN CONFIGURATIONS**

**PDIP, SOIC, QSOP**



**ZIP**



ALL PINS TOP VIEW

**PIN DESCRIPTION AND FUNCTION TABLE**

**FCT377, 2377**

Name	I/O	Description
Di	I	Data Inputs
O <sub>i</sub>	O	Data Outputs
CP	I	Clock Input
CE	I	Clock Enable

Inputs			Internal Q Value	Outputs	Function
CE	CP	Di		O <sub>i</sub>	
H	X	X	NC	NC	Hold Value
L	↑	L	L	L	Load Input Data
L	↑	H	H	H	

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground..... -0.5V to +7.0V  
 DC Output Voltage  $V_O$  ..... -0.5V to 7.0V  
 DC Input Voltage  $V_I$  ..... -0.5V to 7.0V  
 AC Input Voltage (for a pulse width  $\leq 20$  ns)..... -3.0V  
 DC Input Diode Current with  $V_I < 0$ ..... -20 mA  
 DC Output Diode Current with  $V_O < 0$ ..... -50 mA  
 DC Output Current Max. sink current/pin..... 120 mA  
 Maximum Power Dissipation..... 0.5 watts  
 $T_{STG}$  Storage Temperature..... -65° to +165°C

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{in} = 0\text{V}$ ,  $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,3,4,7,8,11,13,14,17,18	4	4	5	7	pF
2,5,6,9,12,15,16,19	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested

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**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 5\%$

Military  $T_A=-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
$\Delta V_t$	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	$\mu\text{A}$
$ i_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}, 0 \leq V_{in} \leq V_{CC}$		-	-	5	
Ios	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}, V_o = \text{GND} (2,3)$		-60	-	-225	mA
Ior	Current Drive FCT2XXX	$V_{CC} = \text{Min}, V_o = 2.0\text{V} (3)$		50	-	-	mA
Vic	Input Clamp Voltage	$V_{CC} = \text{MIN}, I_{in} = 18 \text{ mA} (3)$		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	loh = 12 mA (MIL)	2.4	-	-	Volts
			loh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	lol = 32 mA (MIL)	-	-	0.50	
			lol = 48 mA (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 $\Omega$ )	$V_{CC} = \text{MIN}$	lol = 12 mA (MIL)	-	-	0.50	
			lol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25 $\Omega$ )	$V_{CC} = \text{MIN}$	lol = 12 mA (MIL)	-	25	-	$\Omega$
			lol = 12 mA (COM)	20	28	40	

**Notes:**

1. Typical values indicate  $V_{CC}=5.0\text{V}$  and  $T_A=25^{\circ}\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I <sub>cc</sub>	Quiescent Power Supply Current	V <sub>cc</sub> = MAX, freq = 0 0V ≤ V <sub>in</sub> ≤ 0.2V or V <sub>cc</sub> - 0.2V ≤ V <sub>in</sub> ≤ V <sub>cc</sub>	-	1.5	mA
ΔI <sub>cc</sub>	Supply Current per Input @ TTL HIGH	V <sub>cc</sub> = MAX, V <sub>in</sub> = 3.4 V, freq = 0 (2)	-	2.0	
Q <sub>ccd</sub>	Supply Current per input per mHz	V <sub>cc</sub> = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V <sub>cc</sub> (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V<sub>i</sub>=3.4V)
3. For flipflops Q<sub>ccd</sub> is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I<sub>c</sub> can be computed using the above parameters as explained in the Technical Overview section.

**QSFCT377T, 2377T**

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5%      Military TA = -55°C to 125° C, Vcc = 5.0V±10%  
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes	377 2377		377A 2377A		377C 2377C		Unit	
			Min	Max	Min	Max	Min	Max		
t PHL t PLH	Propagation Delay CP to Oi, 377	COM	1	2	13	2	7.2	2	5.2	ns
		MIL	1	2	15	2	8.3			
	Propagation Delay CP to Oi, 2377	COM	1	2	13	2	7.2	2	5.2	
		MIL	1	2	15	2	8.3			
t S	Data Setup Times Di to CP	COM		2.5		2		1.5		
		MIL		3		2				
t H	Data Hold Time Di to CP	COM		2		1.5		1		
		MIL		2.5		1.5				
t SC	Clock Enable Setup Time, CE to CP	COM		3		2		1.5		
		MIL		3		2				
t HC	Clock Enable Hold Time CE to CP	COM		1.5		1.5		1		
		MIL		1.5		1.5				
t WCP	Clock Pulse Width HIGH or LOW	COM	2	7		6		4		
		MIL	2	7		6				

**Notes:**

- 1) Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) See Test Circuit and Waveforms.