

# ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H131 Dual Master-Slave Type D Flip-Flop

## Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation, 235 mW typical
- Noise margin of 150 mV
- Voltage compensated
- ECL 10K-compatible

## Description

The MC10H131 is a member of Monolithic Memories' ECL family. The MC10H131 is a dual master-slave D-type flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C) and Clock Enable (CE) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the controlling input(s). A change in the information present at the data (D) input will not affect the data output at any other time due to master slave construction.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power supply current.

## Function Tables

R-S TRUTH TABLE

R	S	$Q_{n+1}$
L	L	$Q_n$
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined.

CLOCKED TRUTH TABLE

C	D	$Q_{n+1}$
L	X	$Q_n$
H↓	L	L
H↑	H	H

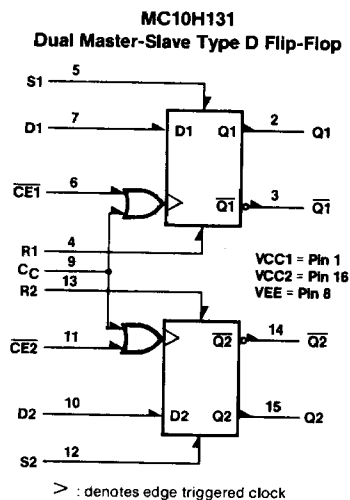
X = Don't Care.

C =  $\overline{CE} + C_C$ .

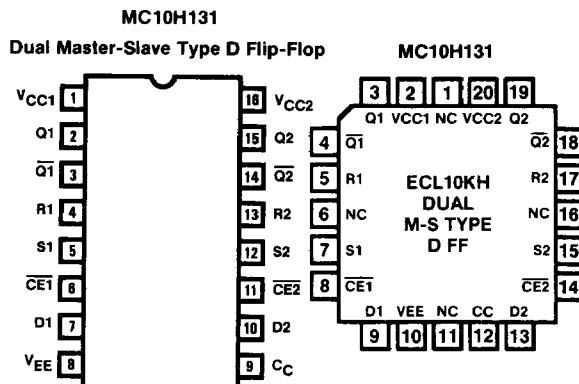
## Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H131	J,N,NL(20)	Com

## Logic Diagram



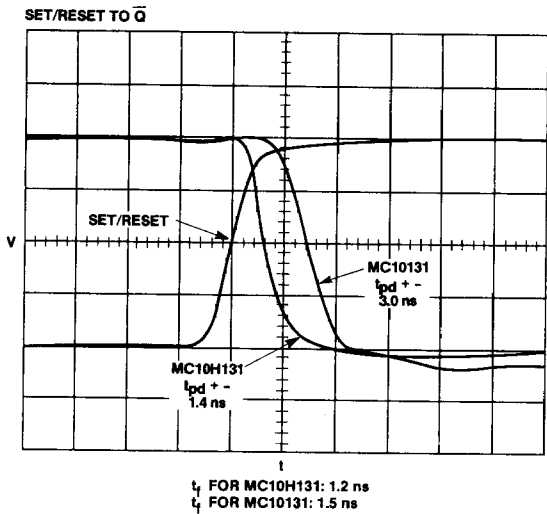
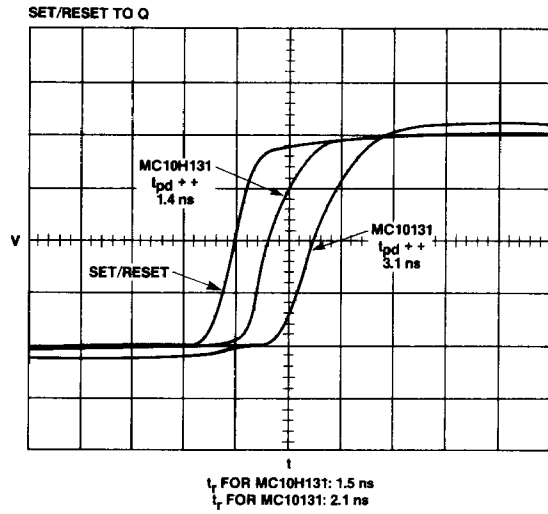
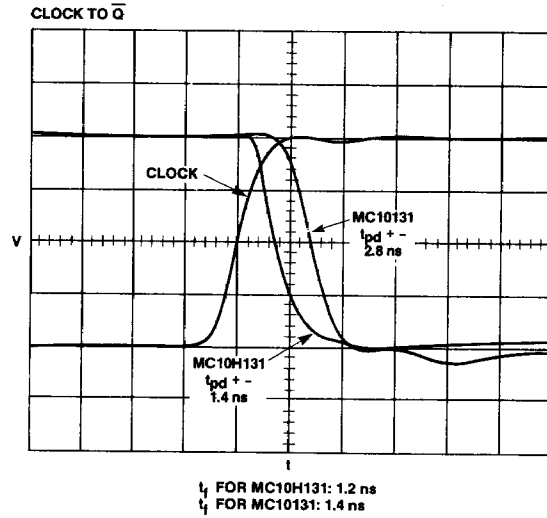
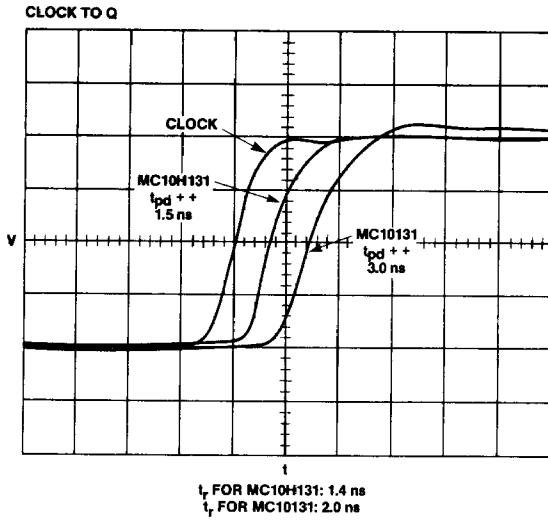
## Pin Configurations



Portions of this Data Sheet reproduced with the courtesy of Motorola Inc.

# MC10H131

## Switching Time Comparison ECL 10KH versus ECL 10K



NOTE:  $t_r$  and  $t_f$  measured from the 20% to the 80% level of the output signal swing.  
 $t_{pd}$  is measured from the 50% level of the input to the 50% level of the output.