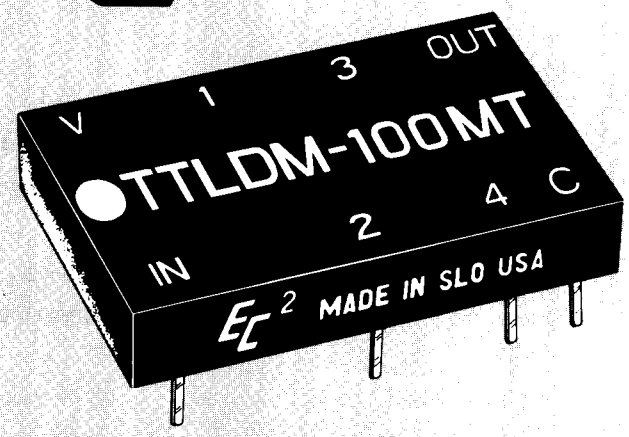


low profile

T^2L COMPATIBLE Thinny DIP LOGIC DELAY MODULE

- Full Military temperature range
- T^2L input and outputs
- Delays stable and precise
- 14-pin DIP package (.165 high)
- Available in delays from 25 to 500ns
- 20% taps – each isolated and with 10 T^2L fan-out capacity
- Fast rise time on all outputs

design notes

The "Thinny DIP Series" Logic Delay Modules developed by Engineered Components Company have been designed to provide precise tapped delays with required driving and pick-off circuitry contained in a single 14-pin DIP package compatible with Schottky T^2L and DTL circuits. These logic delay modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are hermetically sealed in ceramic and are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 3 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The TTLDM is offered in 19 delays from 25ns to 500ns with each module incorporating taps at 20% increments of total delay. Delay tolerances are maintained as shown in the accompanying Part Number Table, when tested under the "Test Conditions" shown. Delay time is measured at the +1.5V level on the leading edge. Rise time for all modules is 4ns maximum, when measured from 0.75V to 2.4V. Temperature coefficient of delay is approximately +500 ppm/°C over the operating temperature range of −55 to +100°C.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the selected output tap without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each module has the capability of driving up to 20 T^2L loads with a maximum of 10 loads on any one tap.

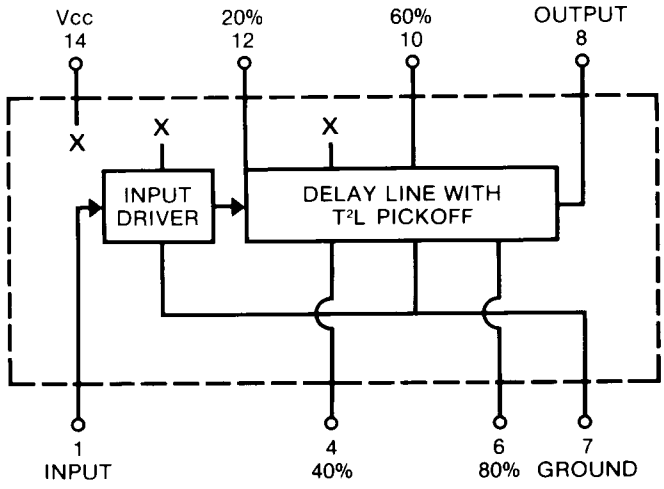
These "Thinny DIP Series" modules are packaged in a 14-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, type SDG-F, and are fully encapsulated in epoxy resin. Flat metal leads meet the solderability requirements of MIL-STD-202, Method 208.

engineered components company
3580 Sacramento Drive, P. O. Box 8121, San Luis Obispo, CA 93403-8121
Phone: (805) 544-3800

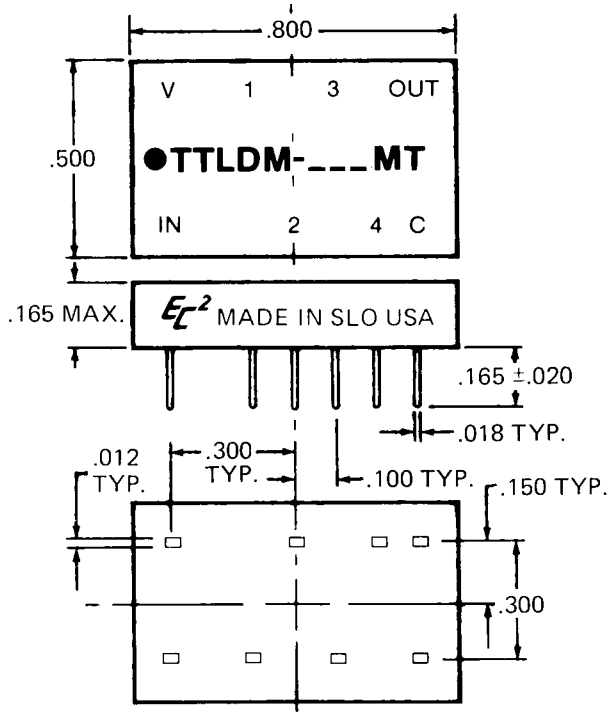
DESIGN NOTES (continued)

Marking consists of manufacturer's name, logo (EC^2), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITIONS

1. All measurements are made at 25°C.
2. Vcc supply voltage is maintained at 5.0V DC.
3. All units are tested using a Schottky toggle-type positive input pulse and one Schottky T^2L load at the output being tested.

φ4. Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

OPERATING SPECIFICATIONS

*Vcc supply voltage: . . . . . 4.75 to 5.25V DC

Vcc supply current:

- Constant "0" in . . . . . 60ma typical
- Constant "1" in . . . . . 20ma typical

Logic 1 input:

- Voltage . . . . . 2V min.; 5.5V max.
- Current . . . . . 2.4V = 50ua max.
  5.5V = 1ma max.

Logic 0 input:

- Voltage . . . . . .8V max.
- Current . . . . . −2ma max.

Logic 1 Voltage out: . . . . . 2.4V min.

Logic 0 Voltage out: . . . . . .4V max.

Operating temperature range: . . . . . −55 to +125°C.

*Delays increase or decrease approximately 2% for a respective increase or decrease of 5% in supply voltage.

PART NUMBER TABLE

φ DELAYS AND TOLERANCES (in ns)					
Part Number	Tap 1	Tap 2	Tap 3	Tap 4	Output
TTLDM-25MT	5 ±1	10 ±1	15 ±1	20 ±1	25 ±1
TTLDM-30MT	6 ±1	12 ±1	18 ±1	24 ±1	30 ±1
TTLDM-35MT	7 ±1	14 ±1	21 ±1	28 ±1.5	35 ±1.5
TTLDM-40MT	8 ±1	16 ±1	24 ±1.5	32 ±1.5	40 ±1.5
TTLDM-45MT	9 ±1	18 ±1	27 ±1.5	36 ±1.5	45 ±2
TTLDM-50MT	10 ±1	20 ±1	30 ±1.5	40 ±2	50 ±2
TTLDM-75MT	15 ±1	30 ±1.5	45 ±2	60 ±2.5	75 ±2.5
TTLDM-100MT	20 ±1	40 ±1.5	60 ±2	80 ±3	100 ±3
TTLDM-125MT	25 ±1	50 ±2	75 ±2.5	100 ±3	125 ±4
TTLDM-150MT	30 ±1.5	60 ±2	90 ±3	120 ±4	150 ±5
TTLDM-175MT	35 ±1.5	70 ±2.5	105 ±4	140 ±5	175 ±5
TTLDM-200MT	40 ±1.5	80 ±2.5	120 ±4	160 ±5	200 ±6
TTLDM-225MT	45 ±2	90 ±3	135 ±4	180 ±6	225 ±7
TTLDM-250MT	50 ±2	100 ±3	150 ±4.5	200 ±6	250 ±8
TTLDM-300MT	60 ±2	120 ±4	180 ±5	240 ±7	300 ±9
TTLDM-350MT	70 ±2	140 ±4.5	210 ±7	280 ±9	350 ±11
TTLDM-400MT	80 ±3	160 ±5	240 ±7	320 ±10	400 ±12
TTLDM-450MT	90 ±3	180 ±6	270 ±8	360 ±11	450 ±14
TTLDM-500MT	100 ±3	200 ±6	300 ±9	400 ±12	500 ±15

φAll modules can be operated with a minimum input pulse width of 40% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.