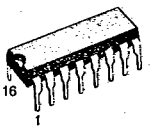
T54LS251
T74LS251

LOW POWER SCHOTTKY INTEGRATED CIRCUITS

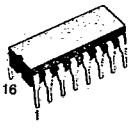
8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The TTL/MSI T54LS251/T74LS251 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

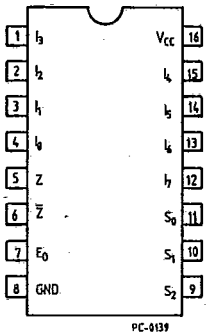
ORDERING NUMBERS:

T54LS251 D2
T74LS251 D1
T74LS251 B1
T74LS251 C1
T74LS251 M1

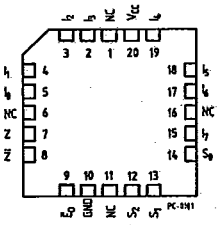
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELCT LOGIC DECODING
- INVERTING AND NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

PIN NAMES

S_0-S_2	Select Input
$\overline{E}_0$	Output Enable (Active LOW) Input
I_0-I_7	Multiplexer Inputs
Z	Multiplexer Outputs
$\overline{Z}$	Complementary Multiplexer Output

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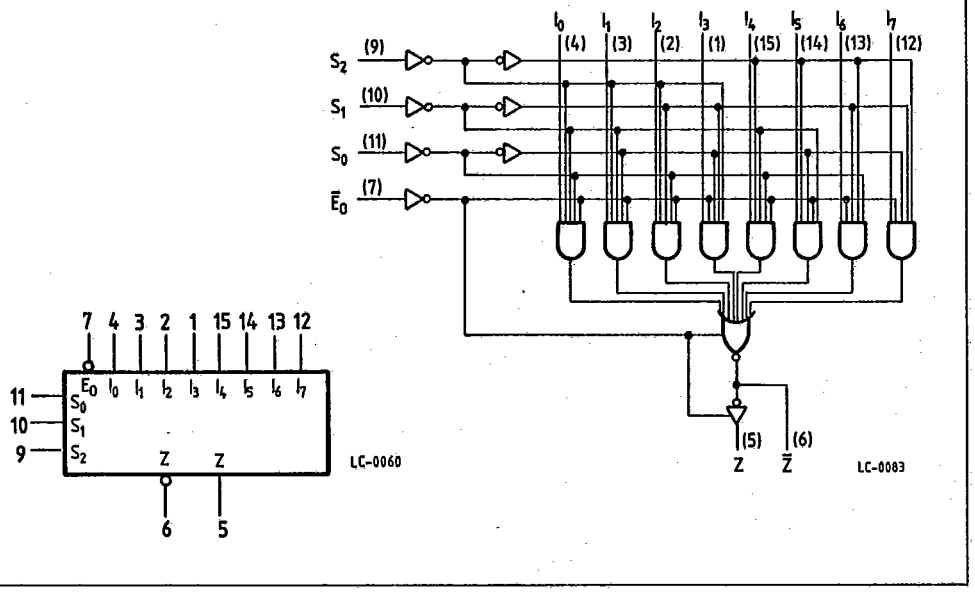
LOGIC SYMBOL AND LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.6 to 5.5	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS251D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS251XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

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FUNCTIONAL DESCRIPTION

The LS251 is a logical implementation of a single pole, 8-position switch the swith position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input (E_0) is active LOW. When it is activated, the logic function provided a the output is:

$$Z = \overline{E}_0 \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 +$$

$$+ I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet {}_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2).$$

When the output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one, device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Outputs Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltage.

TRUTH TABLE

$\overline{E}_0$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (Off)

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Typ.	Max.	Test Conditions (Note 1)		Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		I_{OH} = 1.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.4		I_{OL} = 2.6mA		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA		
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.7V, $V_{\overline{E}}$ = 2.0V		μA
I_{OZL}	Output Off Current LOW				−20	V_{CC} = MAX, V_{OUT} = 0.4V, $V_{\overline{E}}$ = 2.0V		μA
I_{IH}	Input HIGH Current			1.0	20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V		μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current Outputs LOW Outputs Off			6.0 7.0	10 12	V_{CC} = MAX, V_{OUT} = 4.5V, $V_{\overline{E}}$ = 0V V_{CC} = MAX, V_{OUT} = 4.5V, $V_{\overline{E}}$ = 4.5V		mA

AC CHARACTERISTICS: (T_A = 25°C)

Symbol	Parameter	Limits Min.	Typ.	Max.	Test Conditions		Units
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		20 21	33 33	Fig. 1	V_{CC} = 5.0V C_L = 45pF R_L = 667Ω	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		28 28	45 45	Fig. 2		ns
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		10 9.0	15 15	Fig. 1		ns
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		17 18	28 28	Fig. 1		ns
t_{PZH} t_{PZL}	Output Enable Time to $\overline{Z}$ Output		17 24	27 40	Figs. 4,5		ns
t_{PZH} t_{PZL}	Output Enable Time to Z Output		30 26	45 40	Figs. 3,5		ns
t_{PHZ} t_{PLZ}	Output Disable Time to $\overline{Z}$ Output		37 15	55 25	Figs. 3,5	V_{CC} = 5.0V C_L = 50pF	ns
t_{PHZ} t_{PLZ}	Output Disable Time to Z Output		30 15	45 25	Figs. 4,5		ns

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

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3-STATE AC WAVEFORMS AC LOAD CIRCUIT

Fig. 1

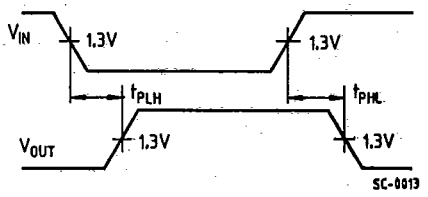


Fig. 2

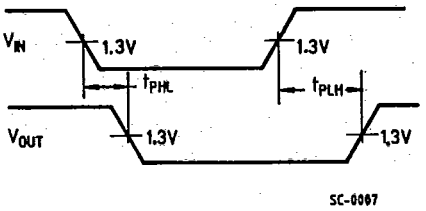


Fig. 3

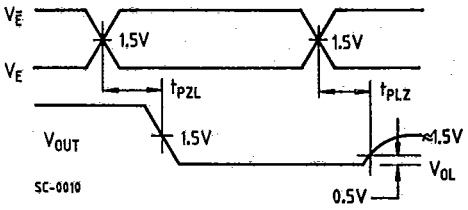


Fig. 4

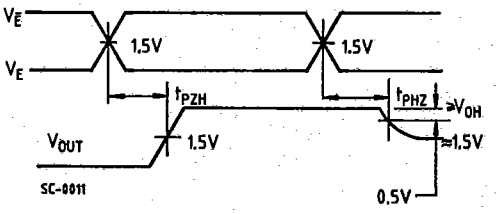
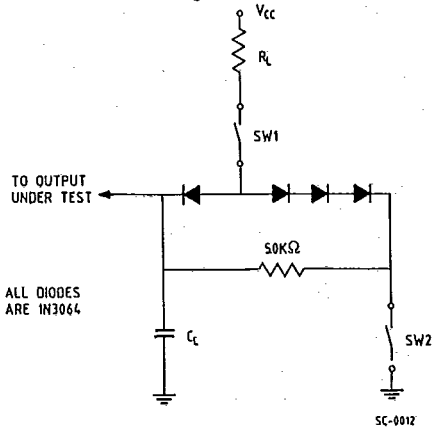


Fig. 5

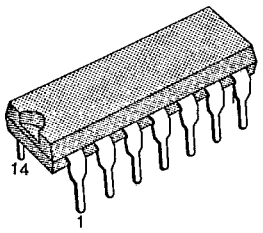


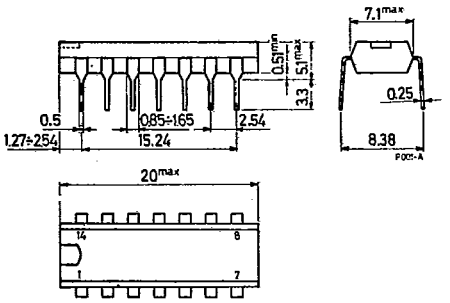
SWITCHING POSITIONS

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

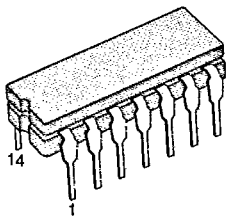
Packages

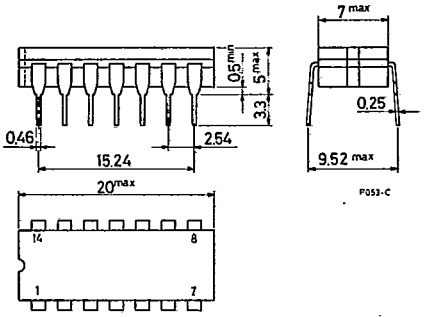
14-LEAD PLASTIC DIP



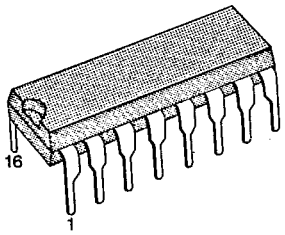


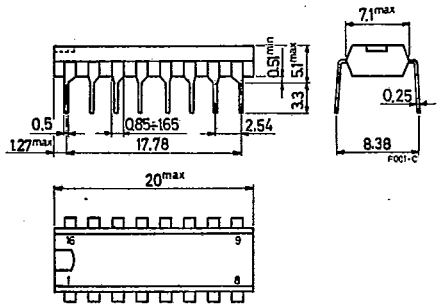
14-LEAD CERAMIC DIP





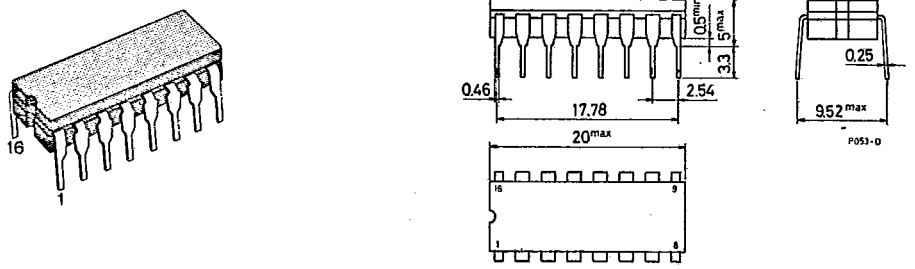
16-LEAD PLASTIC DIP



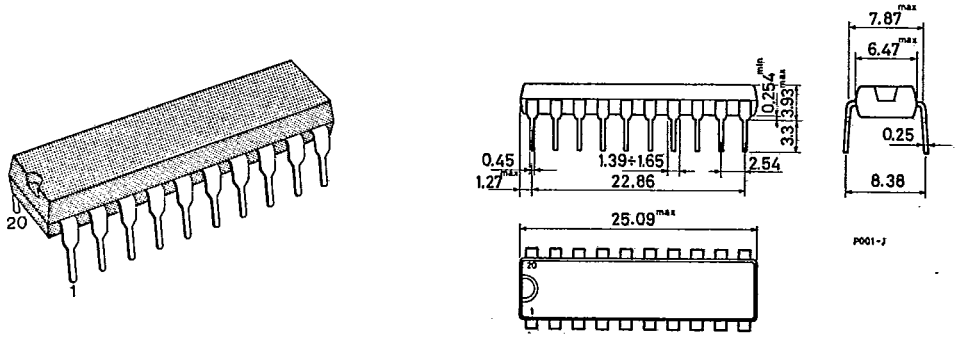


Packages

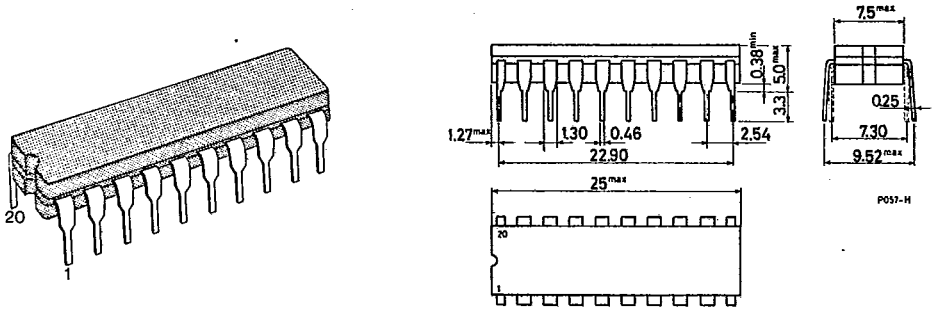
16-LEAD CERAMIC DIP



20-LEAD PLASTIC DIP

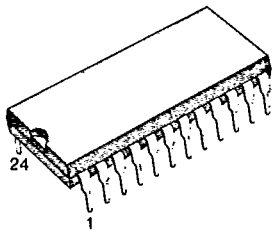


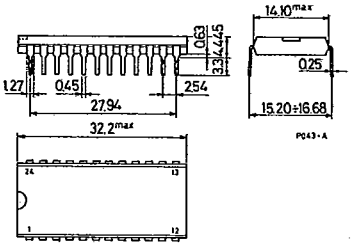
20-LEAD CERAMIC DIP



Packages

24-LEAD PLASTIC DIP





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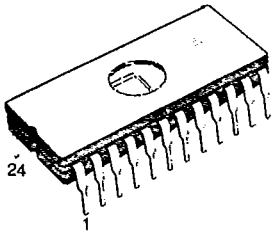
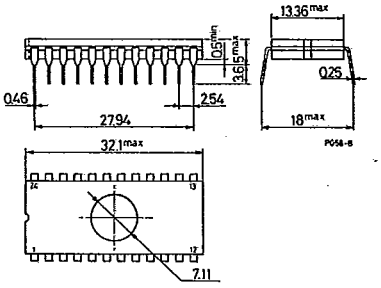
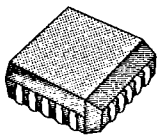
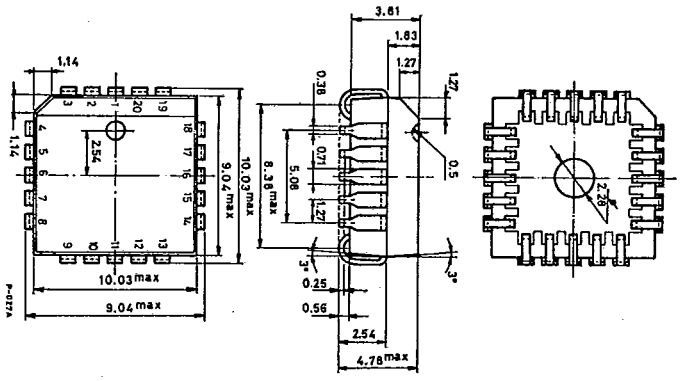




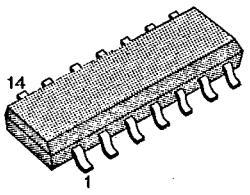
CHIP CARRIER 20 LEAD PLASTIC

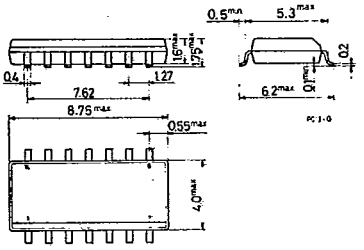




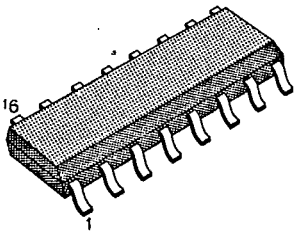
Packages

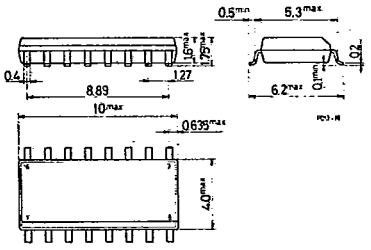
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.