



FailSafe™ PacketClock™ Global Communications Clock Generator

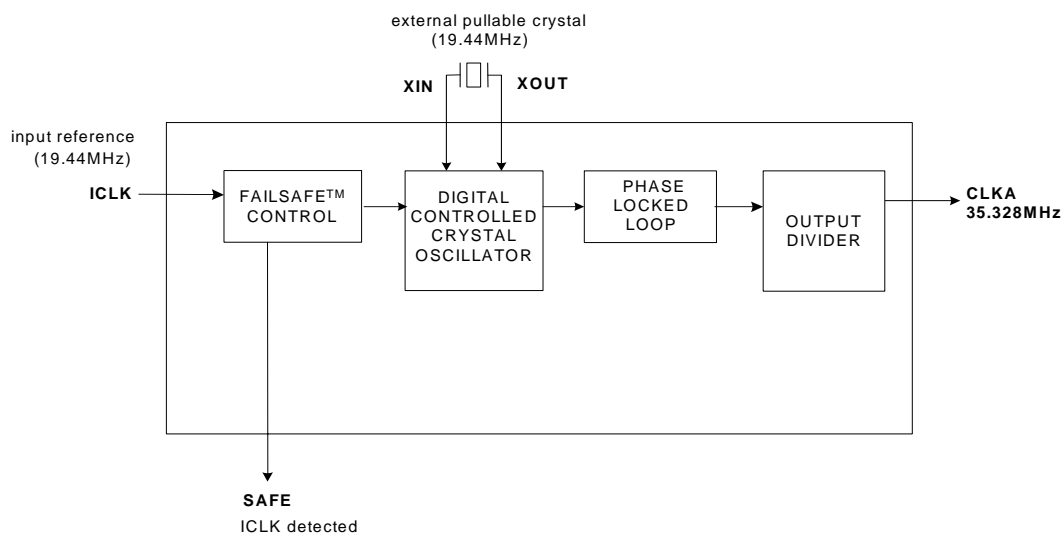
Features

- Fully integrated phase-locked loop (PLL)
- FailSafe™ output
- PLL driven by a crystal oscillator that is phase aligned with external reference
- 35.328-MHz output from 19.44-MHz input
- Low-jitter, high-accuracy outputs
- 3.3V ± 5% operation
- 16-lead TSSOP

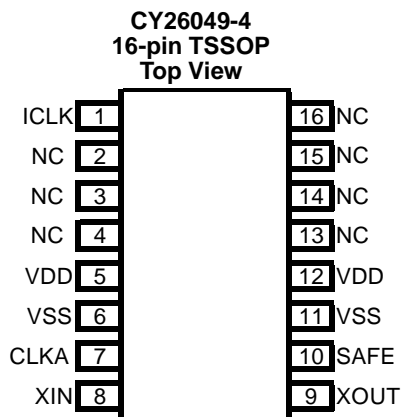
Benefits

- Integrated high-performance PLL tailored for telecommunications frequency synthesis eliminates the need for external loop filter components
- When reference is off, DCXO maintains clock outputs and SAFE pin indicates FailSafe conditions
- DCXO maintains continuous operation should the input reference clock fail
- Glitch-free transition simplifies system design
- FailSafe DCXO loop bandwidth approximately 100Hz
- Works with commonly available, low-cost 19.44-MHz crystal
- Zero-ppm error for all output frequencies
- Compatible across industry standard design platforms
- Industry standard package with 6.4 × 5.0 mm² footprint and a height profile of just 1.1 mm

Logic Block Diagram



Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Description
1	ICLK	Reference Input Clock; 19.44 MHz.
2	NC	No Connect.
3	NC	No Connect.
4	NC	No Connect.
5	VDD	Voltage Supply; 3.3V.
6	VSS	Ground.
7	CLKA	Clock Output; 35.328 MHz.
8	XIN	Pullable Crystal Input; 19.44 MHz.
9	XOUT	Pullable Crystal Output; 19.44 MHz.
10	SAFE	High = reference ICLK within range, Low = reference ICLK out of range.
11	VSS	Ground.
12	VDD	Voltage Supply; 3.3V.
13	NC	No Connect.
14	NC	No Connect.
15	NC	No Connect.
16	NC	No Connect.

Selector Guide

Part Number	Input Frequency Range	Outputs	Output Frequencies
CY26049ZC-4	Reference Input Clock: 19.44 MHz Crystal: 19.44-MHz pullable crystal per Cypress specification	1	35.328 MHz

Description

CY26049-4 is a FailSafe™ frequency synthesizer with a reference clock input and 35.328-MHz output. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure. The continuous, glitch-free operation is achieved by using a DCXO, which serves as a primary clock source. The FailSafe control circuit synchronizes the DCXO oscillator with the reference as long as the reference is within the pull range of the crystal.

In the event of a reference clock failure the DCXO maintains the last frequency of the reference clock. The unique feature of the CY26049-4 is that the DCXO is in fact the primary clocking source. When the reference clock is restored, the DCXO automatically resynchronizes to the reference. The status of the reference clock input, as detected by the CY26049-4, is reported by the SAFE pin.



Absolute Maximum Conditions

Supply Voltage (V_{DD})-0.5 to +7.0V
 DC Input Voltage.....-0.5V to $V_{DD}+0.5$
 Storage Temperature (Non-condensing).....-55°C to +125°C

Junction Temperature -40°C to +125°C
 Data Retention @ $T_j = 125^\circ\text{C}$> 10 years
 Package Power Dissipation..... 350 mW
 ESD (Human Body Model) MIL-STD-883..... 2000V
 (Above which the useful life may be impaired. For user guidelines, not tested.)

Recommended Pullable Crystal Specifications^[1]

Parameter	Description	Comments	Min.	Typ.	Max.	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	-	19.44	-	MHz
C_{LNOM}	Nominal load capacitance		-	14	-	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	-	-	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	-	-	
DL	Crystal drive level	No external series resistor assumed	-	0.5	2	mW
F_{3SEPHI}	Third overtone separation from $3 \cdot F_{NOM}$	High side	400	-	-	ppm
F_{3SEPLO}	Third overtone separation from $3 \cdot F_{NOM}$	Low side	-	-	-200	ppm
C_0	Crystal shunt capacitance		-	-	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	-	250	
C_1	Crystal motional capacitance		14.4	18	21.6	fF

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.15	3.3	3.45	V
T_{AC}	Ambient Temperature (Commercial Temperature)	0	-	70	$^\circ\text{C}$
C_{LOAD}	Max Output Load Capacitance	-	-	15	pF
t_{pu}	Power-up time for all V_{DD} s to reach minimum specified voltage (power ramps must be monotonic)	0.05	-	500	ms

DC Electrical Specifications (Commercial Temp: 0° to 70°C)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.5$, $V_{DD} = 3.3\text{V}$ (source)	12	24	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3\text{V}$ (sink)	12	24	-	mA
V_{IH}	Input High Voltage	CMOS Levels	0.7	-	-	V_{DD}
V_{IL}	Input High Voltage	CMOS Levels	-	-	0.3	V_{DD}
I_{IH}	Input High Current	$V_{IH} = V_{DD}$	-	5	10	μA
I_{IL}	Input Low Current	$V_{IL} = 0\text{V}$	-	5	10	μA
C_{IN}	Input Capacitance		-	-	7	pF
I_{DD}	Supply Current	$C_{LOAD} = 15\text{ pF}$, $V_{DD} = 3.45\text{V}$	-	-	30	mA

AC Electrical Specifications (Commercial Temp: 0° to 70° C)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
f_{ICLK-E}	Frequency, Input Clock	Input Clock Frequency, External Mode	-	19.44	-	MHz
LR	FailSafe Lock Range ^[2]	Range of reference ICLK for Safe = High	-250	-	+250	ppm
$DC = t_2/t_1$	Output Duty Cycle	Duty Cycle defined in Figure 1, measured at 50% of V_{DD}	45	50	55	%
T_{PJIT1}	Clock Jitter; output > 5 MHz	Period Jitter, Peak to Peak, 10,000 periods	-	-	250	ps
		RMS Period Jitter, RMS	-	-	50	ps
t_6	PLL Lock Time	Time for PLL to lock within ± 150 ppm of target frequency	-	-	3	ms

Notes:

1. Ecliptek ECX-5763-19.440M meets these specifications.
2. Dependent on crystals chosen and crystal specs.

AC Electrical Specifications (Commercial Temp: 0° to 70° C) (continued)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_{fs_lock}	FailSafe Lock Time	Time for PLL to lock to ICLK (outputs phase aligned with ICLK and Safe = High)	–	–	7	s
f_{error}	Frequency Synthesis Error	Actual mean frequency error vs. target	–	0	–	ppm
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15$ pF. See Figure 2.	0.8	1.4	2	V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15$ pF. See Figure 2.	0.8	1.4	2	V/ns

Voltage and Timing Definitions

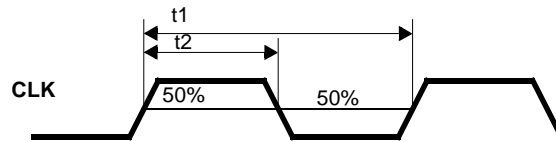


Figure 1. Duty Cycle Definition; $DC = t2/t1$

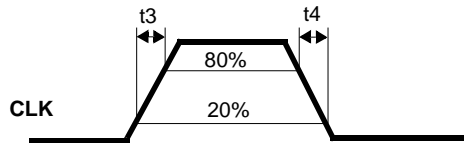
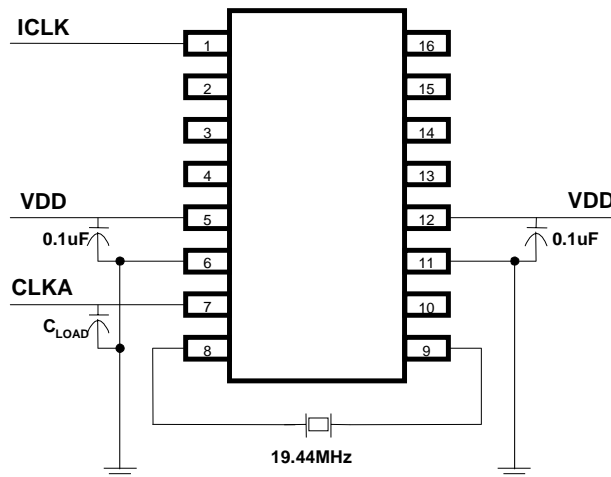


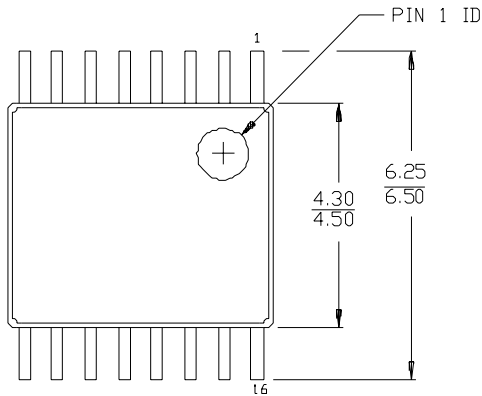
Figure 2. Rise and Fall Time Definitions: $ER = 0.6 \times V_{DD} / t3$, $EF = 0.6 \times V_{DD} / t4$

Test Circuit



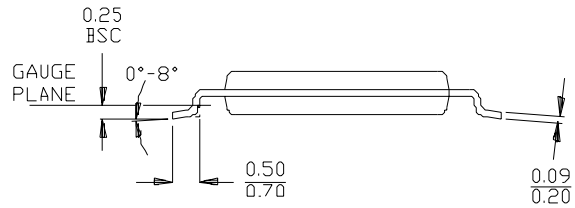
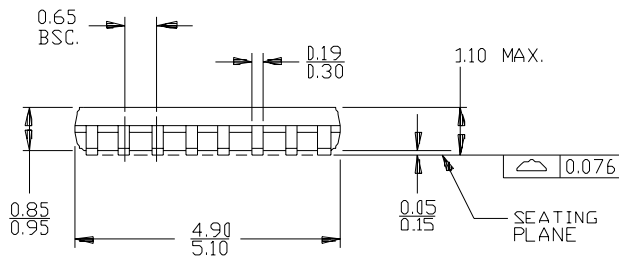
Ordering Information

Ordering Code	Package Type	Operating Temperature Range
CY26049ZC-4	16-lead TSSOP	Commercial 0 to 70°C
CY26049ZC-4T	16-lead TSSOP—Tape and Reel	Commercial 0 to 70°C

Package Drawing and Dimensions
16-lead Thin Shrunken Small Outline Package (4.40 MM Body) Z16


DIMENSIONS IN MILLIMETERS.

MIN.
MAX.



51-85091-**

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Document History Page

Document Title: CY26049-4 FailSafe™ PacketClock™ Global Communications Clock Driver				
Document Number: 38-07484				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	119590	11/01/02	CKN	New Data Sheet
*A	128090	9/11/03	IJA	Changed name from FailSafe™ Communications Clock Generator to FailSafe™ PacketClock™ Global Communications Clock Generator Changed wording in Features and Benefits and Pin Description table Replaced Recommended Pullable Crystal Specifications table