




The VMP2 Clock Oscillator

Features

- Silicon Resonator
- Excellent G Sensitivity Performance
- +2.7V to +3.6V Operation
- CMOS Output
- Output Frequencies to 125 MHz
- Enable/Disable for Board Test and Debug
- -20/70C or -40/85C Operating Temperature
- Industry Standard Plastic SMD Package
- Product is Compliant to RoHS Directive  and Fully Compatible with Lead Free Assembly

Applications

- Microprocessor
- USB
- PC Peripherals
- Digital Camera's
- Ethernet
- Firewire
- PCI

Description

Vectron's VMP2 Clock Oscillator is a silicon MEMS based stabilized square wave generator with a CMOS output, operating off a 3.3V supply.

The VMP2 uses an internal compensation circuit to improve temperature stability which produces performance similar to quartz based products.

VMP2 Data Sheet

Performance Characteristics

Table 1. Electrical Performance					
Parameter	Symbol	Min	Typical	Maximum	Units
Frequency	f_O	1.000		125.000	MHz
Stability (ordering option)		±50, ±100			ppm
Operating Temperature (ordering option)	T_{OP}	-20/70 or -40/85			°C
Operating Supply Voltage ¹	V_{DD}	2.7	3.3	3.6	V
Supply Current, Output Enabled	I_{DD}				
1 to 40 MHz				9	mA
40.01 to 80 MHz				10	mA
80.01 to 125 MHz				16	mA
Supply Current, Output Disabled	I_{DD}			1	uA
Output Logic Levels					
Output Logic High ²	V_{OH}	$0.9 \cdot V_{DD}$			V
Output Logic Low ²	V_{OL}			$0.1 \cdot V_{DD}$	V
Output Load		$\geq 10\text{Kohm}$ $ $ $\leq 15\text{pf}$			
Output Rise/Fall Time ²	t_R t_F			5 5	ns
Duty Cycle ³	SYM			45/55	%
Period Jitter, RMS, 125MHz output			7		ps
Start-up time				10	ms
Enable/Disable ⁴					V
Output Enabled		$0.8 \cdot V_{DD}$			
Output Disabled				$0.2 \cdot V_{DD}$	

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the operating conditions under which these parameters are tested and specified.
3. Duty Cycle is measured defined as On Time/Period.
4. Output will be indeterminate if Enable/Disable is left open.

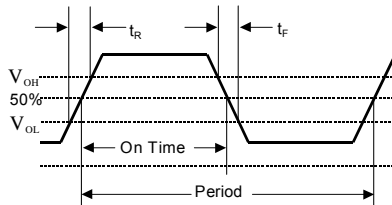


Figure 1. Output Waveform

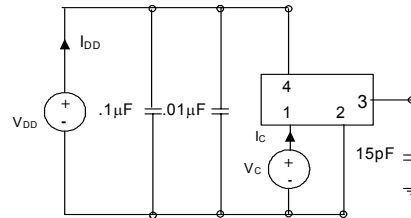


Figure 2. Typical Output Test Conditions (25±5°C)

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Table 2. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	-0.3 to +4.0	V
CMOS Input Voltage		-0.3 to ($V_{DD}+0.3$)	V
CMOS Output Voltage		-0.3 to ($V_{DD}+0.3$)	V
Junction Temperature		150	°C
Storage Temperature	T_{STR}	-55 to 125	°C
Soldering Temperature / Duration	T_{PEAK} / t_P	260 / 10	°C / sec

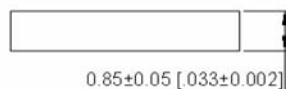
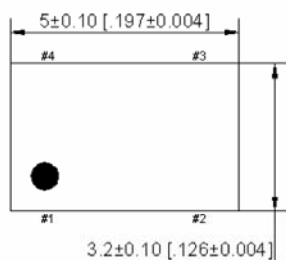
Enable/Disable Functional Description

Under normal operation the E/D is set to a logic high state or logic low state. When E/D is set to a logic low, the oscillator stops and the output is in a high impedance state. This helps reduce power consumption as well as facilitating board testing and troubleshooting. When E/D is set to a logic high state, the oscillator produces an output. Leaving the Enable/Disable pin open results in an indeterminate output state.

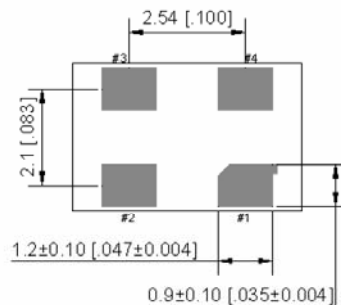
Table 3. Outline Diagrams, Pad Layout and Pin Out

Pin #	Symbol	Function
1	E/D	Enable/Disable
2	GND	Electrical and Case Ground
3	f_O	Output Frequency
4	V_{DD}	Supply Voltage

External Dimensions

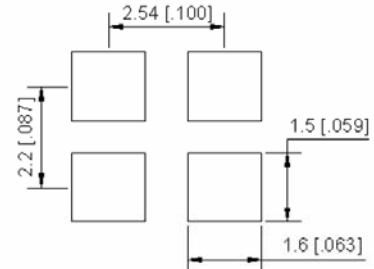


units: mm[inch]



No.	Pin terminal
1	Disable
2	Gnd
3	Output
4	V_{DD}

Recommended land pattern



Devices will be marked with the frequency, a date code and assembly ID information

Figure 3, Package drawing

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Reliability

The VMP2 qualification tests will include:

Table 4. Environmental Compliance	
Parameter	Conditions
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Resistance to Solvents	MIL-STD-883 Method 2015
Moisture Sensitivity Level	MSL1

Handling Precautions

Although ESD protection circuitry has been designed into the the VMP2, proper precautions should be taken when handling and mounting. VI employs a Human Body Model and a Charged-Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model.

Table 5. ESD Ratings	
Model	Minimum
Human Body Model	2000V
Charged Device Model	500V
Machine Model	200V

Suggested IR Profile

Devices are built using lead free epoxy and can also be subjected to standard lead free IR reflow conditions. Figure 4 shows max temperatures and lower temperatures can also be used e.g. peak temperature of 260C.

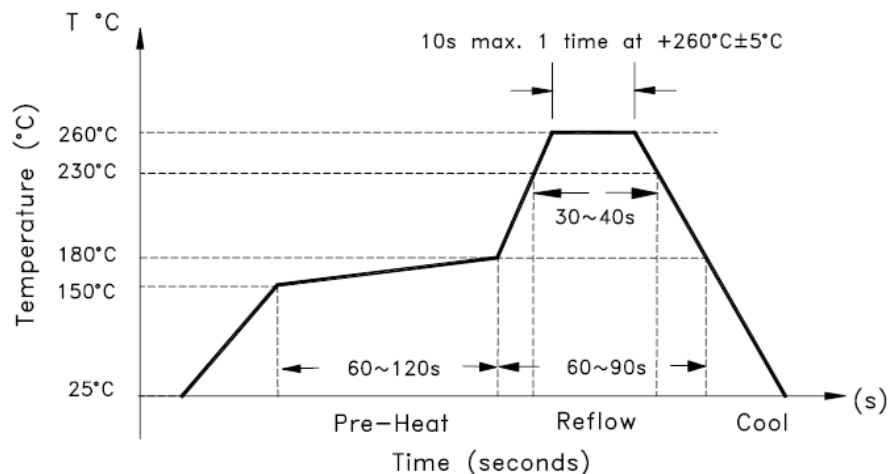


Figure 4

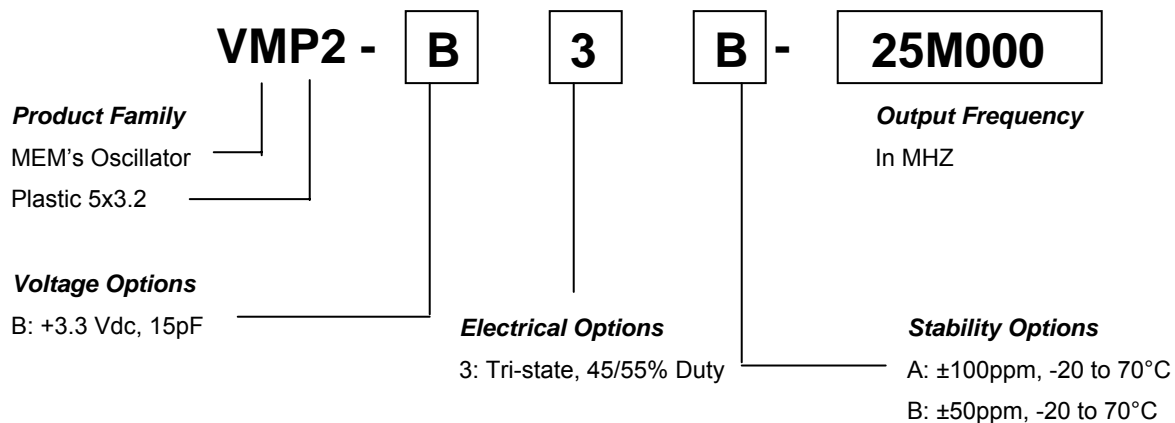
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Table 6. Standard Frequencies (MHz)

2.000	3.686	4.000	4.032	4.9152	5.000	6.000	7.3728	7.680	8.000
9.216	9.600	10.000	12.000	12.500	12.729	14.31818	14.746	16.000	16.128
17.000	20.000	21.000	21.500	22.000	23.000	24.000	25.000	26.000	27.000
29.4912	30.000	32.000	33.000	33.333	36.000	37.500	40.000	42.500	45.000
48.000	50.000	55.000	56.448	58.320	60.000	64.000	66.000	66.666	72.000
75.000	80.000	83.333	84.000	95.000	100.000	110.000	112.500	114.000	115.200
116.640	125.000								

Other frequencies available upon request. Standard frequencies does not imply a stock position.

Ordering Information



2500 pieces per reel, standard
1000 pieces per reel, optional

For Additional Information, Please Contact:



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Rev date: August 28, 2007