

KM416C1000L/LL**CMOS DRAM***1M × 16 Bit CMOS Dynamic RAM with Fast Page Mode***FEATURES**

• Performance range:

	t_{RAC}	t_{CAC}	t_{RC}
KM416C1000L/LL-7	70ns	20ns	130ns
KM416C1000L/LL-8	80ns	20ns	150ns
KM416C1000L/LL-10	100ns	25ns	180ns

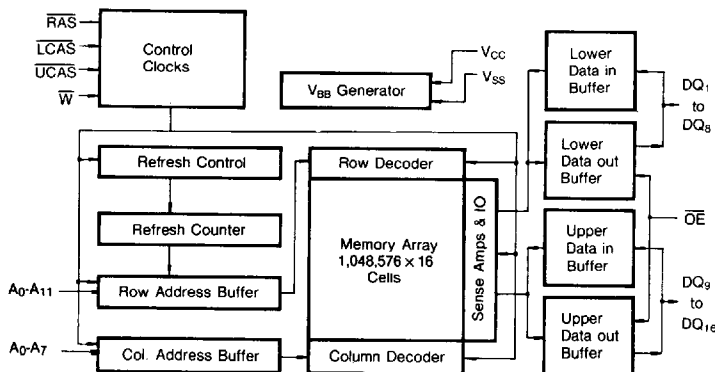
- Fast Page Mode operation
- 2 CAS Byte/Word Read/Write operation
- Self Refresh Capability (LL-version)
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Triple +5V ± 10% power supply
- 4096 cycles 256ms refresh
- Power Dissipation
 - Standby : 1.65mW
 - Active(70/80/100) : 550/495/440mW
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP II Packages

GENERAL DESCRIPTION

The Samsung KM416C1000L/LL is a CMOS high speed 1,048,576 bit × 16 Dynamic Random Access Memory. It's design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C1000L/LL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

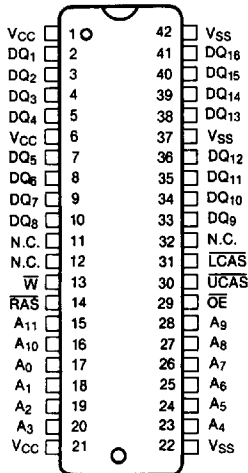
The KM416C1000L/LL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

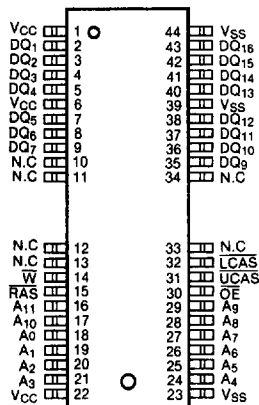
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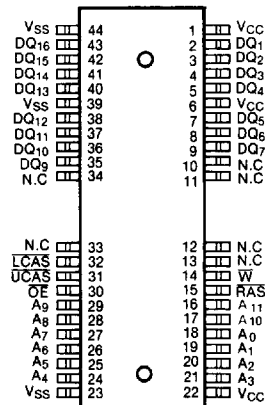
• KM416C1000LJ/LLJ



• KM416C1000LT/LLT



• KM416C1000LTR/LLTR



Pin Names	Pin Function
A ₀ -A ₁₁	Address Inputs
DQ ₁₋₁₆	Data In/Out
V _{SS}	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
V _{CC}	Power (+5V)
N.C.	No Connection

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ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS} , $T_A=0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current (\overline{UCAS} or \overline{LCAS} , Address Cycling @ $t_{RC}=\min.$)	KM416C1000L/LL-7	—	100	mA
	KM416C1000L/LL-8	—	90	mA
	KM416C1000L/LL-10	—	80	mA
Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}$)	I_{CC2}	—	2	mA
\overline{RAS} -Only Refresh Current* ($\overline{UCAS}=\overline{LCAS}$, \overline{RAS} , Address Cycling @ $t_{RC}=\min.$)	KM416C1000L/LL-7	—	100	mA
	KM416C1000L/LL-8	—	90	mA
	KM416C1000L/LL-10	—	80	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{UCAS} or \overline{LCAS} , Address Cycling @ $t_{PC}=\min.$)	KM416C1000L/LL-7	—	100	mA
	KM416C1000L/LL-8	—	90	mA
	KM416C1000L/LL-10	—	80	mA
Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS} \geq V_{CC}-0.2V$)	I_{CC5}	—	300	μA
CAS-Before-RAS Refresh Current* (\overline{RAS} , \overline{UCAS} or \overline{LCAS} Cycling @ $t_{RC}=\min.$)	KM416C1000L/LL-7	—	100	mA
	KM416C1000L/LL-8	—	90	mA
	KM416C1000L/LL-10	—	80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH})= $V_{CC}-0.2V$ Input Low Voltage (V_{IL})= $0.2V$ CAS=CAS Before RAS Cycling or 0.2V D_{IN} =Don't Care $T_{RC}=125\mu S$, $T_{RAS}=T_{RAS\min}-1\mu S$	KM416C1000L	—	500	μA
Self Refresh Current $\overline{RAS}=\overline{CAS}=V_{IL}$ $W=OE=A0-A11$: $V_{CC}=0.2V$ or $0.2V$ $DQ1-16=V_{CC}-0.2V$, $0.2V$ or Open	KM416C1000LL	—	500	μA
Input Leakage Current* (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test =0V)	I_{IL}	-10	10	μA
Output Leakage Current* (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)	I_{OL}	-10	10	μA
Output High Voltage Level ($I_{OH}=-5mA$)	V_{OH}	2.4	—	V
Output Low Voltage Level ($I_{OL}=4.2mA$)	V_{OL}	—	0.4	V

*NOTE: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. In I_{CC4} , Address can be changed maximum once while \overline{UCAS} and $\overline{UCAS}=V_{IH}$.

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CAPACITANCE ($T_A=25^\circ\text{C}$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{11})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}}, \overline{\text{W}}, \overline{\text{OE}}$)	C_{IN2}	—	7	pF
Output Capacitance ($\text{DQ}_1-\text{DQ}_{16}$)	C_{DO}	—	7	pF

AC CHARACTERISTICS ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CC}=5.0\text{V} \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM416C1000L/LL-7		KM416C1000L/LL-8		KM416C1000L/LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{\text{RAS}}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{\text{CAS}}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{\text{CAS}}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	20		20		25		ns	

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AC CHARACTERISTICS ($0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM416C1000L/LL-7		KM416C1000L/LL-8		KM416C1000L/LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to \overline{RAS}	t_{DHR}	55		60		75		ns	6
Refresh period (4096 cycles)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
\overline{CAS} to \overline{W} delay time	t_{CWD}	50		50		60		ns	8
\overline{RAS} to \overline{W} delay time	t_{RWD}	100		110		135		ns	8
Column address to \overline{W} delay time	t_{AWD}	65		70		85		ns	8
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	t_{CSR}	10		10		10		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	t_{CHR}	20		30		30		ns	
\overline{RAS} precharge to \overline{CAS} hold time	t_{RPC}	10		10		10		ns	
\overline{CAS} precharge time (C-B-R counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from \overline{CAS} precharge	t_{CPA}		40		45		55	ns	3
Fast page mode cycle time	t_{FC}	45		50		60		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	100		105		125		ns	
\overline{RAS} pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
\overline{RAS} hold time from \overline{CAS} precharge	t_{RHCP}	45		45		55		ns	
\overline{CAS} precharge time (fast page mode)	t_{CP}	10		10		10		ns	
\overline{RAS} hold time referenced to \overline{OE}	t_{ROH}	20		20		20		ns	
\overline{OE} access time	t_{OEA}		20		20		25	ns	
\overline{OE} to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from \overline{OE}	t_{OEZ}	0	20	0	20	0	25	ns	
\overline{OE} command hold time	t_{OEH}	20		20		25		ns	
\overline{RAS} pulse width (C-B-R self refresh)	t_{RASS}	100		100		100		μ s	19
\overline{RAS} precharge time (C-B-R self refresh)	t_{RPS}	130		150		180		ns	19
\overline{CAS} hold time (C-B-R self refresh)	t_{CHS}	0		0		0		ns	19

KM416C1000L/LL Truth Table

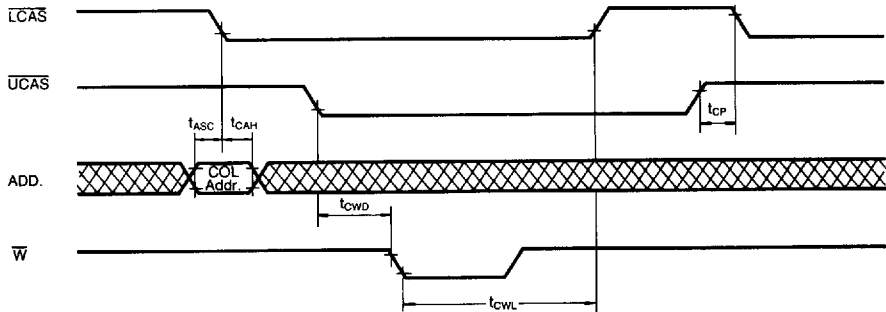
RAS	LCAS	UCAS	\overline{W}	\overline{OE}	DQ ₁₋₈	DQ ₉₋₁₆	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

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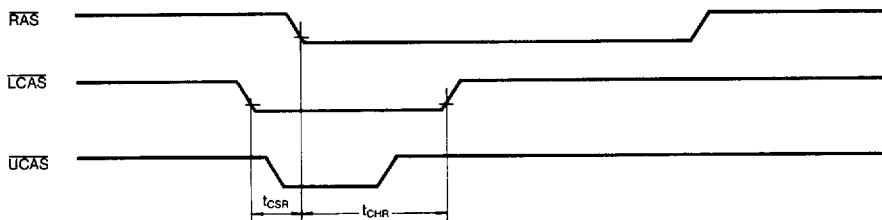
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NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(\min)}$ and $V_{IL(\max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(\min)}$ and $V_{IL(\max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}(\max)}$ limit insures that $t_{\text{RAC}(\max)}$ can be met. $t_{\text{RCD}(\max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}(\max)}$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}(\max)}$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}(\max)}$.
7. $t_{\text{OFF}(\max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}(\min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}(\min)}$, $t_{\text{RWD}} \geq t_{\text{RWD}(\min)}$, $t_{\text{AWD}} \geq t_{\text{AWD}(\min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}(\max)}$ limit insures that $t_{\text{RAC}(\max)}$ can be met. $t_{\text{RAD}(\max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}(\max)}$ limit, then access time is controlled by t_{AA} .
12. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
13. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.



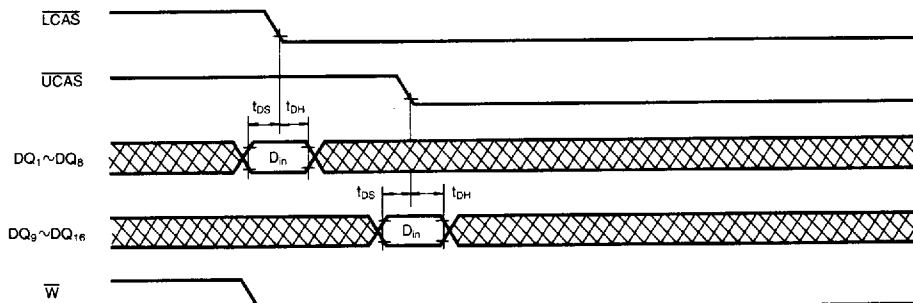
16. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
17. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.



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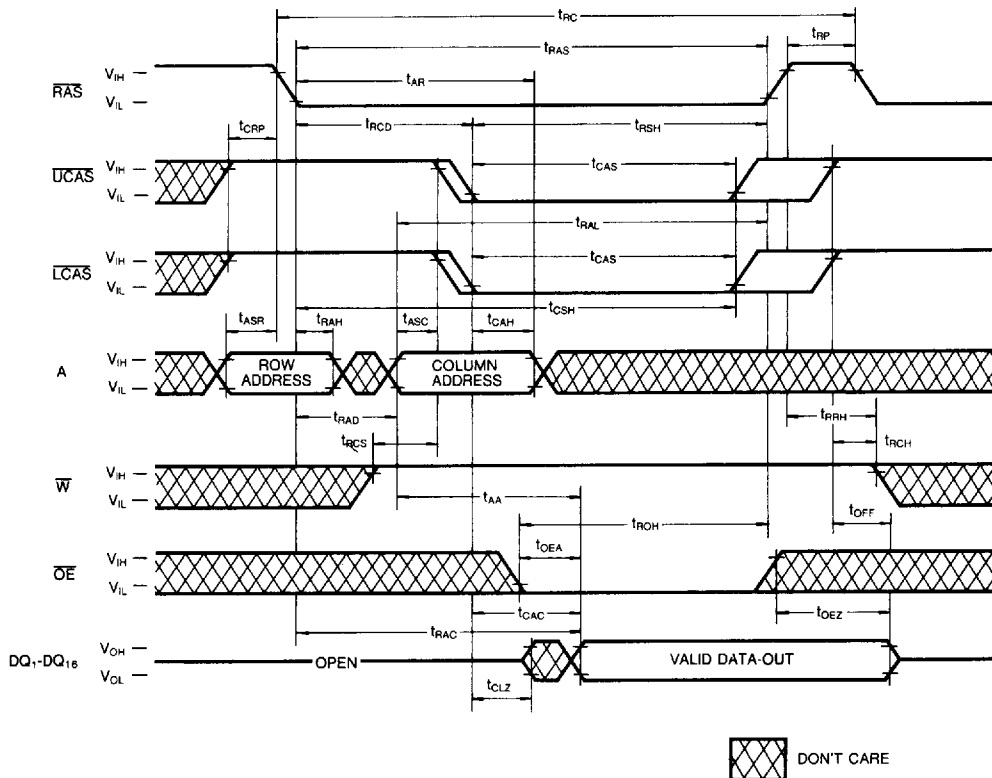
18. t_{DS} , t_{DH} is independently specified for lower byte $D_{in(1\sim 8)}$, upper byte $D_{in(9\sim 16)}$



19. 4096 cycle of Burst Refresh must be executed within 64 ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

WORD READ CYCLE

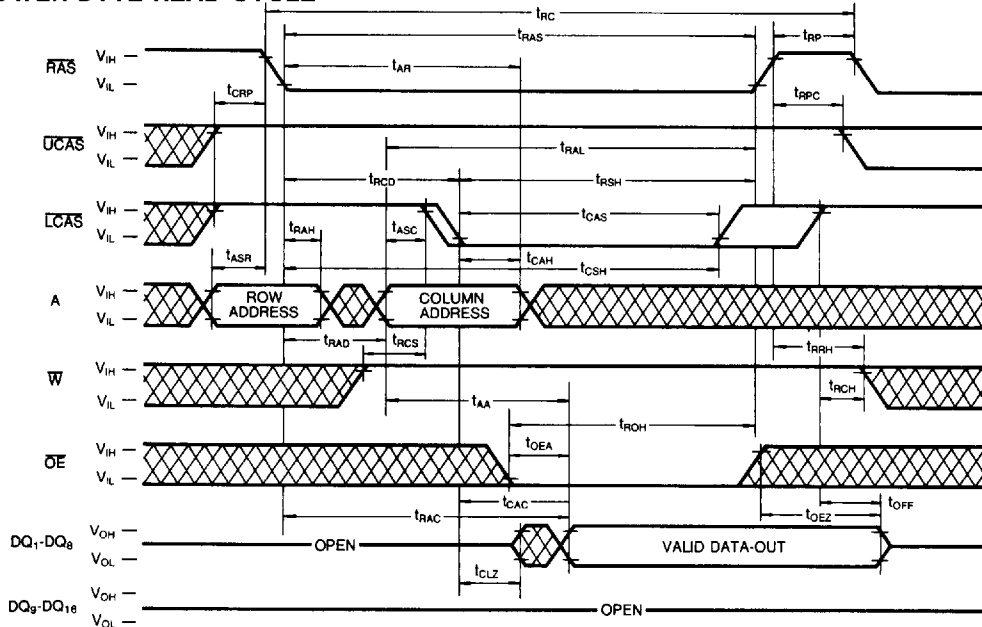


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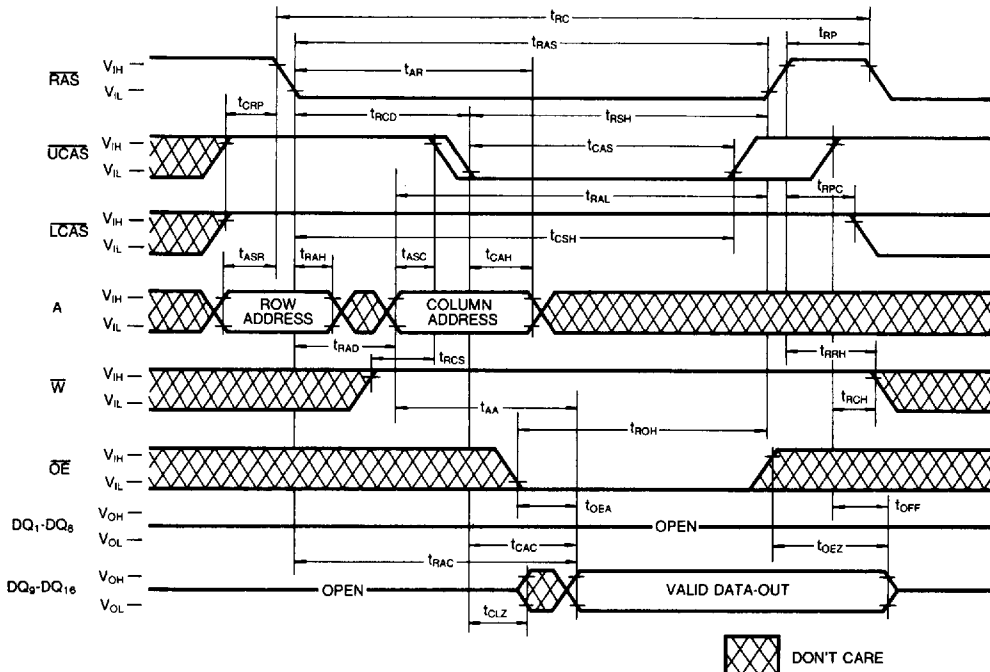
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TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE



UPPER BYTE READ CYCLE

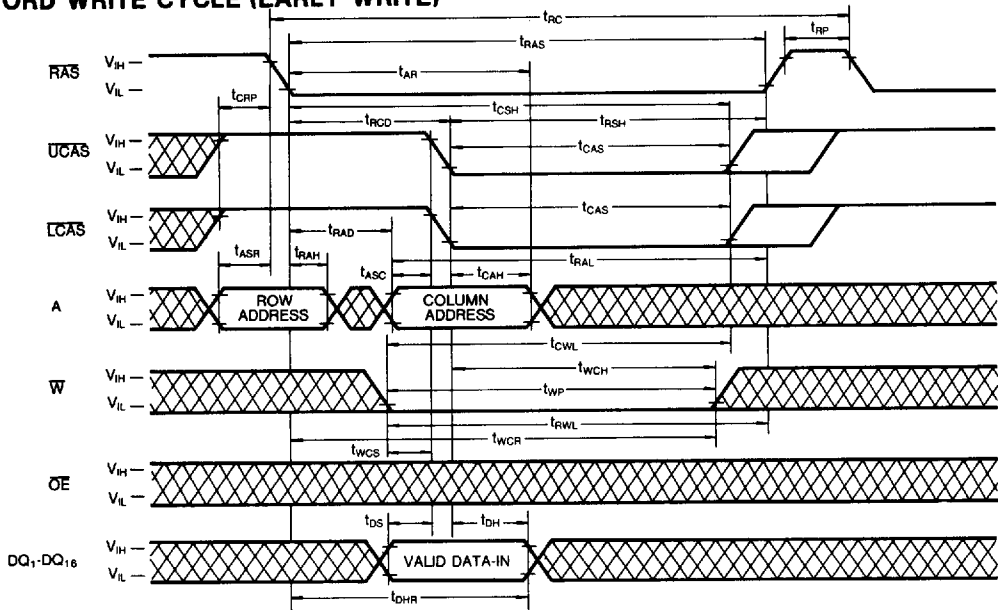


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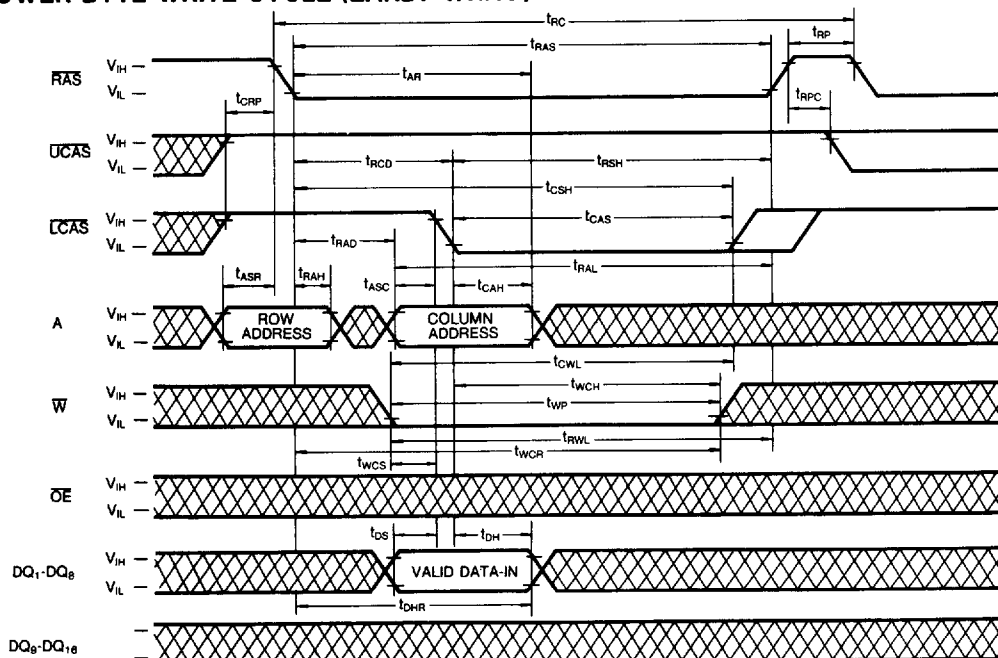
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TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



LOWER BYTE WRITE CYCLE (EARLY WRITE)



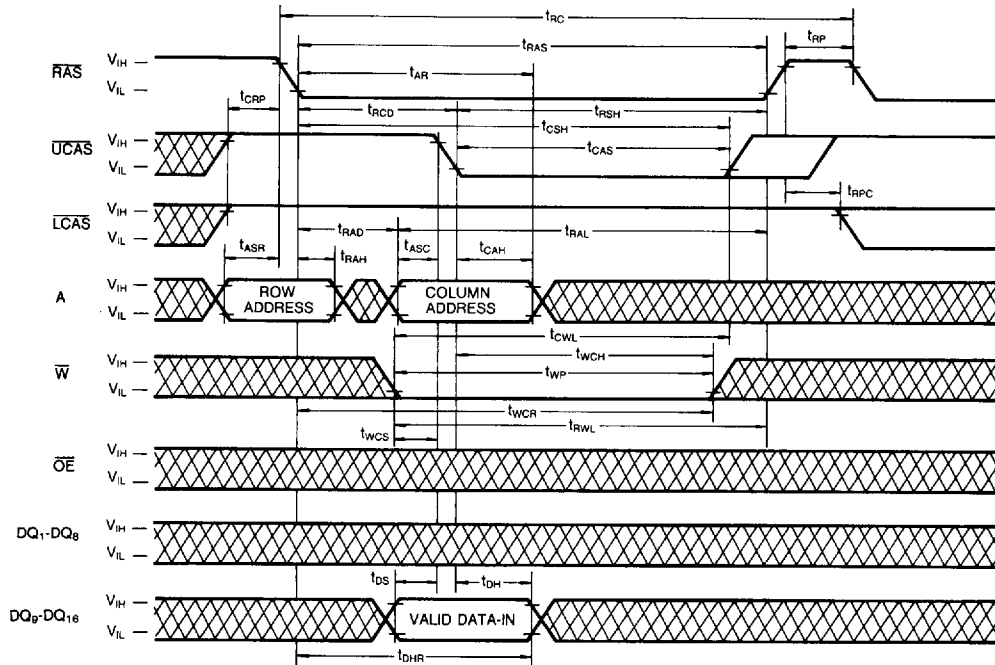
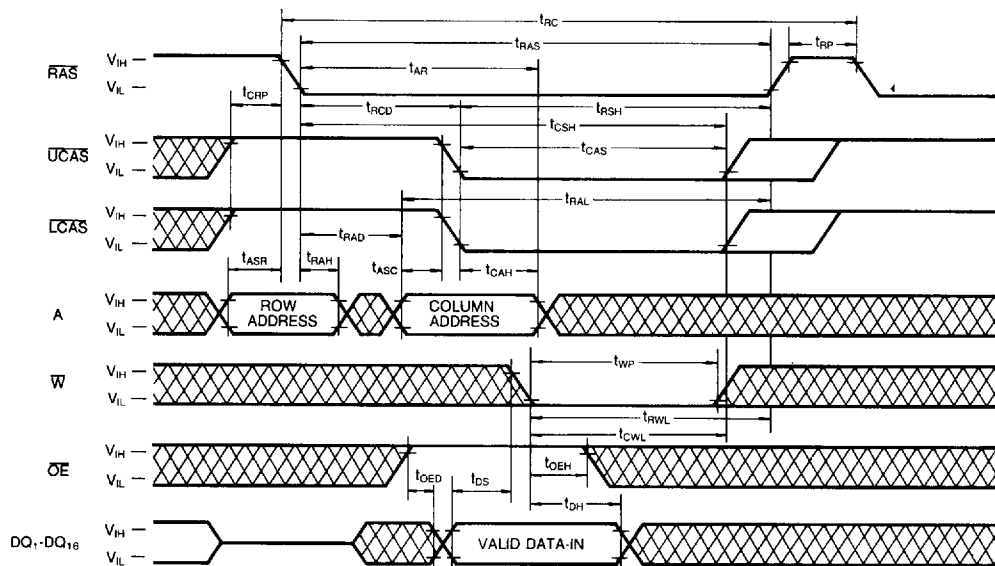
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TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

WORD WRITE CYCLE (\bar{OE} CONTROLLED WRITE)

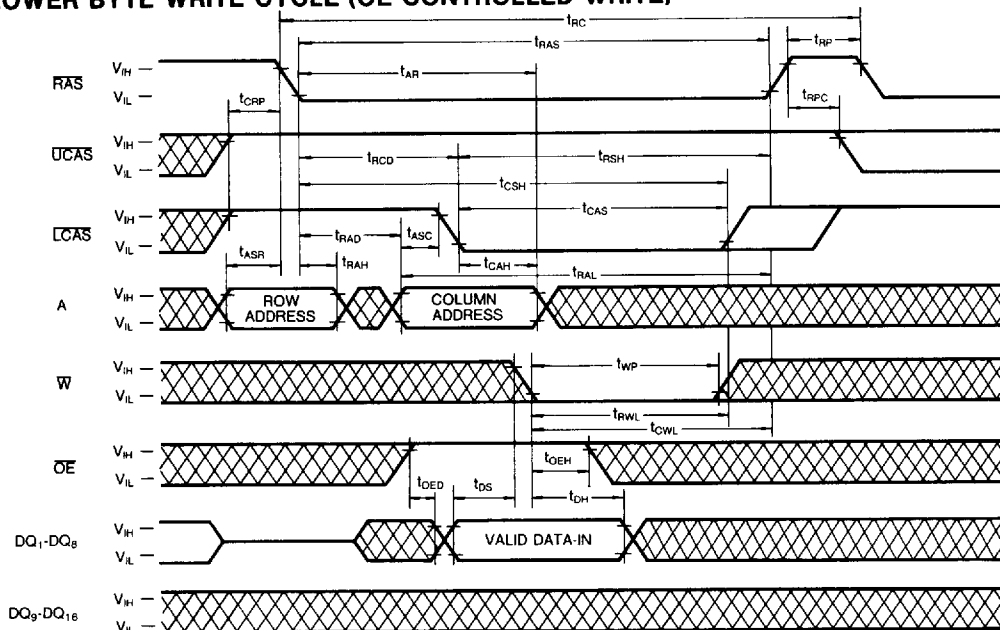
DON'T CARE

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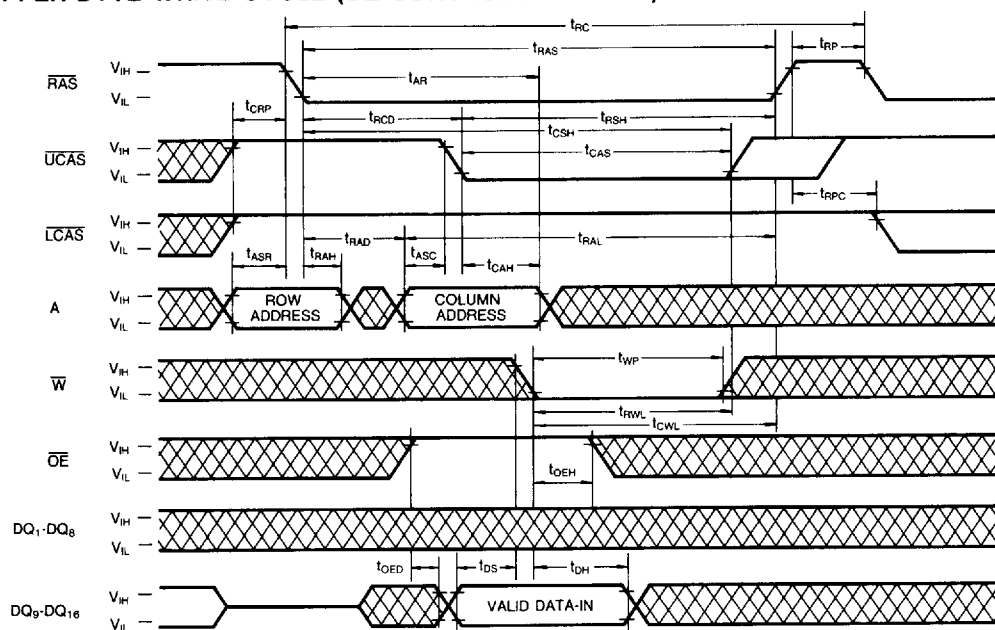
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TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)



UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)



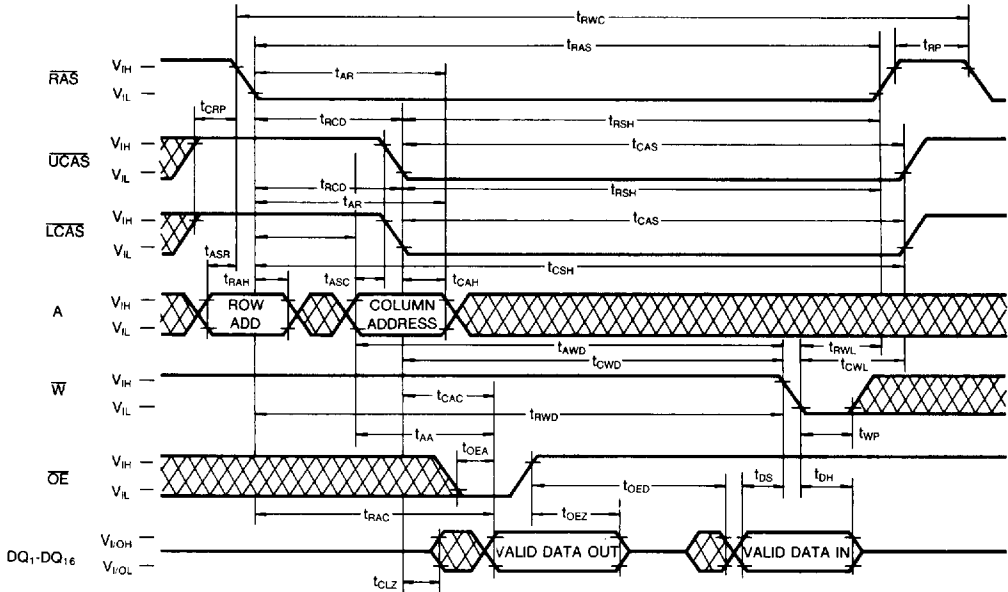
DON'T CARE

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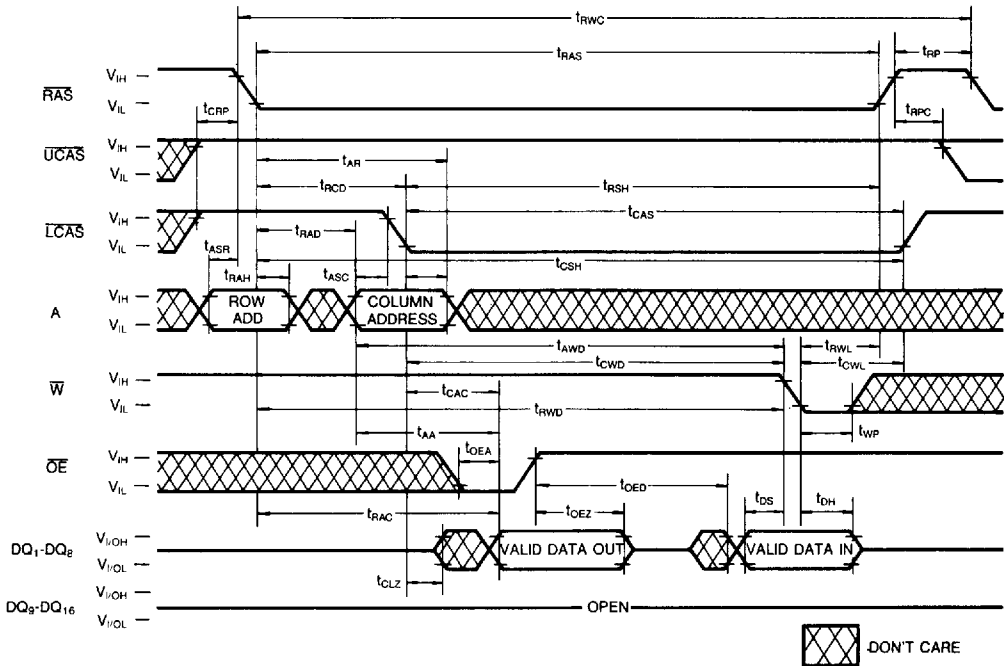
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TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE



READ-MODIFY-LOWER-BYTE-WRITE CYCLE



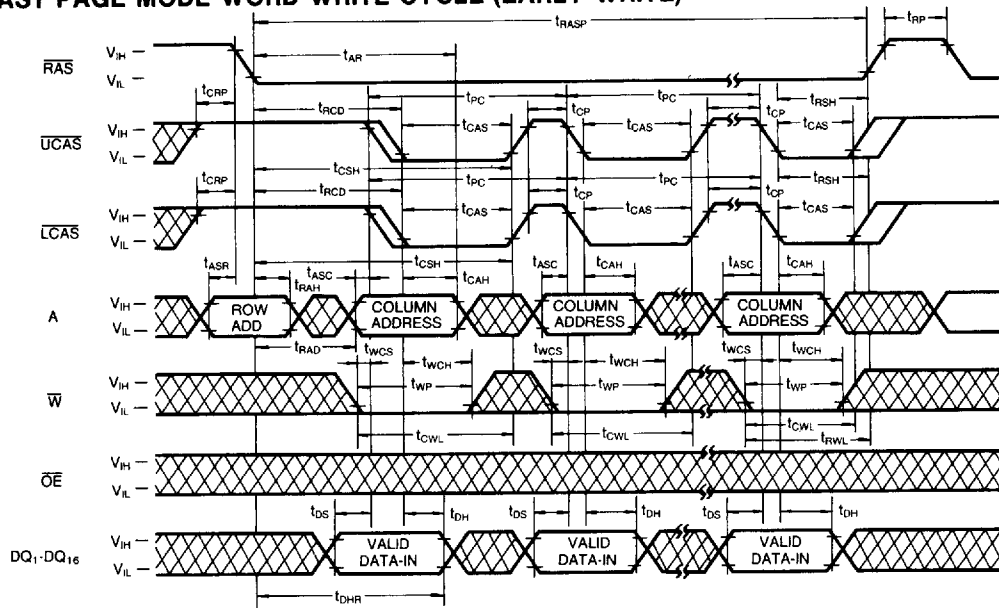
DON'T CARE

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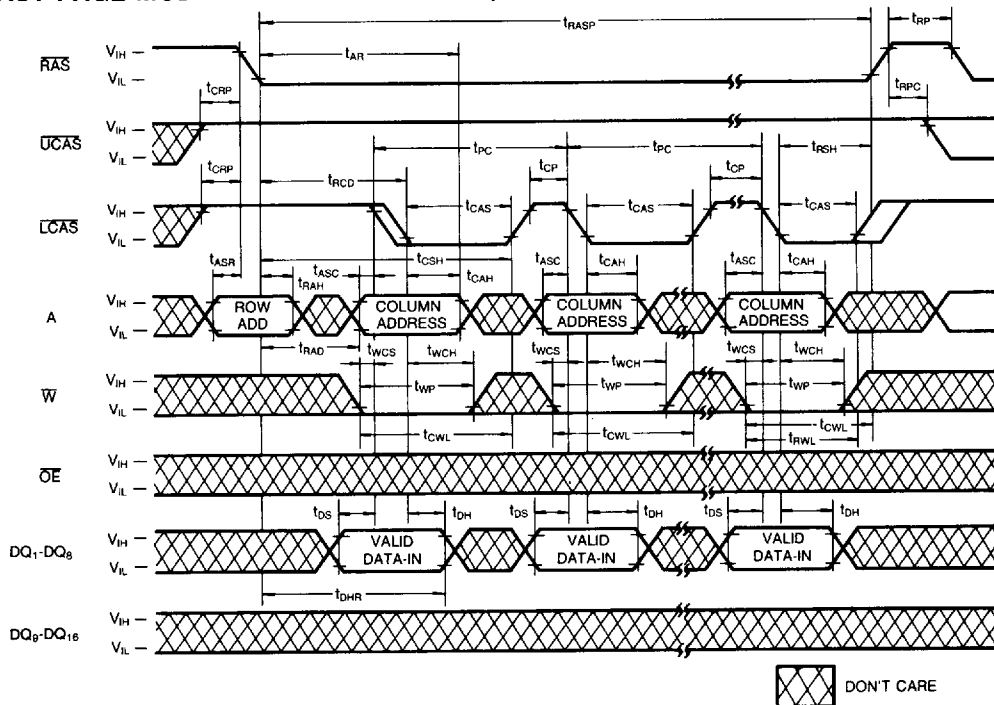
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TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

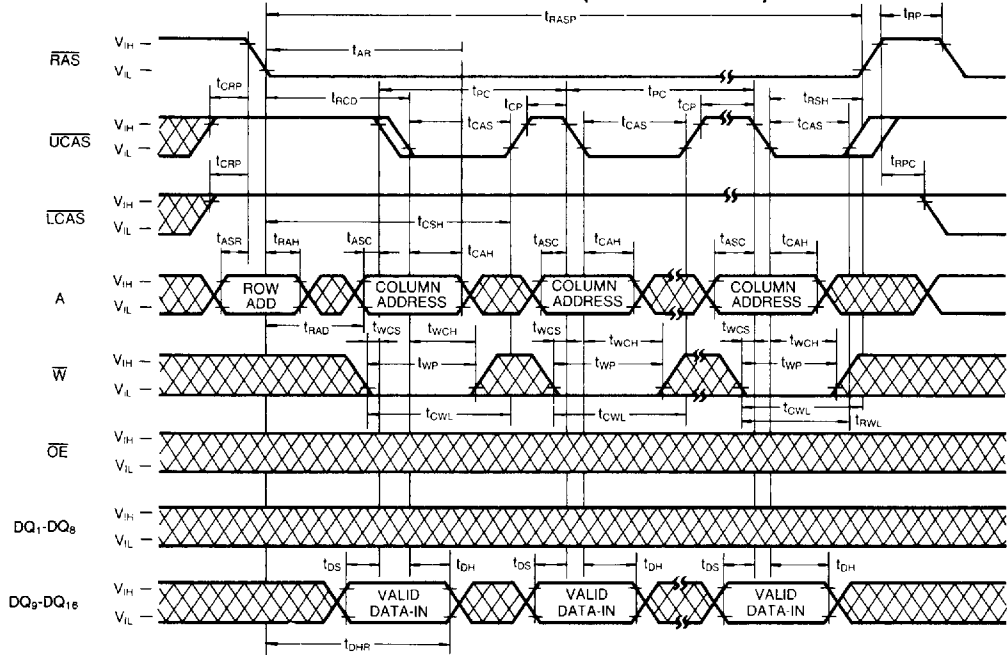


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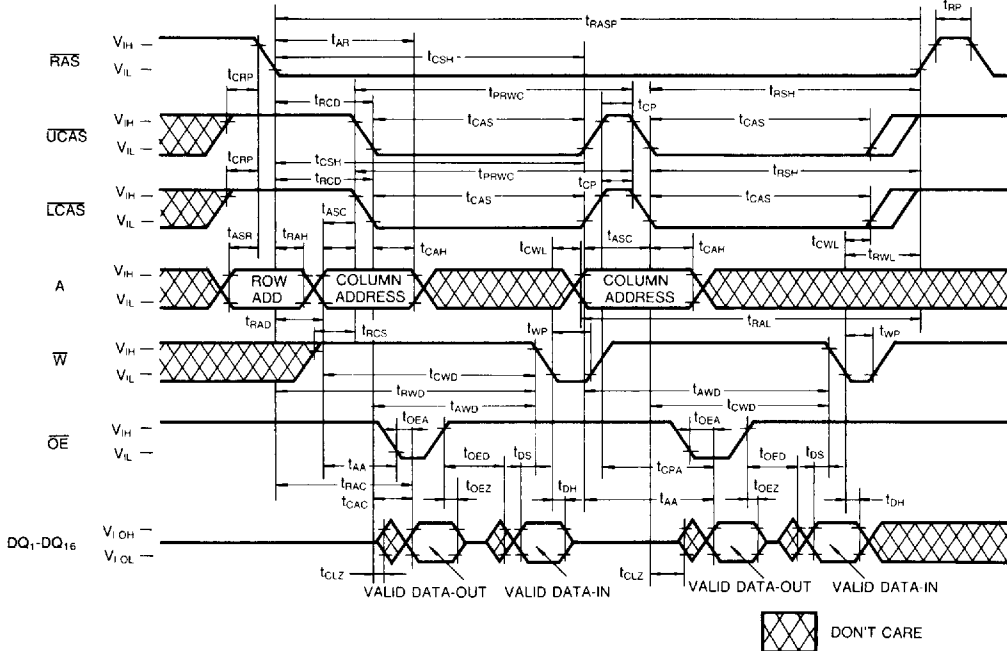
TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



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FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

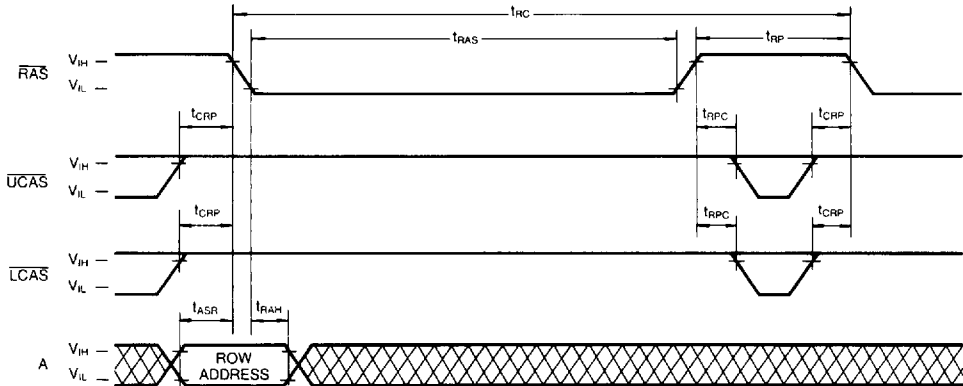
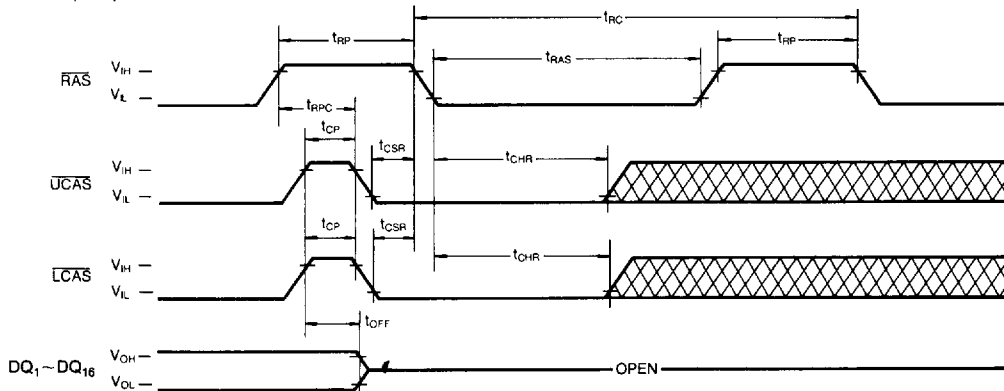
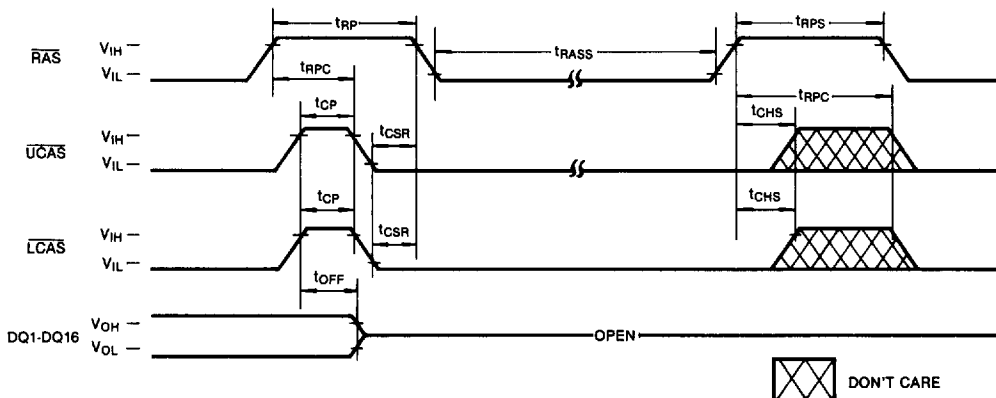


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TIMING DIAGRAMS (Continued)

RAS ONLY REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} = Don't Care \bar{CAS} -BEFORE- \bar{RAS} REFRESH CYCLENOTE: \bar{W} , \bar{OE} , A = Don't Care \bar{CAS} -BEFORE- \bar{RAS} SELF REFRESH CYCLENOTE: \bar{W} , \bar{OE} , A = Don't Care

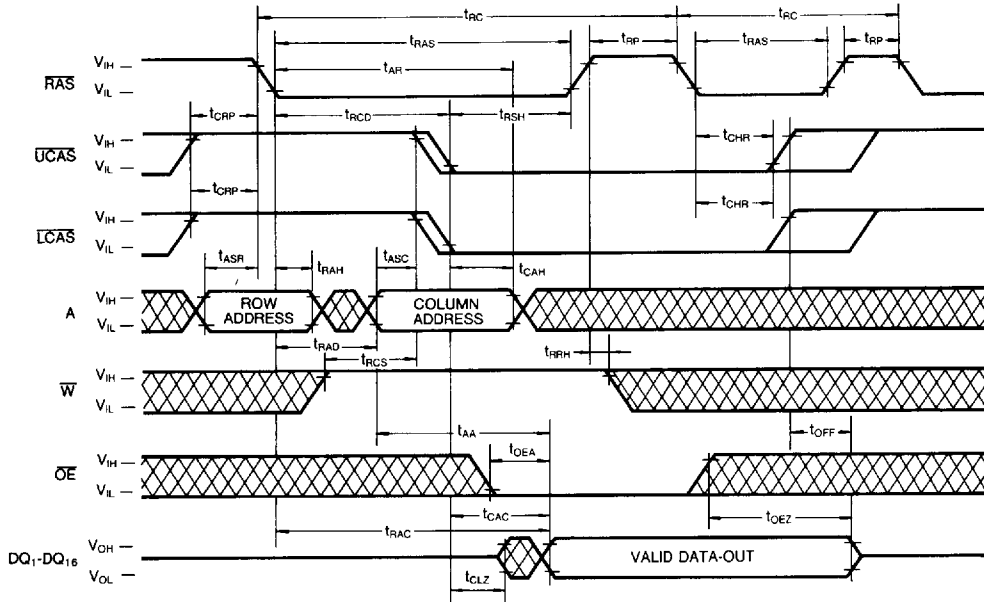
DON'T CARE

KM416C1000L/LL

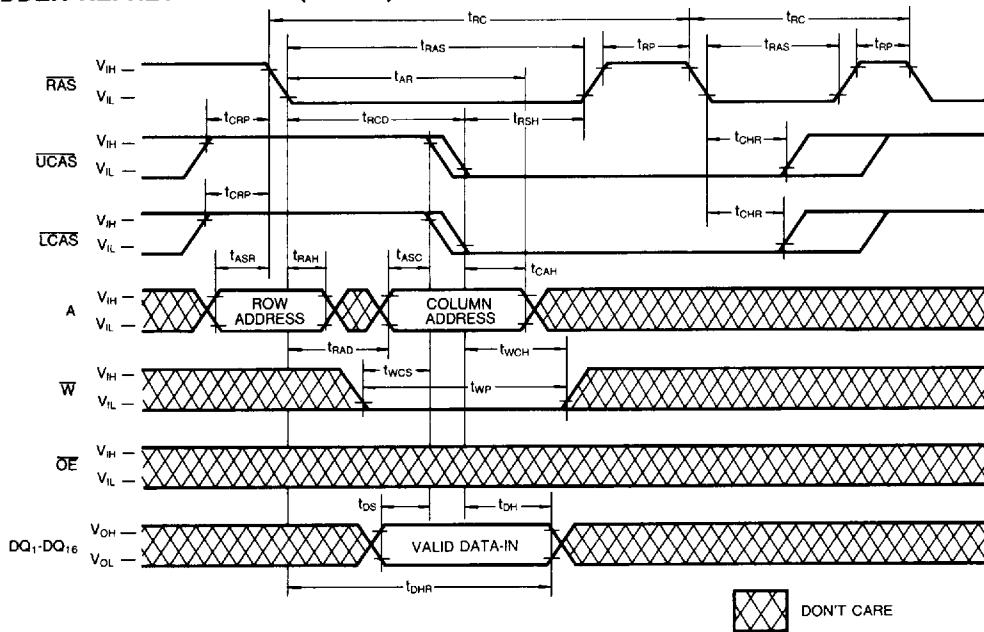
CMOS DRAM

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



KM416C1000L/LL**CMOS DRAM****DEVICE OPERATION****Device Operation**

The KM416C1000L/LL contains 16,777,216 memory locations arranged in 16 groups of 1,048,576 × 1bit each. Twenty address bits are required to address a particular memory location. Since the KM416C1000L/LL has only 12 address input pins, time multiplexed addressing is used to input 12 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{LCAS} , \overline{UCAS}) and the valid row and column address inputs.

Operation of the KM416C1000L/LL begins by strobing in a valid row address with \overline{RAS} while \overline{LCAS} (\overline{UCAS}) remains high. Then the address on the 12 address input pins is changed from a row address to a column address and is strobed in by \overline{LCAS} (\overline{UCAS}). This is the beginning of any KM416C1000L/LL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{LCAS} (\overline{UCAS}) have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the RAS precharge time(t_{RP})requirement.

 \overline{RAS} and \overline{CAS} Timing

The minimum \overline{RAS} and \overline{CAS} pulse widths are specified by $t_{RAS}(\min)$ and $t_{CAS}(\min)$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CAS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM416C1000L/LL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input(\overline{W}) high during a $\overline{RAS}/\overline{XCAS}$ cycle. The access time is normally specified with respect to the falling edge of \overline{RAS} . Additionally the access time also depends on the falling edge of \overline{CAS} and on the valid column address transition. If \overline{XCAS} transitions to a low before $t_{RCD}(\max)$ then the access time to valid data is specified by $t_{RAC}(\min)$. However, if \overline{XCAS} transitions low after $t_{RCD}(\max)$ or if the column address becomes valid after $t_{RAD}(\max)$, access is specified by t_{CAC} or t_{AA} . In order to achieve the minimum access time, $t_{RAC}(\min)$, it is necessary to meet both $t_{RCD}(\max)$ and $t_{RAD}(\max)$.

Write

The KM416C1000L/LL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} , \overline{OE} , \overline{LCAS} and \overline{UCAS} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{XCAS} , whichever is later.

Early Write : An early write cycle is performed by bringing \overline{W} low before \overline{XCAS} . The 16-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the \overline{OE} input.

Read-Modify-Write : In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing \overline{W} low after \overline{CAS} and meeting the data sheet read-modify-write timing requirements. The \overline{OE} input must be low during the time defined by t_{OEa} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the \overline{OE} timing requirements prevents bus contention on the KM416C1000L/LL DQ pins.

Data Output

The KM416C1000L/LL has a three-state output buffers which are controlled by \overline{CAS} and \overline{OE} . Whenever either \overline{CAS} or \overline{OE} is high(V_{IH}), the outputs are in the high impedance(Hi-Z)state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of \overline{CAS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAS} and t_{AA} specify when the valid data will be present at the output. This is true even if a new \overline{RAS} cycle occurs(as in hidden refresh). Each of the KM416C1000L/LL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data : Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State : Early Write, \overline{RAS} -only Refresh, Fast Page Mode Write, \overline{CAS} -before- \overline{RAS} Refresh, \overline{OE} controlled write, \overline{CAS} -only cycle.

Indeterminate Output State : Delayed Write(t_{CWD} or t_{RWD} times are not met)

KM416C1000L/LL**CMOS DRAM****DEVICE OPERATION** (Continued)**Refresh**

The data in the KM416C1000L/LL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) of within 256ms. There are several ways to accomplish this.

RAS-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with \overline{RAS} while \overline{CAS} remains high. This cycle must be repeated for each of the 4096 row address (A_0 - A_{11}).

CAS-before-RAS Refresh: The KM416C1000L/LL has \overline{CAS} -before- \overline{RAS} on-chip refresh capability that eliminates the need for external refresh addresses. If either \overline{LCAS} or \overline{UCAS} in-put is held low for the specified set up time (t_{CSR}) before \overline{RAS} transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next \overline{CAS} -before- \overline{RAS} refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either \overline{LCAS} or \overline{UCAS} input active time and cycling \overline{RAS} . The hidden refresh cycle is actually a \overline{CAS} -before- \overline{RAS} refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh: The self refresh is \overline{CAS} -before- \overline{RAS} refresh to be used for long periods of standby, such as a battery back-up. In normal \overline{CAS} -before- \overline{RAS} condition when \overline{RAS} is held low above 100 μ s an internal timer activates an refresh operation of consecutive row addresses in DRAM. The self refresh mode is exited when either \overline{RAS} or \overline{CAS} goes high (V_{IH}).

Other Refresh Methods: It is also possible to refresh the KM416C1000L/LL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general \overline{RAS} -only or \overline{CAS} -before- \overline{RAS} refresh is the preferred method.

Fast Page Mode

The KM416C1000L/LL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while \overline{RAS} is held low to maintain the row address, \overline{CAS} is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

 \overline{CAS} -before- \overline{RAS} Refresh Counter Test Cycle

A special timing sequence using the \overline{CAS} -before- \overline{RAS} counter test cycle provides a convenient method of verifying the functionality of the \overline{CAS} -before- \overline{RAS} refresh activated circuitry. The cycle begins as a \overline{CAS} -before- \overline{RAS} refresh operation. Then, if \overline{CAS} is asserted high and then low again while \overline{RAS} is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A11 are supplied by on chip refresh counter.

Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM416C1000L/LL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that \overline{RAS} and \overline{CAS} track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200 μ s is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8ms period in which there are no \overline{RAS} cycles. An initialization cycle is any cycle in which \overline{RAS} is cycled.

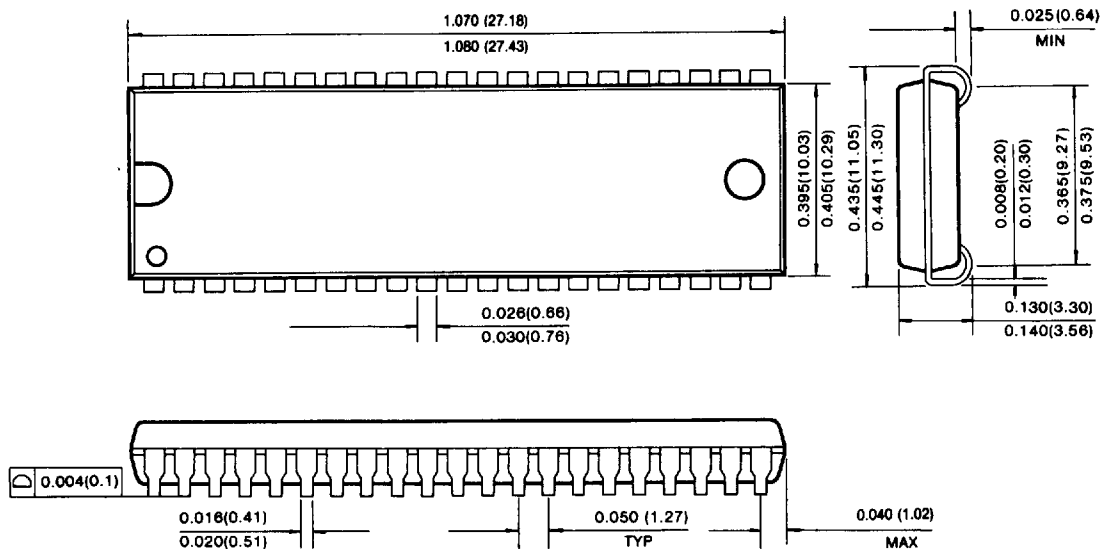
KM416C1000L/LL

CMOS DRAM

PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

