# 512Kx8 Monolithic SRAM, CMOS

## FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
  - Access Times of 70, 85, 100ns
  - Data Retention Function (LP version)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- 32 lead JEDEC Approved Evolutionary Pinout
  - Ceramic Sidebrazed 600 mil DIP (Package 9)
  - Ceramic SOJ (Package 140)
- Single +5V (±10%) Supply Operation

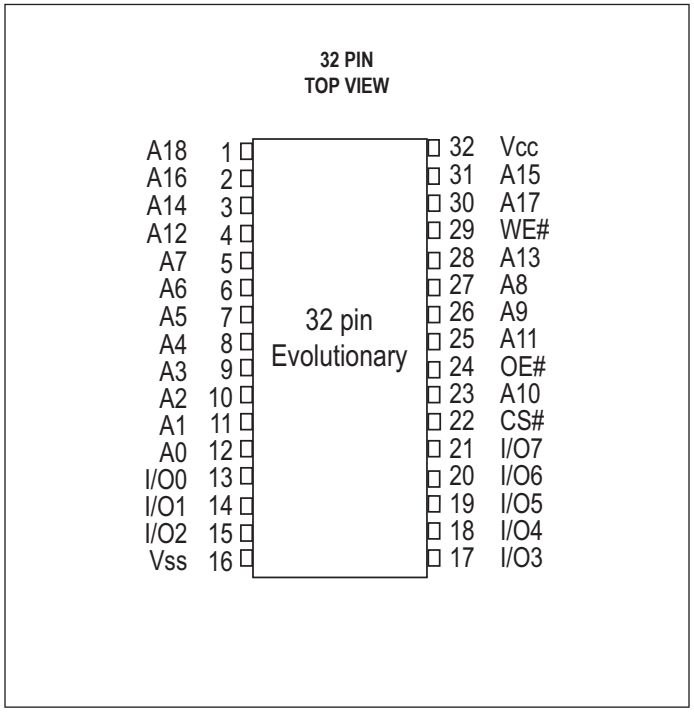
The EDI88512C is a 4 megabit Monolithic CMOS Static RAM.

The 32 pin DIP pinout adheres to the JEDEC evolutionary standard for the four megabit device. Both the DIP and CSOJ packages are pin for pin upgrades for the single chip enable 128K x 8, the EDI88128C. Pins 1 and 30 become the higher order addresses.

A Low Power version with Data Retention (EDI88512LP) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

* This product is subject to change without notice.

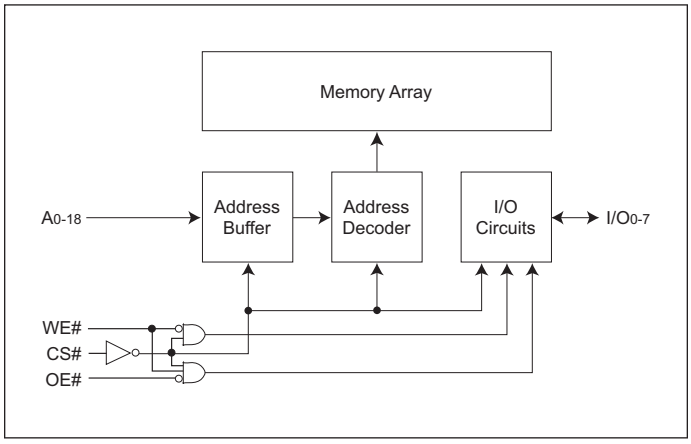
### FIGURE 1 – PIN CONFIGURATION




### PIN DESCRIPTION

| | |
|---|---|
| I/O0-7 | Data Inputs/Outputs |
| A0-18 | Address Inputs |
| WE# | Write Enables |
| CS# | Chip Selects |
| OE# | Output Enable |
| $V_{CC}$ | Power (+5V ±10%) |
| $V_{SS}$ | Ground |
| NC | Not Connected |

### BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Parameter | Value | Unit |
|---|---|---|
| Voltage on any pin relative to Vss | -0.5 to 7.0 | V |
| Operating Temperature $T_A$ (Ambient) | | |
| Commercial | 0 to +70 | °C |
| Industrial | -40 to +85 | °C |
| Military | -55 to +125 | °C |
| Storage Temperature, Plastic | -65 to +150 | °C |
| Power Dissipation | 1 | W |
| Output Current | 20 | mA |
| Junction Temperature, $T_J$ | 175 | °C |

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## TRUTH TABLE

| OE# | CS# | WE# | Mode | Output | Power |
|---|---|---|---|---|---|
| X | H | X | Standby | High Z | $I_{CC2}$, $I_{CC3}$ |
| H | L | H | Output Deselect | High Z | $I_{CC1}$ |
| L | L | H | Read | Data Out | $I_{CC1}$ |
| X | L | L | Write | Data In | $I_{CC1}$ |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ +0.5 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | — | +0.8 | V |

## CAPACITANCE

**$T_A$ = +25°C**

| Parameter | Symbol | Condition | Max | Unit |
|---|---|---|---|---|
| Address Lines | $C_I$ | $V_{IN}$ = Vcc or Vss, f = 1.0MHz | 12 | pF |
| Data Lines | $C_O$ | $V_{OUT}$ = Vcc or Vss, f = 1.0MHz | 14 | pF |

These parameters are sampled, not 100% tested.

## DC CHARACTERISTICS

**$V_{CC}$ = 5V, -55°C ≤ *$T_A$ ≤ +125°C**

| Parameter | Symbol | Conditions | | Min | Typ* | Max | Units |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = 0V to $V_{CC}$ | | — | — | ±10 | µA |
| Output Leakage Current | $I_{LO}$ | $V_{I/O}$ = 0V to $V_{CC}$ | | — | — | ±10 | µA |
| Operating Power Supply Current | $I_{CC1}$ | WE#, CS# = $V_{IL}$, $I_{I/O}$ = 0mA, Min Cycle (70-100ns) | | — | 45 | 75 | mA |
| Standby (TTL) Power Supply Current | $I_{CC2}$ | CS# ≥ $V_{IH}$, $V_{IN}$ ≤ $V_{IL}$, $V_{IN}$ ≥ $V_{IH}$ | | — | 3 | 10 | mA |
| Full Standby Power Supply Current | $I_{CC3}$ | CS# ≥ $V_{CC}$ -0.2V | C | — | — | 5 | mA |
| | | $V_{IN}$ ≥ Vcc -0.2V or $V_{IN}$ ≤ 0.2V | LP | — | — | 2 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 2.1mA | | — | — | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1.0mA | | 2.4 | — | — | V |

NOTE: DC test conditions: $V_{IL}$ = 0.3V, $V_{IH}$ = Vcc -0.3V

## AC TEST CONDITIONS

**Figure 1**

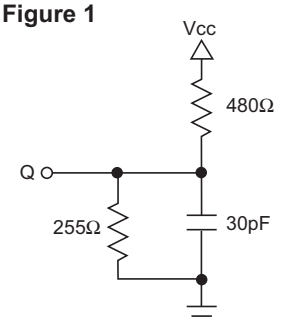
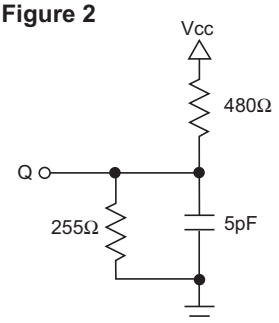



**Figure 2**




| | |
|---|---|
| Input Pulse Levels | $V_{SS}$ to 3.0V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | Figure 1 |

NOTE: For $t_{EHQZ}$, $t_{GHQZ}$ and $t_{WLQZ}$, CL = 5pF Figure 2

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## AC CHARACTERISTICS – READ CYCLE

$V_{CC}$ = 5.0V, Vss = 0V, -55°C ≤ $T_A$ ≤ +125°C

| Parameter | Symbol JEDEC | Symbol Alt. | 70ns Min | 70ns Max | 85ns Min | 85ns Max | 100ns Min | 100ns Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{AVAV}$ | $t_{RC}$ | 70 | | 85 | | 100 | | ns |
| Address Access Time | $t_{AVQV}$ | $t_{AA}$ | | 70 | | 85 | | 100 | ns |
| Chip Enable Access Time | $t_{ELQV}$ | $t_{ACS}$ | | 70 | | 85 | | 100 | ns |
| Chip Enable to Output in Low Z (1) | $t_{ELQX}$ | $t_{CLZ}$ | 10 | | 10 | | 10 | | ns |
| Chip Disable to Output in High Z (1) | $t_{EHQZ}$ | $t_{CHZ}$ | | 25 | | 30 | | 30 | ns |
| Output Hold from Address Change | $t_{AVQX}$ | $t_{OH}$ | 10 | | 10 | | 10 | | ns |
| Output Enable to Output Valid | $t_{GLQV}$ | $t_{OE}$ | | 35 | | 45 | | 50 | ns |
| Output Enable to Output in Low Z (1) | $t_{GLQX}$ | $t_{OLZ}$ | 5 | | 5 | | 5 | | ns |
| Output Disable to Output in High Z(1) | $t_{GHQZ}$ | $t_{OHZ}$ | 0 | 25 | 0 | 30 | 0 | 30 | ns |

1. This parameter is guaranteed by design but not tested.

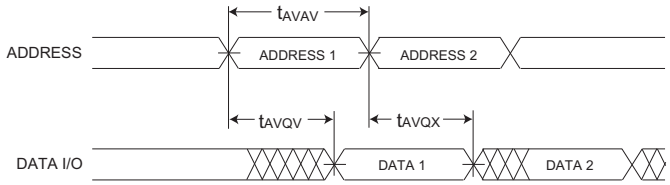
## AC CHARACTERISTICS – WRITE CYCLE

$V_{CC}$ = 5.0V, $V_{SS}$ = 0V, -55°C ≤ $T_A$ ≤ +125°C

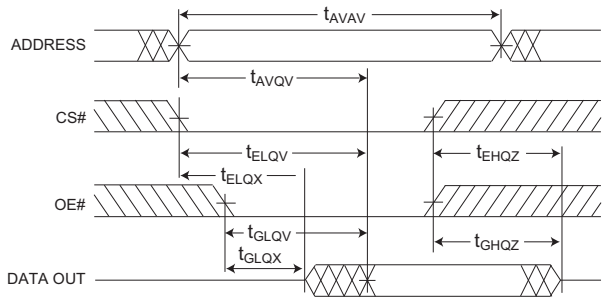
| Parameter | Symbol JEDEC | Symbol Alt. | 70ns Min | 70ns Max | 85ns Min | 85ns Max | 100ns Min | 100ns Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| Write Cycle Time | $t_{AVAV}$ | $t_{WC}$ | 70 | | 85 | | 100 | | ns |
| Chip Enable to End of Write | $t_{ELWH}$<br>$t_{ELEH}$ | $t_{CW}$<br>$t_{CW}$ | 60<br>60 | | 70<br>70 | | 80<br>80 | | ns<br>ns |
| Address Setup Time | $t_{AVWL}$<br>$t_{AVEL}$ | $t_{AS}$<br>$t_{AS}$ | 0<br>0 | | 0<br>0 | | 0<br>0 | | ns<br>ns |
| Address Valid to End of Write | $t_{AVWH}$<br>$t_{AVEH}$ | $t_{AW}$<br>$t_{AW}$ | 65<br>65 | | 70<br>70 | | 80<br>80 | | ns<br>ns |
| Write Pulse Width | $t_{WLWH}$<br>$t_{WLEH}$ | $t_{WP}$<br>$t_{WP}$ | 50<br>50 | | 55<br>55 | | 60<br>60 | | ns<br>ns |
| Write Recovery Time | $t_{WHAX}$<br>$t_{EHAX}$ | $t_{WR}$<br>$t_{WR}$ | 0<br>0 | | 0<br>0 | | 0<br>0 | | ns<br>ns |
| Data Hold Time | $t_{WHDX}$<br>$t_{EHDX}$ | $t_{DH}$<br>$t_{DH}$ | 0<br>0 | | 0<br>0 | | 0<br>0 | | ns<br>ns |
| Write to Output in High Z (1) | $t_{WLQZ}$ | $t_{WHZ}$ | 0 | 25 | 0 | 30 | 0 | 30 | ns |
| Data to Write Time | $t_{DVWH}$<br>$t_{DVEH}$ | $t_{DW}$<br>$t_{DW}$ | 40<br>30 | | 40<br>35 | | 40<br>40 | | ns<br>ns |
| Output Active from End of Write (1) | $t_{WHQX}$ | $t_{WLZ}$ | 5 | | 0 | | 0 | | ns |

1. This parameter is guaranteed by design but not tested.

## FIGURE 2 – TIMING WAVEFORM – READ CYCLE

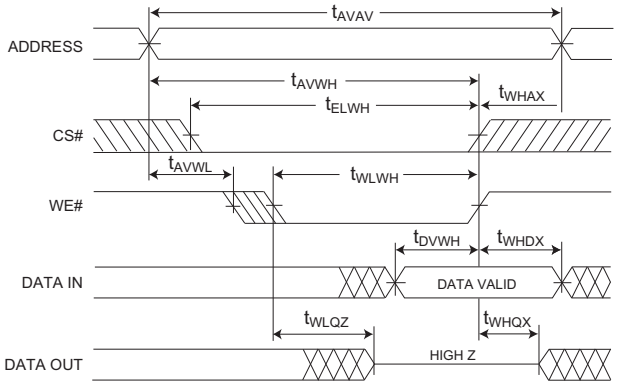



READ CYCLE 1 (WE# HIGH; OE#, CS# LOW)



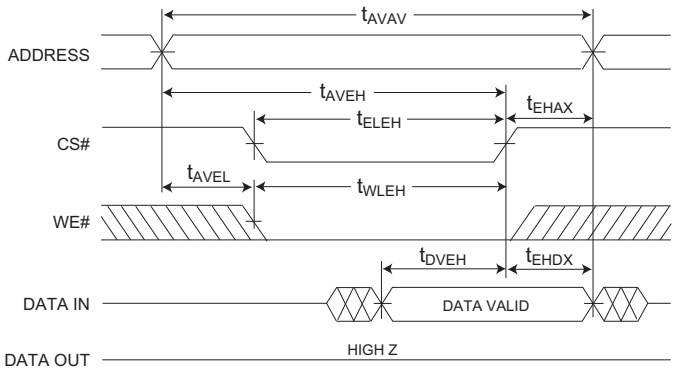

READ CYCLE 2 (WE# HIGH)

## FIGURE 3 – WRITE CYCLE – WE# CONTROLLED




WRITE CYCLE 1, WE# CONTROLLED

## FIGURE 4 – WRITE CYCLE – CS# CONTROLLED



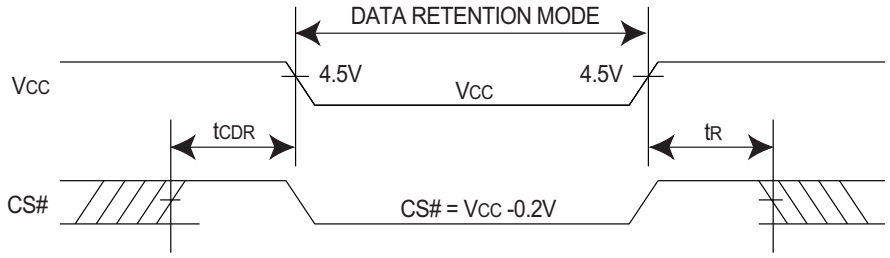

WRITE CYCLE 2, CS# CONTROLLED

## DATA RETENTION CHARACTERISTICS (EDI88512LP ONLY)

**-55°C ≤ $T_A$ ≤ +125°C**

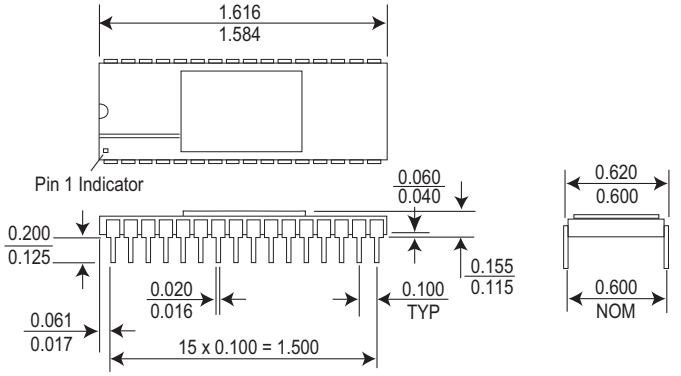
| Characteristic<br>Low Power Version only | Sym | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Data Retention Voltage<br>Data Retention Quiescent Current | $V_{CC}$<br>$I_{CCDR}$ | $V_{CC}$ = 2.0V<br>CS# ≥ $V_{CC}$ -0.2V | 2<br>– | –<br>– | –<br>185 | V<br>µA |
| Chip Disable to Data Retention Time<br>Operation Recovery Time | $t_{CDR}$<br>$T_R$ | $V_{IN}$ ≥ $V_{CC}$ -0.2V<br>or $V_{IN}$ ≤ 0.2V | 0<br>$t_{AVAV}$ | –<br>– | –<br>– | ns<br>ns |

## FIGURE 5 – DATA RETENTION – CS# CONTROLLED



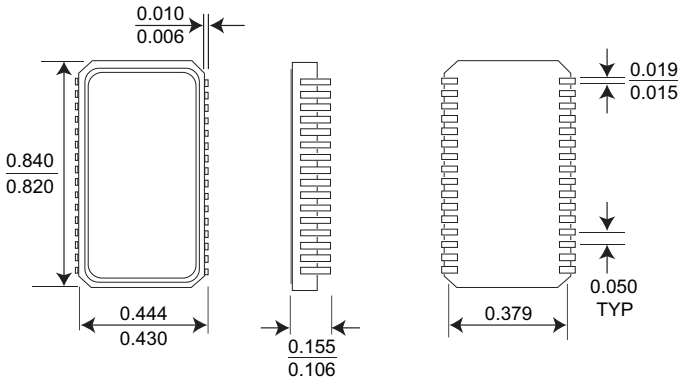

DATA RETENTION, CS# CONTROLLED

## PACKAGE 9: 32 LEAD SIDEBRAZED CERAMIC DIP




ALL DIMENSIONS ARE IN INCHES

## PACKAGE 140: 32 LEAD CERAMIC SOJ




ALL DIMENSIONS ARE IN INCHES

## ORDERING INFORMATION

**EDI 8 8512 C X X X**

**MICROSEMI CORPORATION:**

**SRAM:**

**ORGANIZATION, 512Kx8:**

**TECHNOLOGY:**

C = CMOS Standard Power

LP = Low Power

**ACCESS TIME (ns):**

**PACKAGE TYPE:**

C = 32 lead Sidebrazed DIP, 600 mil (Package 9)

N = 32 lead Ceramic SOJ (Package 140)

**DEVICE GRADE:**

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

## Document Title

512Kx8 Monolithic SRAM, CMOS

## Revision History

| Rev # | History | Release Date | Status |
|---|---|---|---|
| Rev 12 | Changes (Pg. 1-X)<br>12.1 Change document layout from White Electronic Designs to Microsemi<br>12.2 Add document Revision History page | February 2011 | Final |