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ECL Products	

10175
Latch

Quint D-Latch with Common Reset and 2 Wired-OR Common Clock Inputs

FEATURES

- **Typical propagation delay: 2.5ns**
- **Typical supply current ($-I_{EE}$): 78mA**

DESCRIPTION

The 10175 includes five D-latches with common reset and two wired-OR common clock inputs. When the clock is in the High state, any change of the data input does not affect the output state. When the clock is in the Low state, any change of the data input is transferred at the output. The outputs are latched on the positive transition of the clock. The reset input is enabled only when the Clock is High. All unused inputs must be tied Low to V_{IL} or V_{EE}.

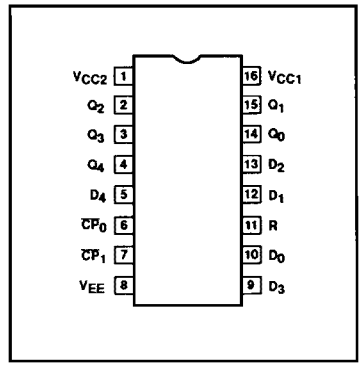
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10175N
16–Pin Ceramic DIP	10175F

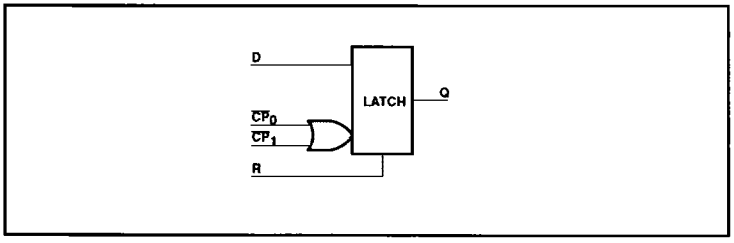
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_4$	Data Inputs
$\overline{CP}_0$, $\overline{CP}_1$	Clock Inputs
R	Reset Input
$Q_0 - Q_4$	Data Outputs

PIN CONFIGURATION

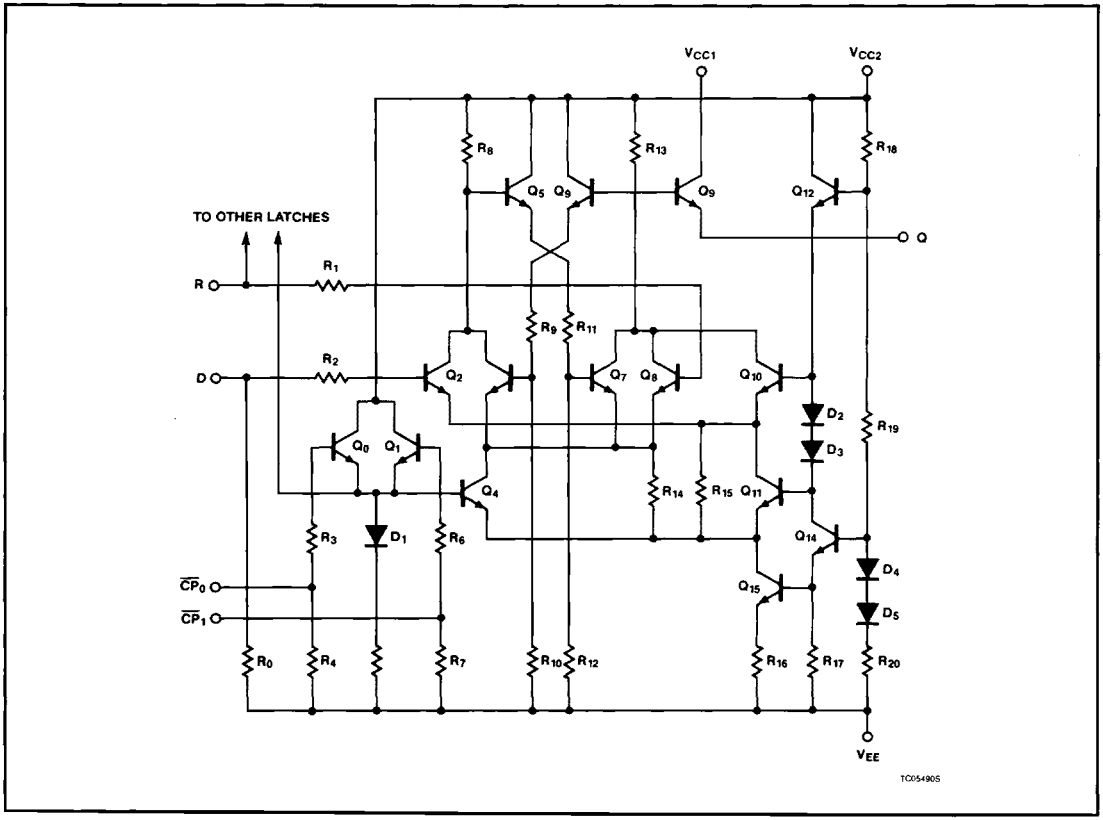


LOGIC DIAGRAM



Latch | 10175

SIMPLIFIED SCHEMATIC



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{CP}_0$	$\overline{CP}_1$	R	D	Q_{n+1}
L	L	X	L	L
L	L	X	H	H
H	X	L	X	Q_n
X	H	L	X	Q_n
H	X	H	X	L
X	H	H	X	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to each D_n	−1060		−890	mV
			$T_A = +25°C$	input, with V_{ILMIN} applied	−960		−810	mV
			$T_A = +85°C$	to all other inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{IHT} to each D_n, one	−1080			mV
			$T_A = +25°C$	at a time, with V_{ILMIN} applied	−980			mV
			$T_A = +85°C$	to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{ILT} to each input, one			−1655	mV
			$T_A = +25°C$	at a time, with V_{ILMIN} applied			−1630	mV
			$T_A = +85°C$	to all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	−1890		−1675	mV
			$T_A = +25°C$		−1850		−1650	mV
			$T_A = +85°C$		−1825		−1615	mV
I_{IH}	High level input current	Other inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under			480	µA
			$T_A = +25°C$	test, one at a time, with V_{ILMIN}			290	µA
			$T_A = +85°C$	applied to all other inputs.			290	µA
		R input	$T_A = -30°C$	Apply V_{IHMAX} to R input			1000	µA
			$T_A = +25°C$	with V_{ILMIN} applied to all			650	µA
			$T_A = +85°C$	other inputs.			650	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				107	mA
			$T_A = +25°C$			78	97	mA
			$T_A = +85°C$				107	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

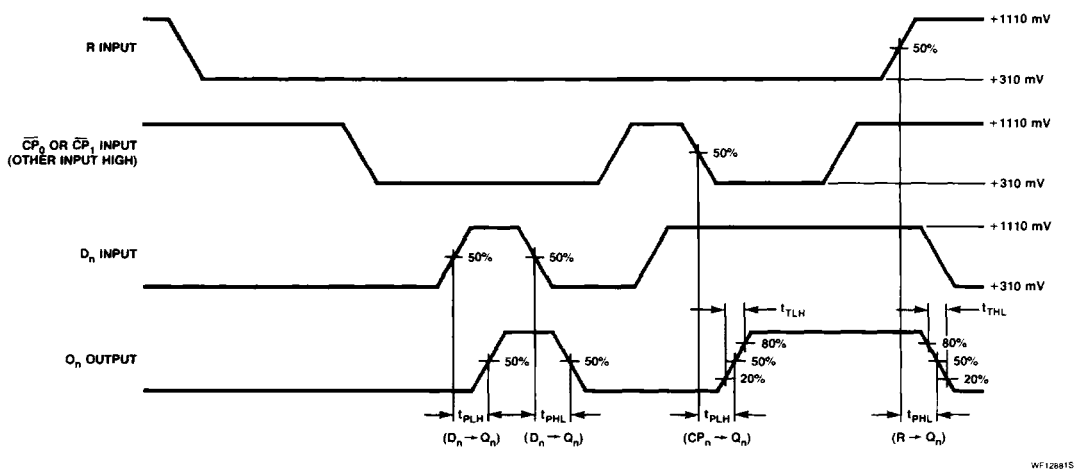
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

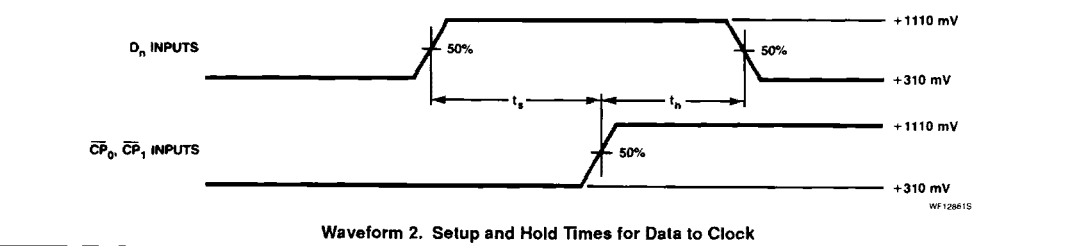
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	3.60 3.60	1.00 1.00	2.50 2.50	3.50 3.50	1.00 1.00	3.60 3.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_n		1.00 1.00	4.70 4.70	1.00 1.00		4.30 4.30	1.00 1.00	4.40 4.40	ns ns
t_{PLH} t_{PHL}	Propagation delay R to Q_n		1.00 1.00	4.00 4.00	1.00 1.00		3.90 3.90	1.00 1.00	4.20 4.20	ns ns
t_s	Setup time D_n to $\overline{CP}_n$	Waveform 2	2.50		2.50			2.50		ns
t_h	Hold time D_n to $\overline{CP}_n$	Waveform 2	1.50		1.50			1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	3.60 3.60	1.10 1.10		3.50 3.50	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times



Waveform 2. Setup and Hold Times for Data to Clock