1.5A DUAL OPEN-DRAIN MOSFET DRIVERS

FEATURES

- **Independently-Programmable Rise and Fall Times**
- **Low Output Impedance .....7Ω Typ**
- **High Speed t_R, t_F .....<30 ns with 1000 pF Load**
- **Short Delay Times**
- **Wide Operating Range .....4.5V to 18V**

APPLICATIONS

- **Motor Controls**
- **Self-Commutating MOSFET Bridge Driver**
- **Driving Bipolar Transistors**
- **Driver for Nonoverlapping Totem Poles**
- **Reach-Up/Reach-Down Driver**

RUGGED

- **Tough CMOS™ Construction**
- **Latch-Up Protected: Will Withstand >500 mA Reverse Current (Either Polarity)**
- **Input Withstands Negative Swings Up to –5V**

GENERAL DESCRIPTION

The TC4404 and TC4405 are CMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the final output totem pole have been left disconnected so individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of individual drain-current-limiting resistors in the pull-up and pull-down sections of the output, thus allowing the user to define the rates of rise and fall desired for a capacitive load, or a reduced output swing if driving a resistive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 ns for a 1000-pF load. There is no upper limit.

For driving MOSFETs in motor-control applications, where slow-on/fast-off operation is desired, these devices are superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because they allow accurate control of turn-on, while maintaining fast turn-off and maximum noise immunity for an OFF device.

When used to drive bipolar transistors, these drivers maintain the high speeds common to other Teledyne drivers and allow insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-off. By proper positioning of the resistor, either npn or pnp transistors can be driven.

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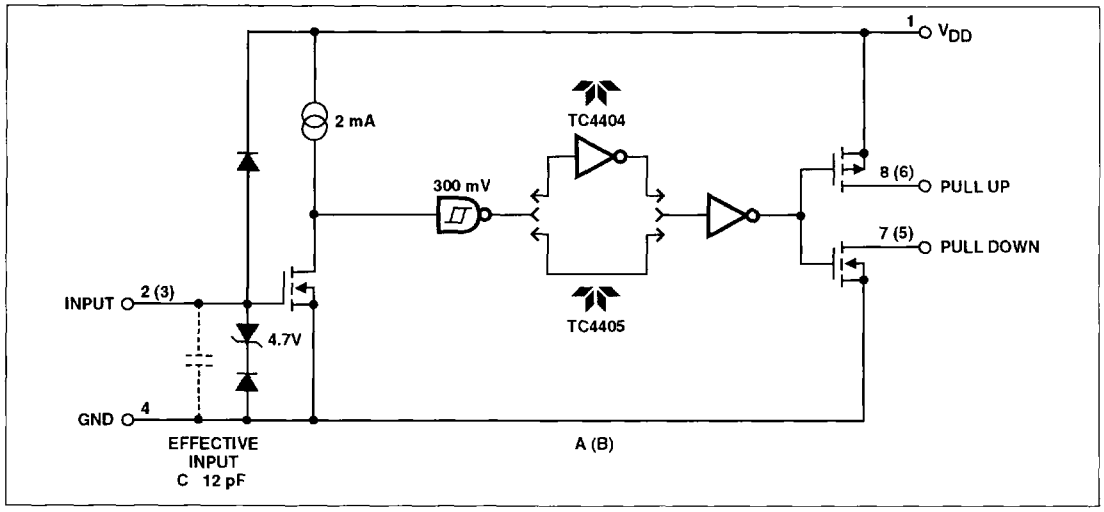
FUNCTIONAL DIAGRAM



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TC4404
TC4405

For driving many loads in low-power regimes, these drivers, because they eliminate shoot-through currents in the output stage, require significantly less power at higher frequencies, and can be helpful in meeting low-power budgets.

Because neither drain in an output is dependent on the other, these devices can also be used as open-drain buffer/drivers where both drains are available in one device, thus minimizing chip count. Unused open drains should be returned to the supply rail their device sources are connected to (pull-downs to ground, pull-ups to V_{DD}), to prevent static damage. In addition, in situations where timing resistors, or other means of limiting crossover currents are used, like drains may be paralleled for greater current carrying capacity.

These devices are built using Teledyne Components' new Tough CMOS process and are capable of giving reliable service in the most demanding electrical environments: they will not latch under any conditions within their power and voltage ratings; they are not subject to damage when up to 5V of noise spiking of either polarity occurs on their ground pin; and they can accept, without damage or logic upset, up to 1/2 amp of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

ORDERING INFORMATION

Part No.	Logic	Package	Temperature Range
TC4404CPA	Inverting	8-Pin PDIP	0°C to +70°C
TC4404COA	Inverting	8-Pin SOIC	0°C to +70°C
TC4405CPA	Noninverting	8-Pin PDIP	0°C to +70°C
TC4405COA	Noninverting	8-Pin SOIC	0°C to +70°C
TC4404EPA	Inverting	8-Pin PDIP	–40°C to +85°C
TC4404EOA	Inverting	8-Pin SOIC	–40°C to +85°C
TC4405EPA	Noninverting	8-Pin PDIP	–40°C to +85°C
TC4405EOA	Noninverting	8-Pin SOIC	–40°C to +85°C
TC4404MJA	Inverting	8-Pin CerDIP	–55°C to +125°C
TC4405MJA	Noninverting	8-Pin CerDIP	–55°C to +125°C

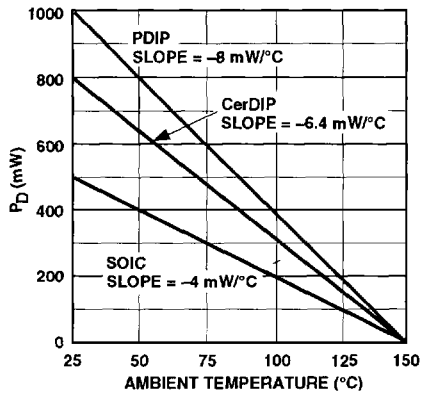
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +22V
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 55°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 45°C/W
- SOIC $R_{\theta J-A}$ ..... 250°C/W
- SOIC $R_{\theta J-C}$ ..... 75°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... –40°C to +85°C
- M Version ..... –55°C to +125°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Package Power Dissipation



POWER-ON OSCILLATION

It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement. A 'quick fix' for most applications which exhibit POWER-ON OSCILLATION problems is to place approximately 10 kΩ in series with the input of the MOSFET driver.

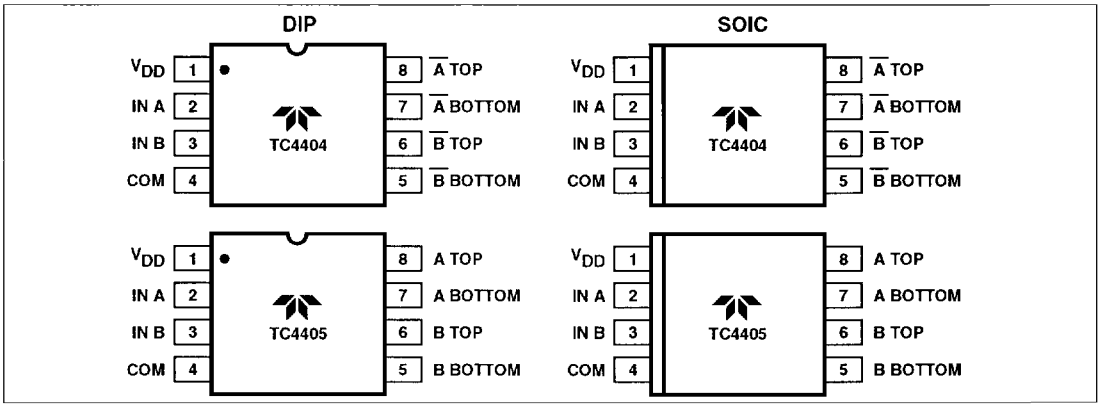
ELECTRICAL CHARACTERISTICS:

Specifications measured at T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	−5V ≤ V_{IN} ≤ V_{DD}	−1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD}−0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V; Any Drain	—	7	10	Ω
I_{PK}	Peak Output Current	Any Drain	—	1.5	—	A
I_{DC}	Continuous Output Current	Any Drain	—	—	100	mA
I_R	Latch-Up Protection	Any Drain Withstand Reverse Current	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1000 pF	—	25	30	ns
t_F	Fall Time	Figure 1, C_L = 1000 pF	—	25	30	ns
t_{D1}	Delay Time	Figure 1, C_L = 1000 pF	—	—	30	ns
t_{D2}	Delay Time	Figure 1, C_L = 1000 pF	—	—	50	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	4.5	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.4	mA

NOTE: 1. Switching times guaranteed by design.

PIN CONFIGURATIONS



TC4404
TC4405

ELECTRICAL CHARACTERISTICS: Specifications measured over operating temperature range with $4.5V \le V_{DD} \le 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$-5V \le V_{IN} \le V_{DD}$	−10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD}−0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V; Any Drain	—	9	12	Ω
I_{PK}	Peak Output Current	Any Drain	—	1.5	—	A
I_{DC}	Continuous Output Current	Any Drain	—	—	100	mA
I_R	Latch-Up Protection	Any Drain Withstand Reverse Current	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1000 pF	—	—	40	ns
t_F	Fall Time	Figure 1, C_L = 1000 pF	—	—	40	ns
t_{D1}	Delay Time	Figure 1, C_L = 1000 pF	—	—	40	ns
t_{D2}	Delay Time	Figure 1, C_L = 1000 pF	—	—	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	8	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.6	mA

NOTE 1. Switching times guaranteed by design.

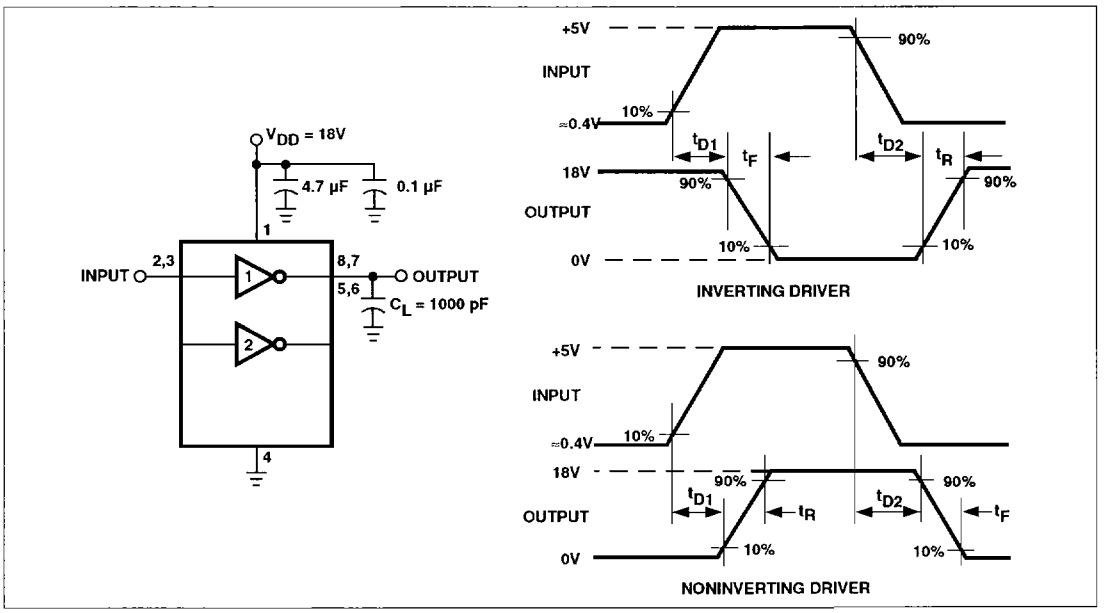


Figure 1 Switching Time Test Circuit

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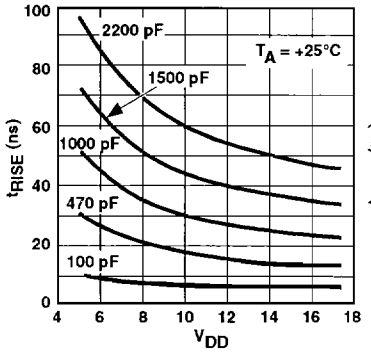
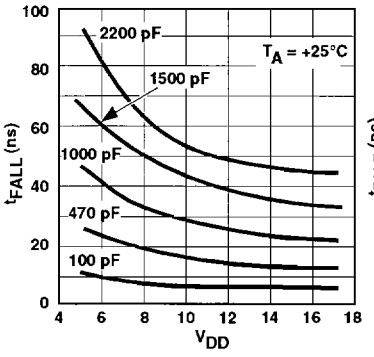
TYPICAL CHARACTERISTICS CURVES

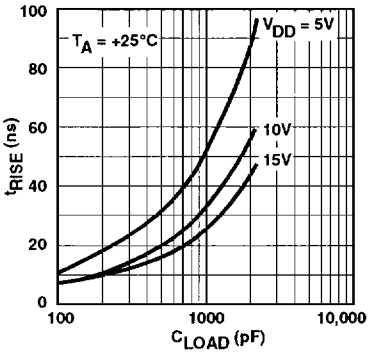
Rise Time vs. Supply Voltage



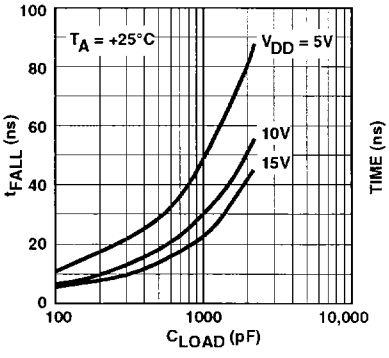
Fall Time vs. Supply Voltage



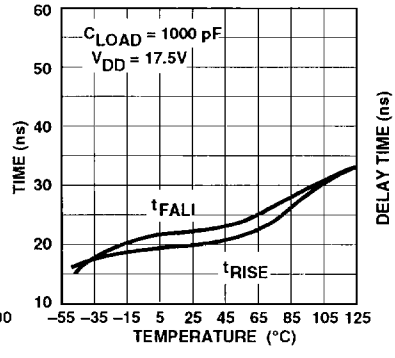
Rise TIme vs. Capacitive Load



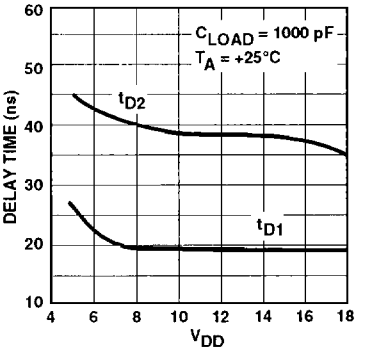
Fall Time vs. Capacitive Load



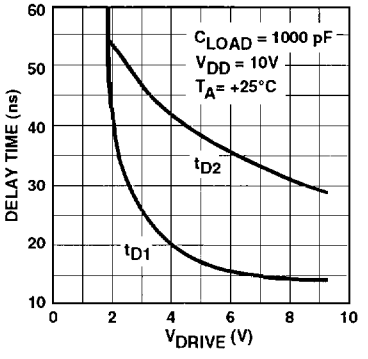
Rise and Fall Times vs. Temperature



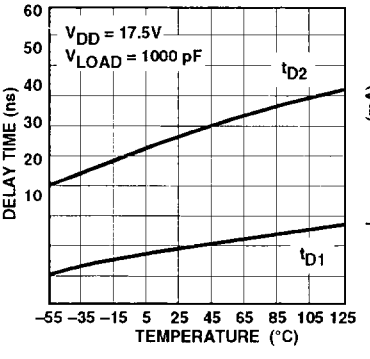
Propagation Delay vs. Supply Voltage



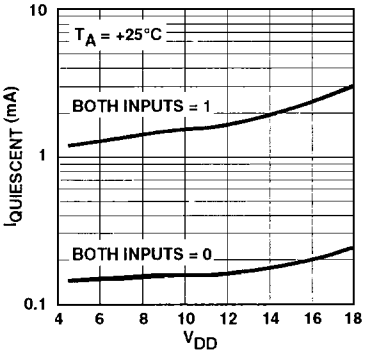
Effect of Input Amplitude on Delay Time



Propagation Delay Time vs. Temperature

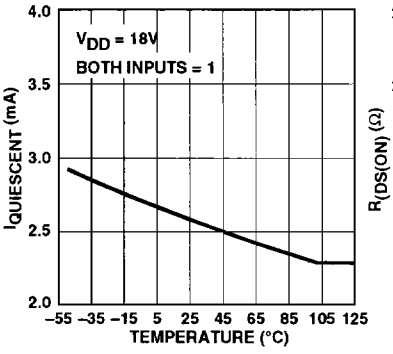


Quiescent Supply Current vs. Voltage

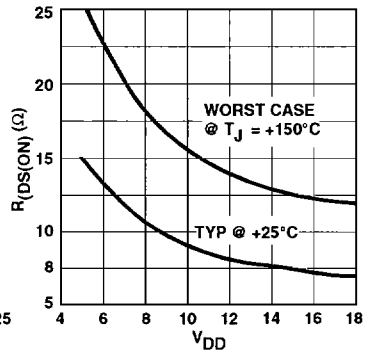


TYPICAL CHARACTERISTICS CURVES (Cont.)

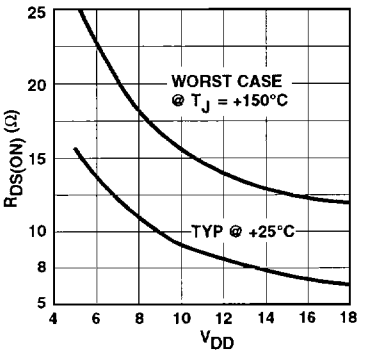
Quiescent Supply Current vs. Temperature



Pull-Up Output Resistance

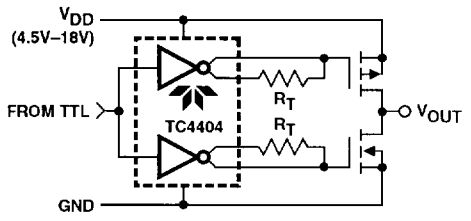


Pull-Down Output Resistance

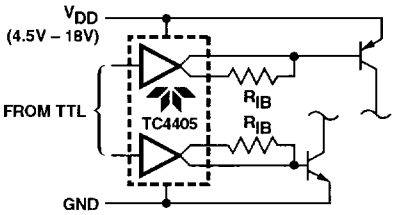


TYPICAL APPLICATIONS

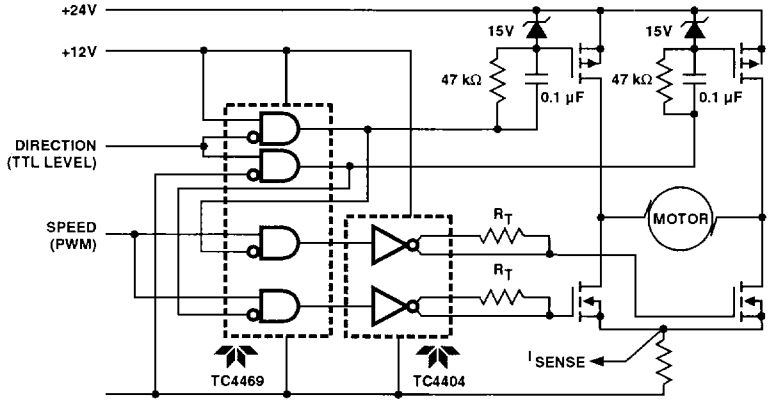
Zero Crossover Current Totem-Pole Switch



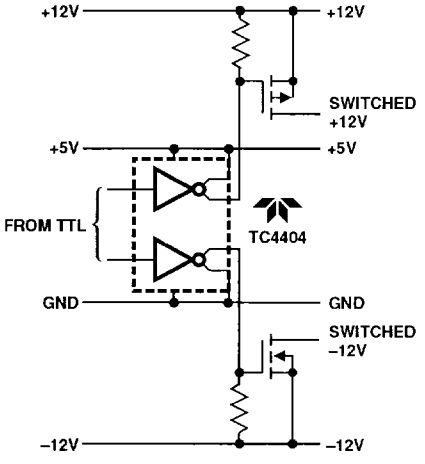
Driving Bipolar Transistors



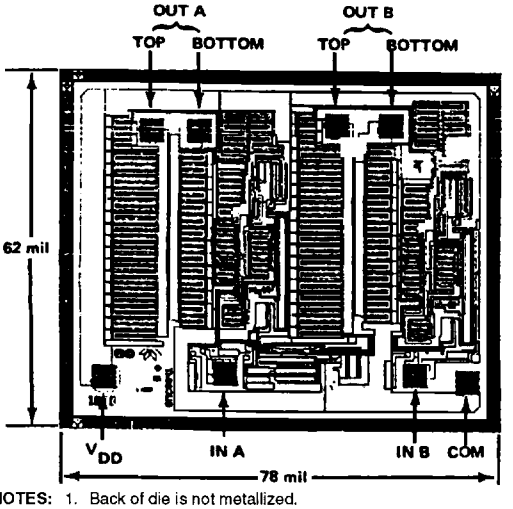
Servo Motor Control



Reach-Up and Reach-Down Driving



BONDING DIAGRAM



NOTES: 1. Back of die is not metallized.
2. Back of die is common to V_{DD}.

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