FAIRCHILD
A Schlumberger Company

F9470 Communication and Console Controller

Microprocessor Product

Description

The Fairchild F9470 Communication and Console Controller is an LSI MOS device that provides the Fairchild F9445 16-bit I^3L® microprocessor with virtual console control and programmed serial I/O via a pair of asynchronous communication ports.

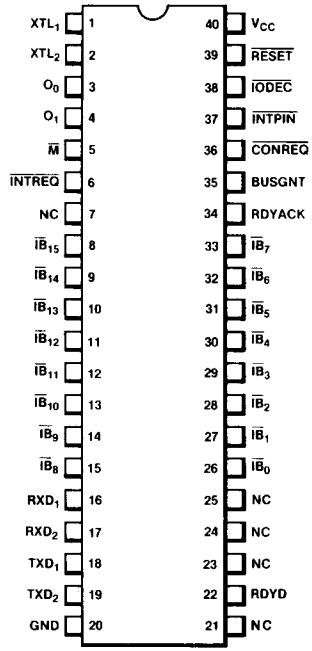
The F9470 provides a variety of useful console functions, including examine and deposit to memory and accumulators, jump to a specified location, and trace the F9445 instruction execution.

The F9470 operates in two modes: console control and I/O service. In the console mode, all communication with the F9445 is controlled by the F9470, which interprets user commands, requests the appropriate information from the F9445, and then outputs it to the operator's terminal.

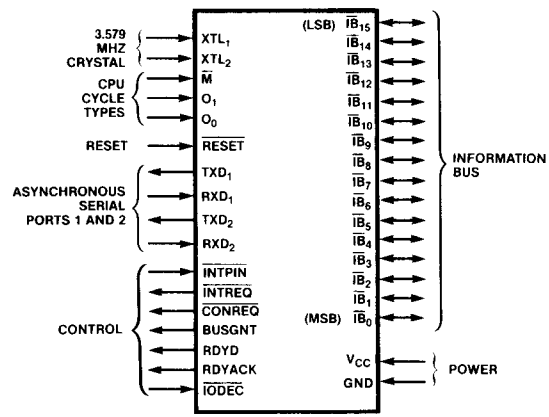
In the I/O service mode, the F9470 acts as a serial I/O controller, interfacing the serial I/O devices to the F9445 through device codes 10-13 and 77. The console commands are not available while in the I/O service mode; all I/O in this mode is programmed through the F9445.

- **Accesses Microprocessor Internal Registers**
- **Two Asynchronous Serial Ports**
- **Allows CRT Terminal to Operate as a Console for an F9445 System**
- **40-Pin DIP Requiring Single +5 V Power Supply**
- **NMOS Technology**

Connection Diagram



Signal Functions



Serial I/O

The F9470 has two asynchronous serial input/output ports. These ports can operate at 110, 300, 1200, 1800, or 2400 baud; port 1 can also operate at 4800 baud (refer to table 1 for baud rate selection codes and restrictions). The baud rate of both ports must be initialized through port 1. The baud rate of port 1 is set by typing a carriage return, <RETURN>, which should be the first key entered after power-up or after issuing the reset baud rate (S) command.

If the baud rate selected for port 1 is 4800, port 2 is disabled and the console mode is entered. If the baud rate of port 1 is 110, the port 2 baud rate is set to 110 and the console mode is entered. If the baud rate of port 1 is between 300 and 2400, the F9470 displays the prompt

```
PEP
+
```

indicating that the baud rate code for port 2 must be entered by the user. These codes are shown in table 1.

The baud rate of port 2 must be less than or equal to the baud rate of port 1, and certain combinations are not allowed (as indicated in the table). If the baud rate code entered for port 2 is incorrect, the F9470 again displays the PEP + prompt.

Console Mode Operation

Once the baud rates have been set, the F9470 enters the console mode (CM), as indicated by a * prompt. In the CM, the F9470 executes the eight console mode commands described in table 2. In response to the A, C, and E interrogative commands, the F9470 requests a console operation from the F9445. The F9445 executes that operation under the control of the F9470 and returns a result to the F9470, if appropriate. Leading octal operands are required with C and E commands. (Execution of interrogative commands halts the F9445.)

The J and R commands cause the F9445 to start program execution at a specified memory location. The J command transfers the F9470 from the CM to the I/O service mode (IOSM), while the R command leaves the F9470 in the CM. The J command causes the F9470 to transfer to the IOSM without affecting F9445 status.

The T command single-steps the F9445 under control of the F9470, and displays the CPU registers after each instruction. This command halts the F9445.

While executing the R and T commands, the F9470 does not respond to I/O instructions from the F9445; all I/O read operations (including tests of device flags) return a zero.

Table 1 Baud Rate Selections and Restrictions for Serial I/O

Baud Rate Codes for Port 2

Code	Baud Rate Selected
0	Disabled
1	110
2	300
3	1200
4	1800
5	2400

Baud Rate Options

Port 1 Baud Rates	Valid Baud Rates for Port 2					
	None	110	300	1200	1800	2400
110		x				
300	x		x			
1200	x		x	x		
1800	x		x		x	
2400	x	x	x	x		x
4800	x					

110 baud automatically sets port 2 to 110
4800 baud automatically disables port 2

Table 2 F9470 Console Mode Commands and Active Keys

Command	Function	Description
		COMMANDS
A	Display Accumulators	Displays in octal the following registers: PC, AC0, AC1, AC2, AC3, SP, and FP.
n,vC	Change Accumulator	Deposits octal value v into register n, where n is n: 0 1 2 3 4 5 Corresponding Register: AC0 AC1 AC2 AC3 SP FP
x:v	Deposit Memory	Deposits octal value v into memory location x.
xE	Examine Memory	Opens and displays the contents of memory location x, allowing octal numbers to be entered. Memory locations may be closed by: <RETURN> which opens the next memory location ^ (caret) which opens the previous memory location <ESC> which returns to the monitor
xJ	Jump	Loads F9445 PC with x, starts program execution, and transfers to the IOSM. When x = 0, transfers to the IOSM, and does not affect F9445 status.
xR	Run	Same as Jump, except that F9470 remains in the CM. When x = 0, transfers to the IOSM, and does not affect F9445 status.
S	Set Baud Rate	Resets F9470. The <RETURN> following S initialized the baud rate of port 1.
nT	Trace	Traces n octal steps of F9445 program execution, displaying CPU registers after each instruction, in the form: Instruction Address Instruction AC0 AC1 AC2 AC3 SP FP Before tracing a program, set the program counter to the appropriate location, using the xE command. Trace defaults to single-step, if n is omitted.
		ACTIVE KEYS
BACKSPACE		Deletes the previously-typed character.
BREAK		Transfers the F9470 from the IOSM to the CM. Does not affect F9445 program execution except that the F9445 I/O instructions are no longer interpreted by the F9470.

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I/O Service Mode Operation

In the I/O service mode, the F9470 acts as a serial I/O controller, interfacing two serial I/O ports to the F9445 using device codes 10 through 13. Executing the J command changes the F9470 from the CM to the IOSM and causes the F9445 to start program execution.

In the IOSM, the F9470 communication format is 1 start bit, 8 data bits, and 2 stop bits. Any parity bit should be set to 1. Table 3 lists the F9445 instruction that the F9470 recognizes when in the IOSM. These commands are a subset of the F9445 instructions described in the F9445 data sheet. When in the I/O service mode, the F9470 optionally responds to the device code 77 control instructions (defined in table 4). These device codes (10, 11, 12, 13, and 77) are octal values of the six least significant instruction bits (refer to table 5).

Pressing the BREAK key at any time transfers the F9470 from the IOSM to the CM. The BREAK does not affect the F9445 program execution; therefore, execution continues until a console command is executed. The F9470 does not interpret F9445 I/O commands after the BREAK is pressed. Because the execution speeds of the F9445 and the F9470 differ, certain programming considerations must be made when using the F9470.

1. The busy flag of the F9470 input ports is not visible to the programmer, hence the SKPBN and SKPBZ instructions should not be used with device codes 10 or 12.

2. After clearing a device-done flag, the F9470 requires time to clear the associated interrupt request. This time, which depends on the baud rate, varies from 10-100 microseconds. When performing interrupt-driven I/O, add a delay between the clear interrupt instruction and the next F9445 interrupt enable instruction. This delay ensures that the previously serviced request is cleared before the F9445 interrupt flag is re-enabled.

   A simple method of adding the required delay is to insert a no I/O (NIO) instruction between the interrupt clear instruction (e.g., DIAC O,TTI) and the subsequent interrupt enable (INTEN) instruction.

3. The F9470 interrupt mask bits are set by applying power to the board or executing an IORST instruction. To perform interrupt-driven I/O with the F9470, the mask bits must first be cleared with an MSKO instruction.

Table 3 F9470 I/O Service Instructions

Instruction	Description
DIAx ACC,DEV	Data In from A
DOAx ACC,DEV	Data Out from A
NIOx DEV	No I/O; Used to Start or Clear a Device
SKPBN DEV	Skip if Busy = 1
SKPBZ DEV	Skip if Busy = 0
SKPDN DEV	Skip if Done = 1
SKPDZ DEV	Skip if Done = 0

NOTES
If x = S (start), set busy flag, clear done.
If x = C (clear), clear busy flag, set done.
ACC = Accumulator 0, 1, 2, or 3.
DEV = Device Codes = 10, 11, 12, 13.
Note that Busy is not defined for input devices (TTI and PTR); hence, SKPBN and SKPBZ should not be used with these devices.

Table 4 F9470 Interrupt Control Commands

Instruction	Description
IORST	Clears all busy and done flags and sets all interrupt disable flags (disabling interrupts).
MSKO ACC	Enables or disables device interrupts by clearing or setting the interrupt disable flag in the device. The interrupt disable flag of each device is associated with a specific data line, and is set if its mask bit is 1, cleared if 0.
INTA ACC	Reads device code of highest priority device that is requesting an interrupt. The 6-bit code is loaded into ACC bits 10-15. All 16 bits are set to 0 if no device is interrupting.

Interrupt Disable Bits for I/O Devices

IB Bits	8	9	10	11	12	13	14	15
Mnemonic				PTR		PTP	TTI	TTO
Function				CH2 In		CH2 Out	CH1 In	CH1 Out

Table 5 Instruction Device Codes for IOSM

Device Code	Mnemonic	Description	Action
10	TTI	Teletype In	Input on Channel 1
11	TTO	Teletype Out	Output on Channel 1
12	PTR	Paper Tape Reader	Input on Channel 2
13	PTP	Paper Tape Punch	Output on Channel 2
77	CPU	CPU	

Hardware Interface

The F9470 interfaces to the F9445 through the 16-bit information bus (IB), the processor status lines ($\overline{M}$, O_1, O_0), and the processor control lines (RDYA, RDYD, BUSGNT, $\overline{CONREQ}$, and $\overline{INTREQ}$). All data transfers between the F9445 and the F9470 occur on the IB. These transfers are controlled by the three bus wait lines (RDYA, RDYD, and BUSGNT). Refer to figure 1.

The F9470 requests interrupt and console service by asserting $\overline{INTREQ}$ and $\overline{CONREQ}$, respectively. The F9470 determines the processor cycle type (e.g., read console code, or read console data) during console operations by sensing the $\overline{M}$, O_1, and O_0 lines. (For more information on F9445 data transfers, see the F9445 data sheet.) The F9470 uses standard serial line driver/receivers (1488/1489) and requires a 3.57954 MHz parallel resonant crystal.

The F9470 outputs use open collectors with internal 6 kΩ pull-up resistors. The $\overline{CONREQ}$, $\overline{INTREQ}$, BUSGNT, and RDYD outputs may interface directly to the F9445 if the F9470 drive characteristics are not exceeded. All F9470 inputs, except XTL_1 and XTL_2, have internal 6 kΩ pull-up resistors.

The F9470 requires external logic that denies RDYA and asserts $\overline{IODEC}$ during an I/O instruction to devices 10-13 and optionally 77. There are three components to this decoding logic, as shown in figure 1:

1. An LS533 latches the upper four device code bits ($\overline{IB}_{10}$-$\overline{IB}_{13}$) using STRBA. This data is typically available elsewhere in an F9445-based system.

2. The LS138 decodes the I/O instruction device code and produces an output if the instruction addresses devices 10-13. Output also occurs with DS77 if J2 is installed.

3. The LS74 delays the address phase of all I/O instructions for two clocks to provide the delay needed by the LS138.

Jumper Options

The three jumpers, J1, J2, and J3, tailor the F9470 to a particular system. In response to an interrupt acknowledge (INTA) instruction, the F9470 samples interrupt priority in ($\overline{INTPIN}$). When low, $\overline{INTPIN}$ indicates that no higher priority I/O device has a pending interrupt request, and that the F9470 should place its interrupt code on the IB. The $\overline{INTPIN}$ signal should be driven by the $\overline{INTPO}$ of the next higher priority device, if any; otherwise, install J1.

The J2 circuit allows the F9470 to respond to device code 77 instructions (INTA, MSKO, and IORST). Remove J2 when the F9470 is used in a system with other I/O devices that demand fast response to device code 77 instructions.

The J3 circuit enables the F9470 decode logic. With J3 removed, the F9470 does not respond to the F9445 I/O instructions.

DC Characteristics

The dc characteristics of the console controller are provided in table 6 (T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%, I/O Power Dissipation = 100 mW).

Figure 1 F9470 System Interface

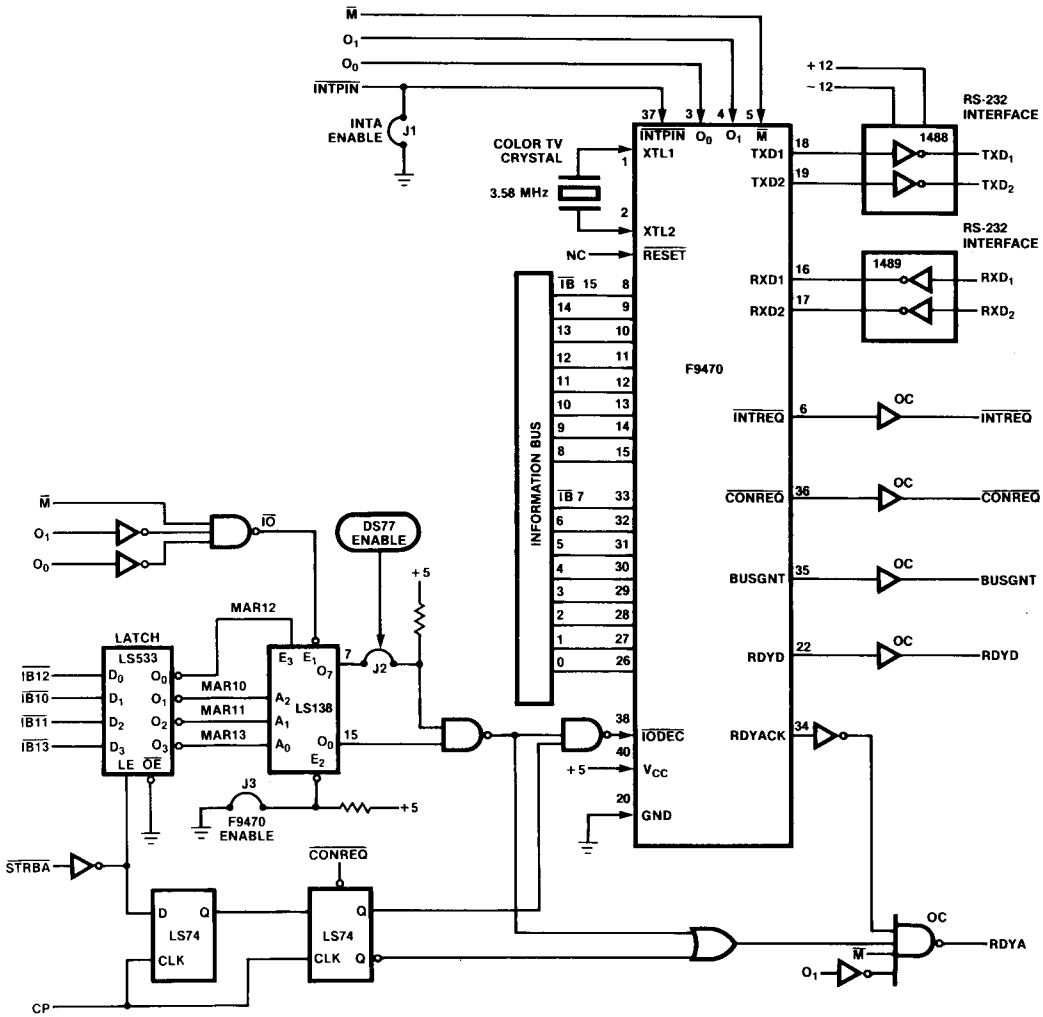

Table 6 Console Controller DC Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
I_{CC}	Power Supply Current	—	100	mA	Outputs Open
P_D	Power Dissipation	—	550.0	mW	Outputs Open
V_{IH}	Input High Voltage	2.0	5.8	V	
V_{IL}	Input Low Voltage	−0.3	0.8	V	
I_{LOD}	Leakage Current (open drain ports)	−10.0	+10.0	mA	Pull-down, device off V_{OH} = 13.2 V
I_{OL}	Output Low Current	1.8	—	mA	V_{OL} = 0.4 V

Absolute Maximum Ratings

These are stress ratings only, and functional operation at these ratings, or under any conditions above those indicated in this document, is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect device reliability, and exposure to stresses greater than those listed may cause permanent damage to the device.

Temperature (ambient) under bias
- F9470DC: 0 °C, +70 °C
- F9470DM: −55 °C, +125 °C

Storage temperature: −55 °C, +150 °C

Voltage on all open drain pins: −1.0 V, +13.2 V

Voltage on all other pins, with respect to ground: −1.0 V, +7.0 V

Power dissipation: 1.5W

Ordering Information

Part Number	Package	Temperature Range*
F9470DC	Ceramic	C
F9470DL	Ceramic	L
F9470DM	Ceramic	M

* C = Commercial Temperature Range 0 °C to +70 °C
L = Limited Temperature Range −40 °C to +85 °C
M = Military Temperature Range −55 °C to +125 °C

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