

128Kx32 3.3V SRAM MODULE

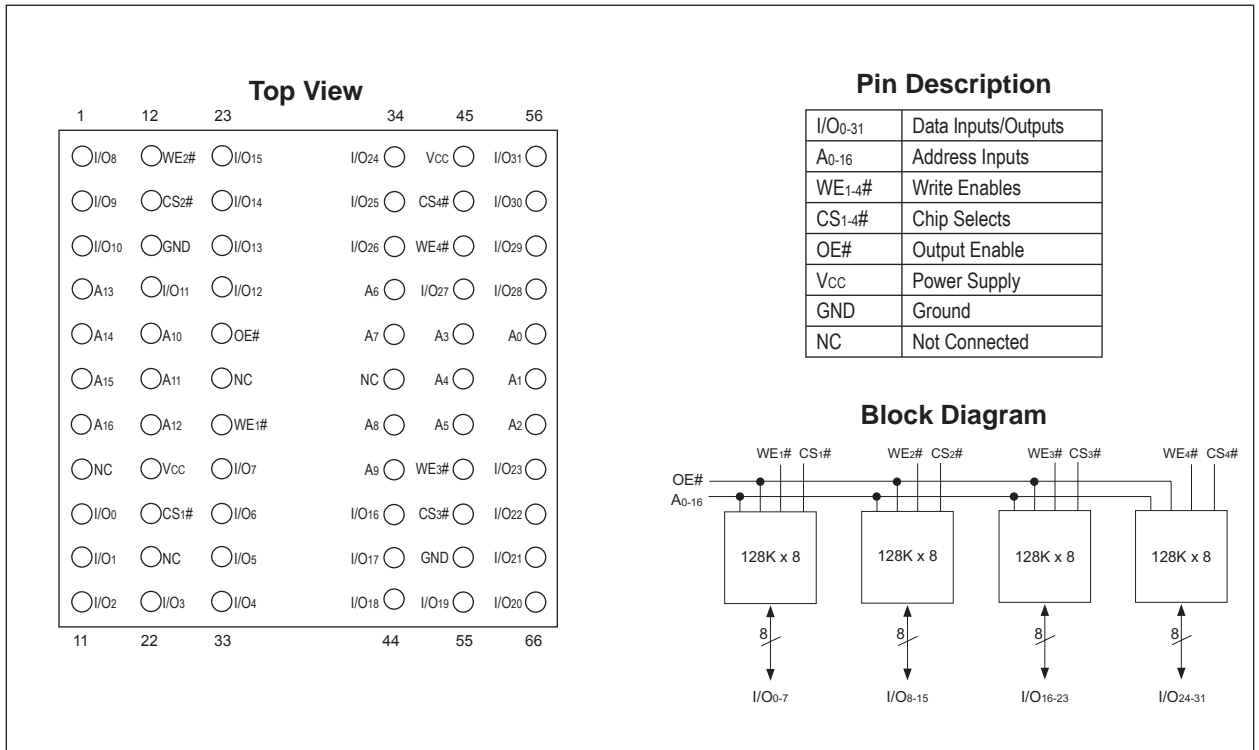
FEATURES

- Access Times of 15**, 17, 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Low Voltage Operation
- Packaging
 - 66-pin, PGA Type, 1.075 inch square Hermetic Ceramic HIP (Package 400)
 - 68 lead, Hermetic CQFP (G2U), 22.4mm (0.880 inch) square (Package 510), 3.56mm (0.140 inch) high.
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS128K32V-XG2UX - 8 grams typical
 - WS128K32NV-XH1X - 13 grams typical

* This product is subject to change without notice.

** Commercial and Industrial only.

FIGURE 1 – PIN CONFIGURATION FOR WS128K32NV-XH1X



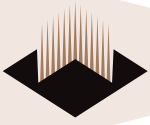
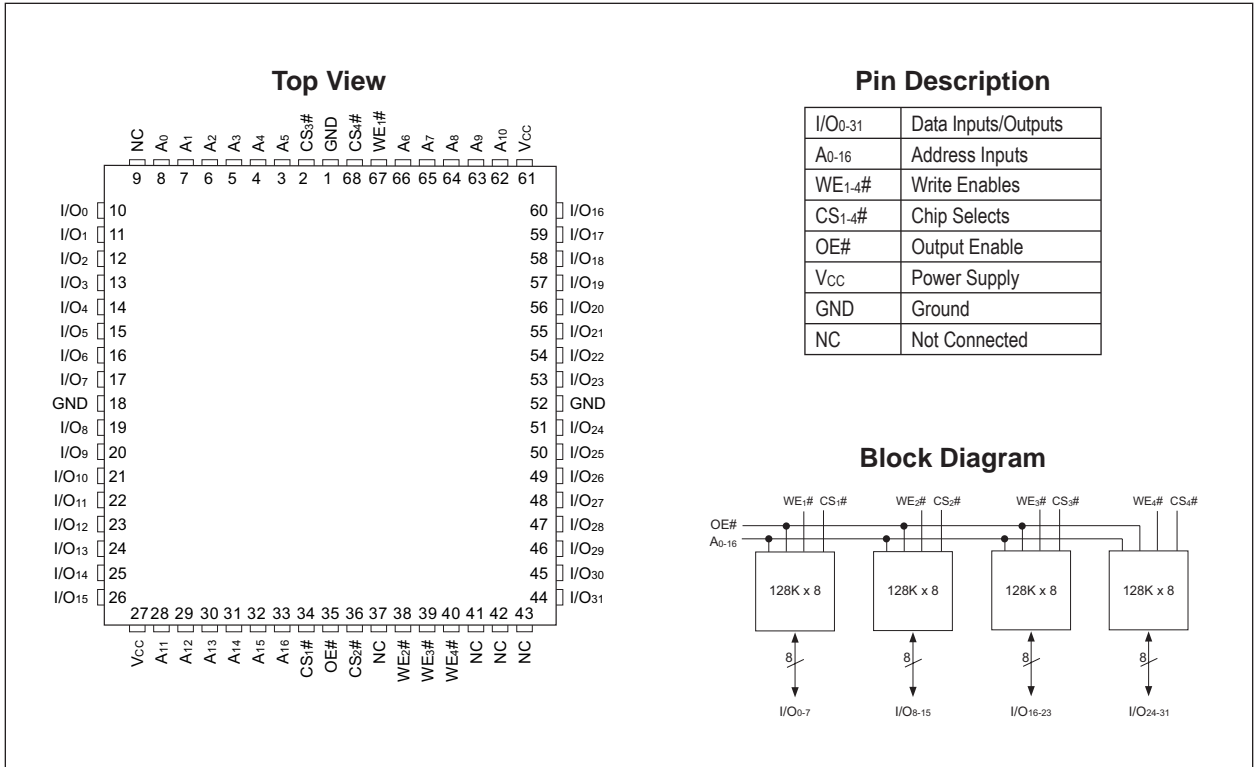


FIGURE 2 – PIN CONFIGURATION FOR WS128K32V-XG2UX





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	5.5	V

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V

CAPACITANCE

T_A = +25°C, V_{IN} = 0V, F = 1.0 MHz

Parameter	Symbol	Max	Unit
OE# capacitance	C _{OE}	50	pF
WE1-4# capacitance HIP (PGA)	C _{WE}	20	pF
CQFP G2U		15	
CS1-4# capacitance	C _{CS}	20	pF
Data# I/O capacitance	C _{I/O}	20	pF
Address input capacitance	C _{AD}	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 3.3V ±0.3V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC} x 32	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz		500	mA
Standby Current	I _{SB}	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz		32	mA
Output Low Voltage	V _{OL}	I _{OL} = 6mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V



AC CHARACTERISTICS

$V_{CC} = 3.3V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-15*		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		35		ns
Address Access Time	t_{AA}		15		17		20		25		35	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25		35	ns
Output Enable to Output Valid	t_{OE}		10		11		12		15		20	ns
Chip Select to Output in Low Z	t_{CLZ}^1	5		5		5		5		5		ns
Output Enable to Output in Low Z	t_{OLZ}^1	5		5		5		5		5		ns
Chip Disable to Output in High Z	t_{CHZ}^1		8		9		10		12		15	ns
Output Disable to Output in High Z	t_{OHZ}^1		8		9		10		12		15	ns

1. This parameter is guaranteed by design but not tested.

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AC Characteristics

$V_{CC} = 3.3V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-15*		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		35		ns
Chip Select to End of Write	t_{CW}	13		14		15		20		30		ns
Address Valid to End of Write	t_{AW}	13		14		15		20		30		ns
Data Valid to End of Write	t_{DW}	10		11		12		15		18		ns
Write Pulse Width	t_{WP}	13		14		15		20		30		ns
Address Setup Time	t_{AS}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		0		ns
Output Active from End of Write	t_{OW}^1	5		5		5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}^1		8		9		10		10		15	ns
Data Hold Time	t_{DH}	0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

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FIGURE 3 – AC TEST CIRCUIT

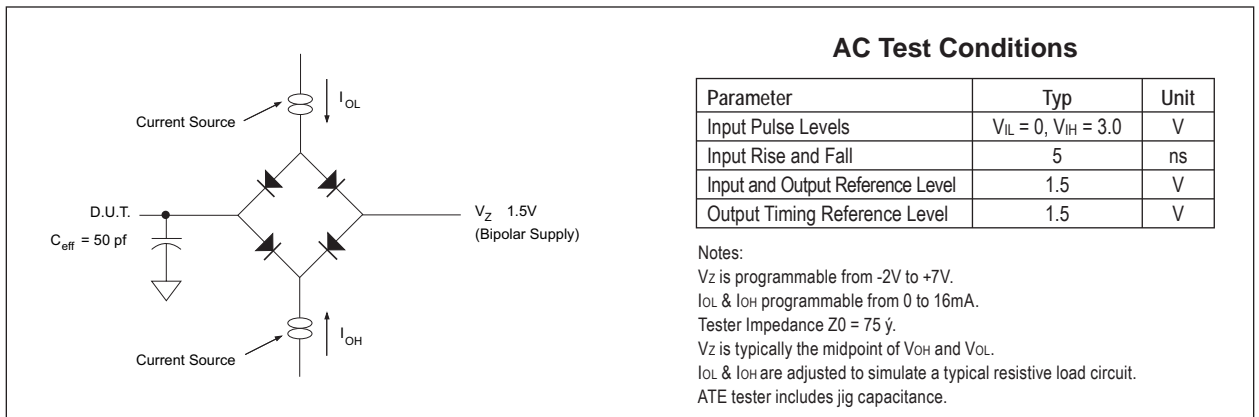




FIGURE 4 – TIMING WAVEFORM - READ CYCLE

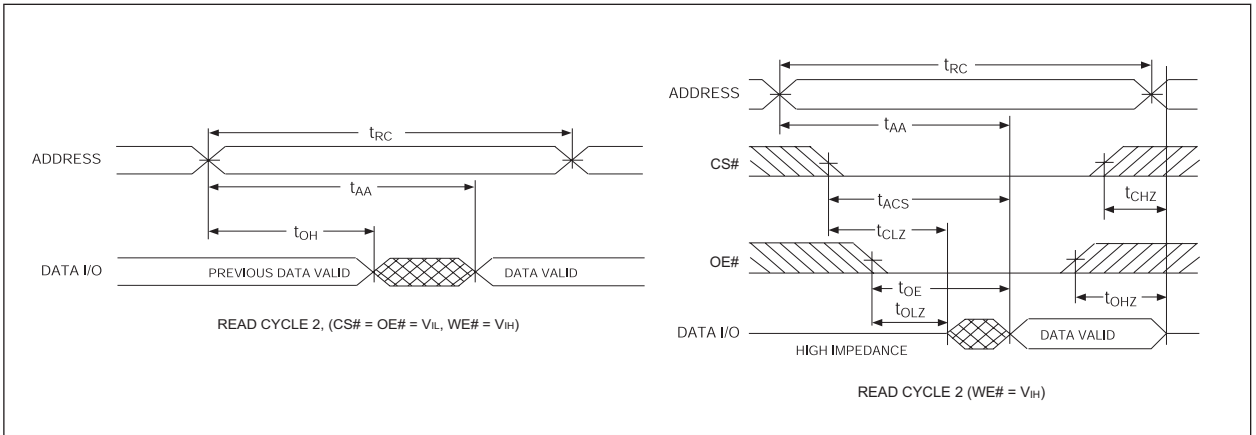


FIGURE 5 – WRITE CYCLE - WE# CONTROLLED

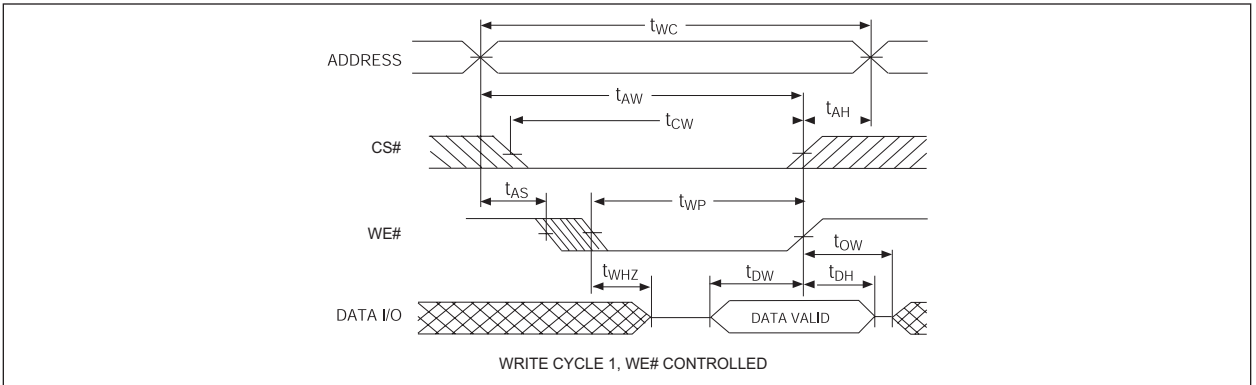
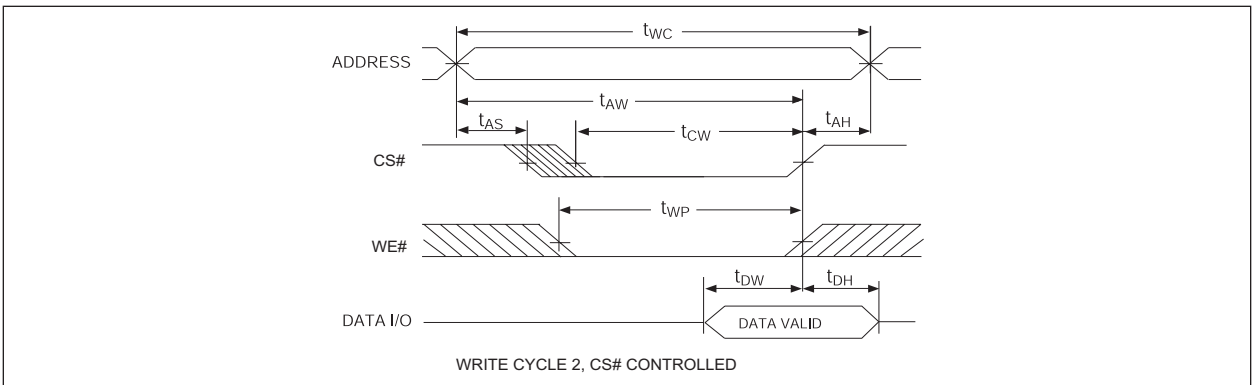
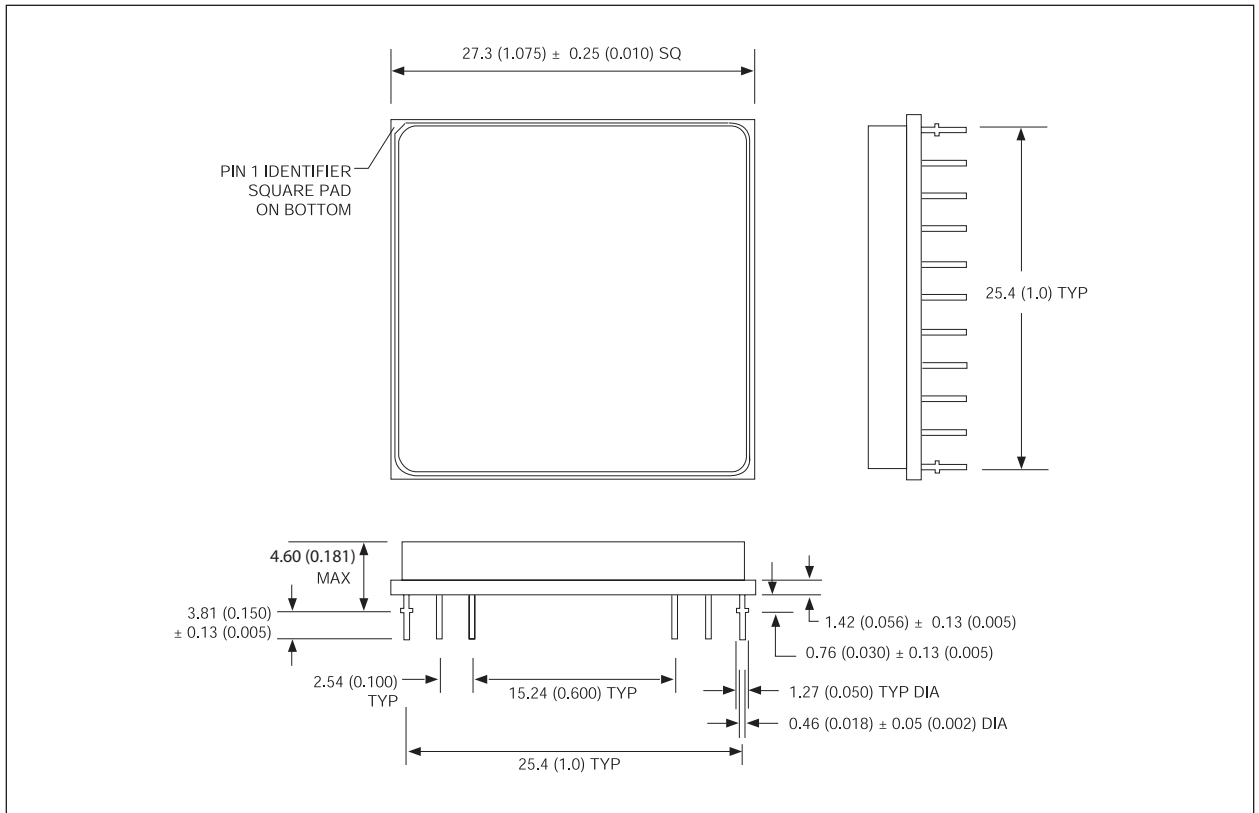


FIGURE 6 – WRITE CYCLE - CS# CONTROLLED





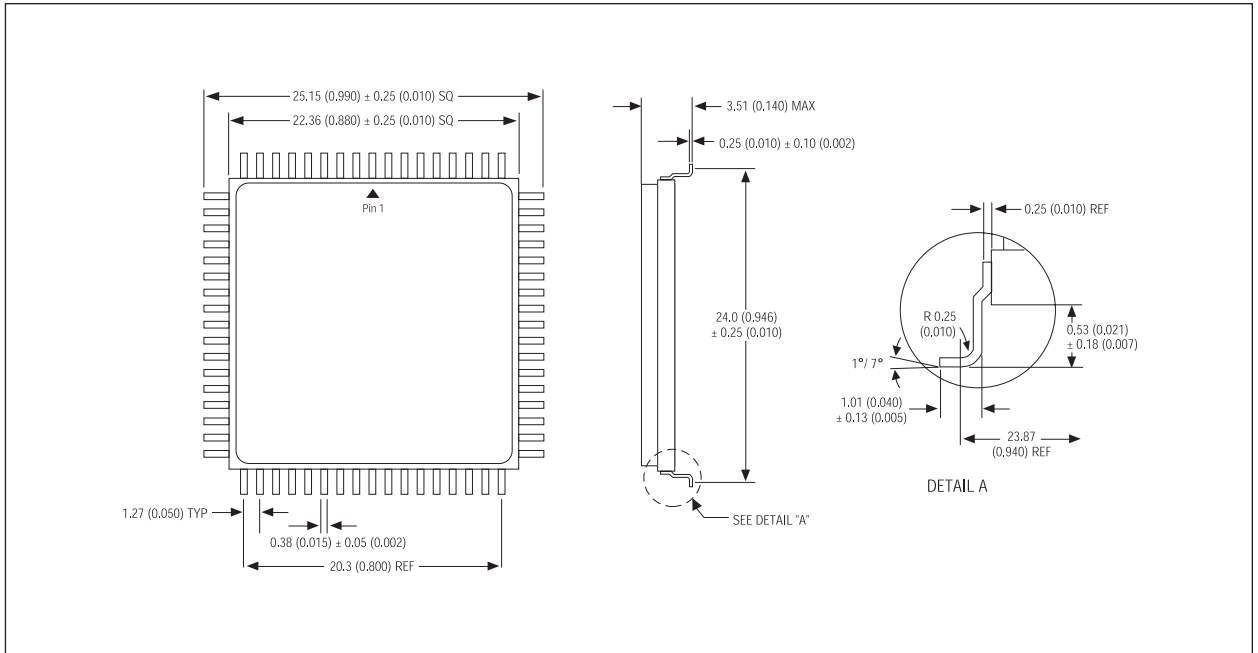
PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 510: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2U)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



W S 128K 32 X V - XXX X X X

LEAD FINISH:

Blank = Gold plated leads
A = Solder dip leads

DEVICE GRADE:

M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:

H1 = Ceramic Hex-In-line Package, HIP (Package 400)
G2U = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 510)

ACCESS TIME (ns)

LOW VOLTAGE SUPPLY 3.3V ± 10%

IMPROVEMENT MARK:

N = No Connect at pins 8, 21, 28, 39 in HIP for upgrade. (H1 only)

ORGANIZATION, 128Kx32

User configurable as 256Kx16 or 512Kx8

SRAM

WHITE ELECTRONIC DESIGNS CORP.