FEMTOCLOCKS™ 1:5, CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

ICS840245I

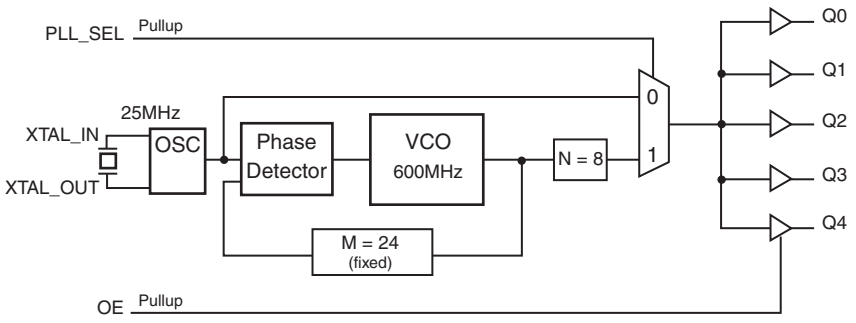
General Description

The ICS840245I is a low skew, 1-to-5 LVCMOS/LVTTL SATA/SAS Clock Generator and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. The ICS840245I can synthesize 75MHz reference clock frequencies with a 25MHz crystal. Each of the 5 outputs on the ICS840245I can drive two series terminated 50Ω transmission lines, effectively making the ICS840245I a 1-to-10 clock generator. An output enable (OE) pin, which controls only the Q4 output, allows the application to use Q4 as an optional output (for example, test output pin). The ICS840245I uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical random rms phase jitter. The ICS840245I is packaged in a 16-pin TSSOP package.

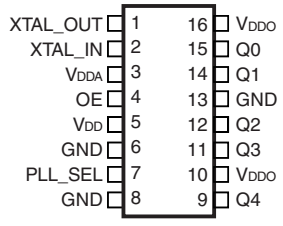
Features

- Five LVCMOS outputs, 15Ω typical output impedance
- Crystal oscillator interface
- Supports the following output frequency: 75MHz
- Output skew: 25ps (typical)
- RMS phase jitter @ 75MHz (900kHz - 7.5MHz): 0.454ps (typical)
- Output supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS840245I
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface.
3	V_{DDA}	Power		Analog supply pin.
4	OE	Input	Pullup	Output clock enable pin. When HIGH, Q4 output is enabled. When LOW, forces Q4 to Hi-Z state. LVCMOS/LVTTL interface levels. See Table 3A.
5	V_{DD}	Power		Core supply pin.
6, 8, 13	GND	Power		Power supply ground.
7	PLL_SEL	Input	Pullup	PLL select pin. Selects between PLL and bypass mode. When HIGH, PLL is enabled. LVCMOS/LVTTL interface levels. See Table 3B.
9, 11, 12, 14, 15	Q4, Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
10, 16	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance			8		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance	3.3V±5%		15		Ω
		2.5V±5%		20		Ω

TABLE 3A. CONTROL FUNCTION TABLE

Control Input	Output
OE	**Q0**
0	Hi-Z
1	Active

TABLE 3B. PLL_SEL FUNCTION TABLE

Control Input	Outputs
PLL_SEL	**Q0:Q4**
0	Bypass
1	PLL

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.08	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				48	mA
I_{DDA}	Analog Supply Current				8	mA
I_{DDO}	Output Supply Current	No Load			36	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				48	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current	No Load			32	mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				43	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current	No Load			32	mA

TABLE 4D. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE, PLL_SEL	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	OE, PLL_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.3V±5%	2.6			V
			V_{DDO} = 2.5V±5%	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.3V±5% or 2.5V±5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information, Output Load Test Circuit.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pf parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			75		MHz
*t*sk(o)	Output Skew; NOTE 1, 3				55	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	Integration Range: 900kHz - 7.5MHz		0.503		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
odc	Output Duty Cycle		49		51	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			75		MHz
*t*sk(o)	Output Skew; NOTE 1, 3				55	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	Integration Range: 900kHz - 7.5MHz		0.494		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
odc	Output Duty Cycle		49		51	%

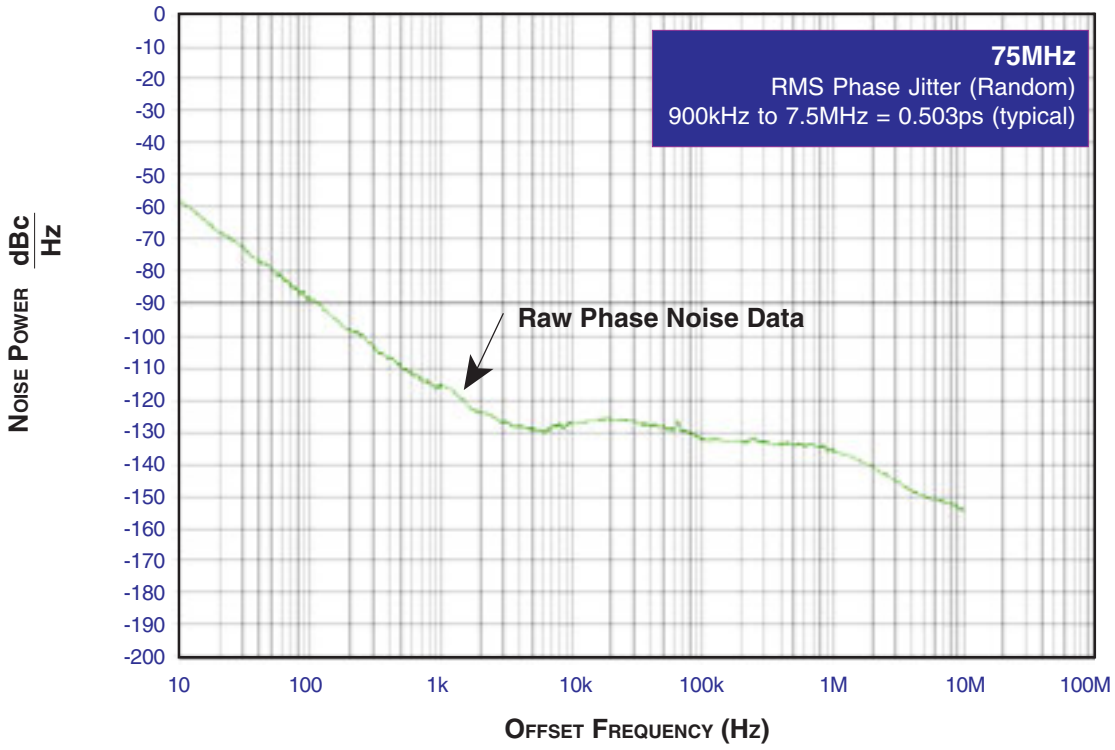
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6C. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

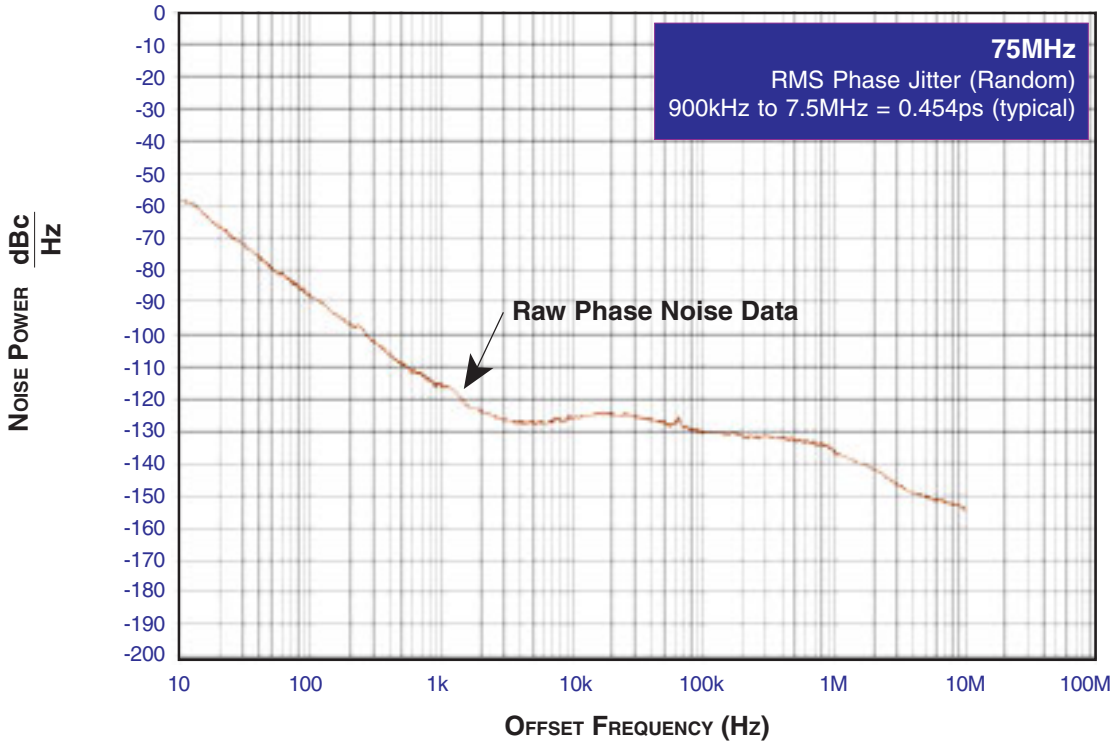
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			75		MHz
*t*sk(o)	Output Skew; NOTE 1, 3				50	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	Integration Range: 900kHz - 7.5MHz		0.454		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle		49		51	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

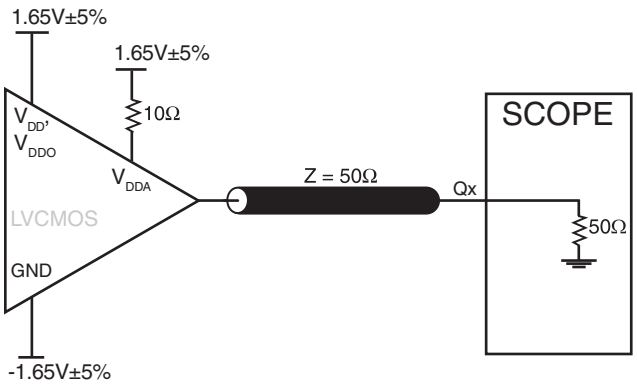
Typical Phase Noise at 75MHz @ 3.3V



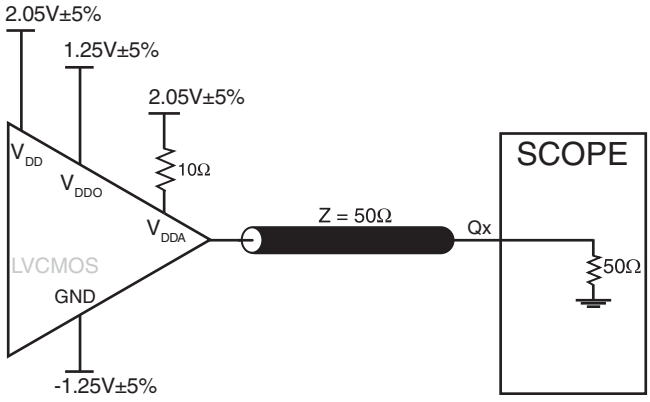
Typical Phase Noise at 75MHz @ 2.5V



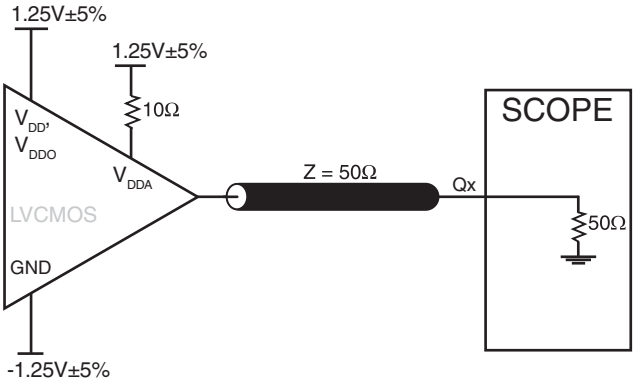
PARAMETER MEASUREMENT INFORMATION



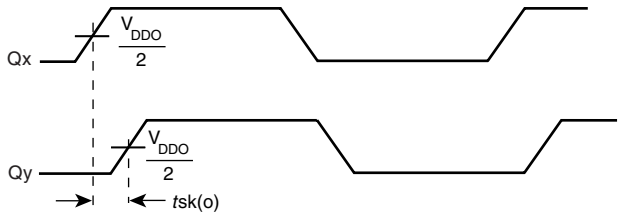
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



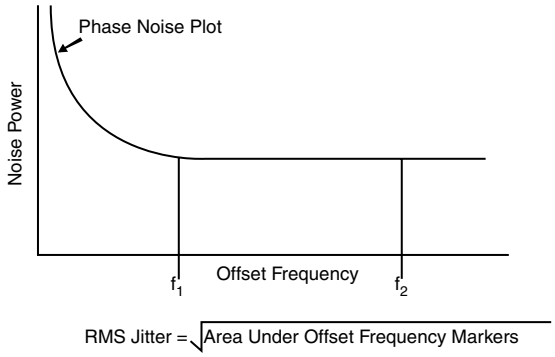
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



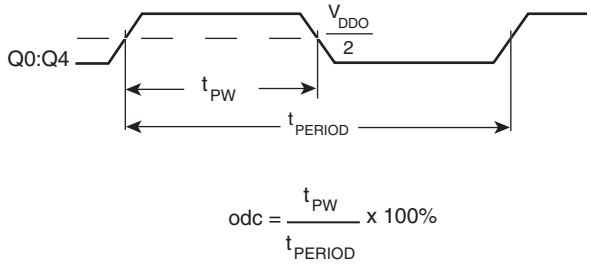
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



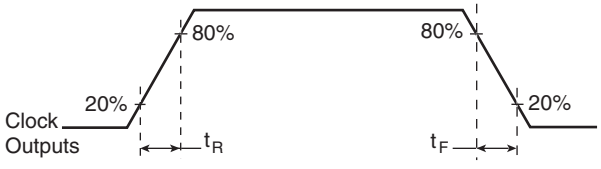
OUTPUT SKEW



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840245I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

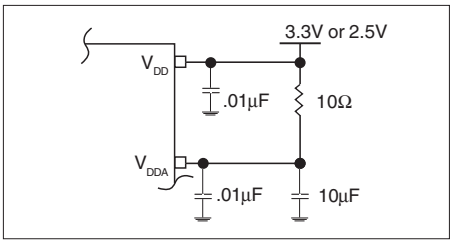


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. There should be no trace attached.

Crystal Input Interface

The ICS840245I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

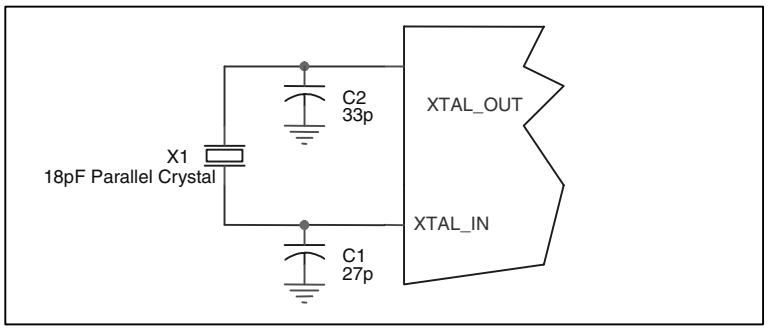


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

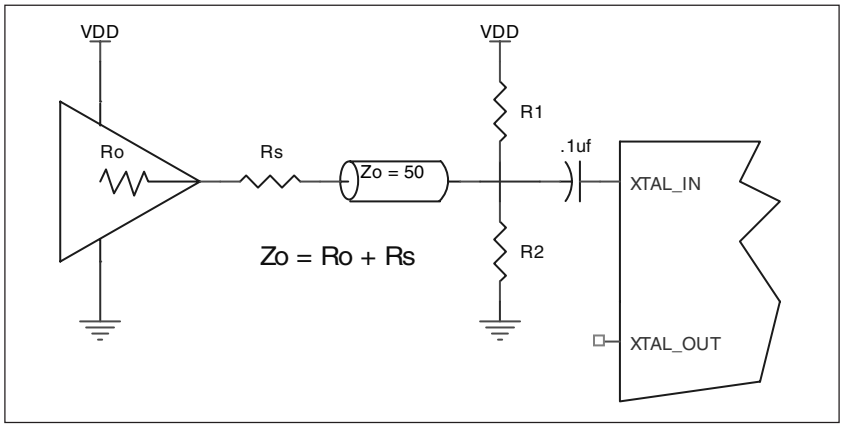


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS840245I is: 1965

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

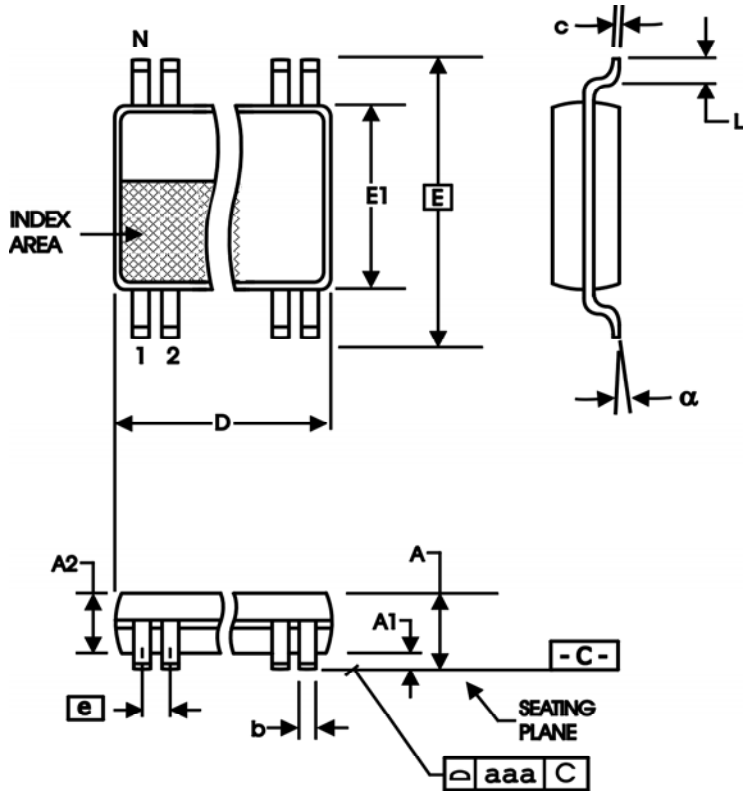


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840245AGI	840245AI	16 Lead TSSOP	tube	-40°C to 85°C
ICS840245AGIT	840245AI	16 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS840245AGILF	40245AIL	16 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS840245AGILFT	40245AIL	16 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T4A	3	Power Supply 3.3V DC Characteristics Table - changed I_{DD} max. from 41mA to 48mA.	11/16/06
	T4B	3	Power Supply 3.3/2.5V DC Characteristics Table - changed I_{DD} max. from 40mA to 48mA, I_{DDA} max. from 8mA to 12mA, I_{DDO} from 27mA to 32mA, and V_{DDA} min. from V_{DD} - 0.08V to V_{DD} - 0.12V.	
	T4C	3	Power Supply 2.5V DC Characteristics Table - changed I_{DD} max. from 38mA to 43mA, I_{DDA} max. from 8mA to 12mA, I_{DDO} from 27mA to 32mA, and V_{DDA} min. from - 0.08V to V_{DD} - 0.12V.	
		9	Corrected Crystal Input Interface drawing.	

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