

74ACT1284 IEEE 1284 Transceiver

General Description

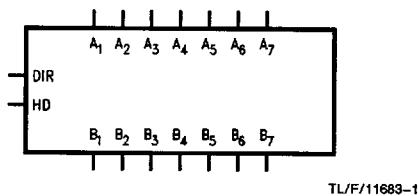
The 'ACT1284 contains four non-inverting bidirectional buffers and three non-inverting buffers with open Drain outputs and high drive capability on the B ports. It is intended to provide a standard signaling method for a bi-direction parallel peripheral in an Extended Capabilities Port mode (ECP).

The HD (active HIGH) input pin enables the B ports to switch from open Drain to a high drive totem pole output, capable of sourcing 14 mA on all seven buffers. The DIR input determines the direction of data flow on the bidirectional buffers. DIR (active HIGH) enables data flow from A ports to B ports. DIR (active LOW) enables data flow from B ports to A ports.

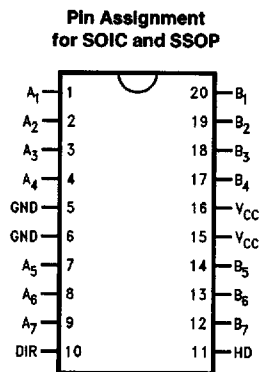
Features

- TTL-compatible inputs
- A ports have standard 4 mA totem pole outputs
- Typical input hysteresis of 0.5V
- B port high drive source/sink capability of 14 mA
- Bidirectional non-inverting buffers
- Supports IEEE P1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals
- B-port outputs in High Impedance mode during power down
- Guaranteed 4000V minimum ESD protection

Logic Symbol



Connection Diagram



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Pin Descriptions

Pin Names	Description
HD	High Drive Enable Input (Active High)
DIR	Direction Control Input
A ₁ -A ₄	Side A Inputs or Outputs
B ₁ -B ₄	Side B Inputs or Outputs
A ₅ -A ₇	Side A Inputs
B ₅ -B ₇	Side B Outputs

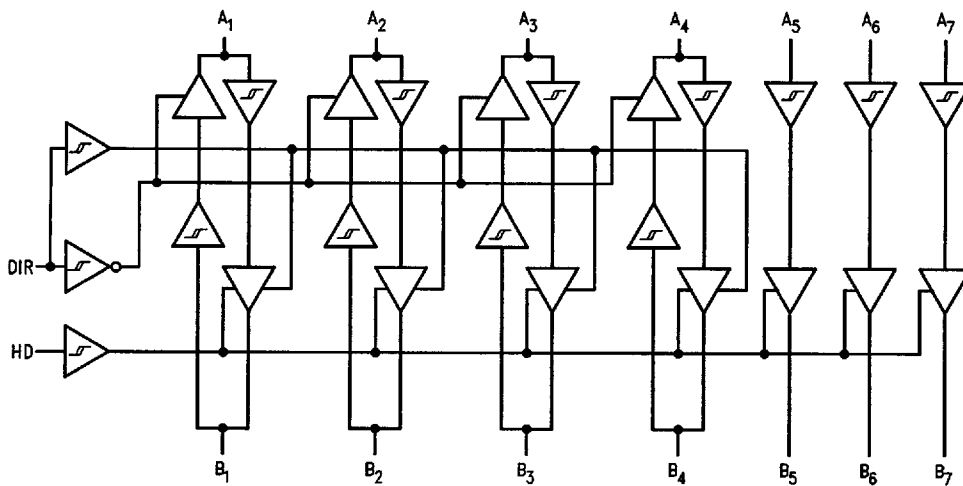
Truth Table

Inputs		Outputs
DIR	HD	
L	L	B ₁ -B ₄ Data to A ₁ -A ₄ , and A ₅ -A ₇ Data to B ₅ -B ₇ *
L	H	B ₁ -B ₄ Data to A ₁ -A ₄ , and A ₅ -A ₇ Data to B ₅ -B ₇
H	L	A ₁ -A ₇ Data to B ₁ -B ₇ **
H	H	A ₁ -A ₇ Data to B ₁ -B ₇

Note: *B₅-B₇ Open Drain Outputs

**B₁-B₇ Open Drain Outputs

Logic Diagram



TL/F/11683-3

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I) A Side	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage (V_I) B Side	-2V to +7V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O) A Side	-0.5V to $V_{CC} + 0.5V$
DC Output Voltage (V_O) B Side	-2V to +7V
DC Output Source or Sink Current (I_O)	±50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) -65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.7V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A) ACT	-40°C to +85°C

DC Characteristics

Symbol	Parameter	V_{CC} (V)	Guaranteed Limits			Units	Conditions
			$T_A = +25^\circ\text{C}$	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
V_{IH}	Minimum High Level Input Voltage	4.7	2.0	2.0	2.0	V	Recognized High Signal
		5.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.7	0.8	0.8	0.8	V	Recognized Low Signal
		5.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.7	4.5	4.5	4.5	V	$I_{OUT} = -50 \mu\text{A} (A_n)$ * $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -4 \text{ mA} (A_n)$
		4.7	3.7	3.7	3.7		
		4.7	2.4	2.4	2.4		
V_{OL}	Maximum Low Level Output Voltage	4.7	0.2	0.2	0.2	V	$I_{OUT} = 50 \mu\text{A} (A_n)$ * $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 4 \text{ mA} (A_n)$
		4.7	0.4	0.4	0.4		
		4.7	0.3	0.3	0.4		
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	±1.0	±1.0	μA	$V_I = V_{CC}, \text{GND}$ (DIR, A5, A6, A7, HD)
I_{CCT}	Maximum I_{CC} /Input	5.5		1.5	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{CC}	Maximum Quiescent Supply Current	5.5	400	400	500	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum Output Leakage Current	5.5	±20	±20	±20	μA	$V_O = V_{CC}, \text{GND}$
I_{OFF}	Maximum B-Side Power Down Leakage Current	0.0	100	100	100	μA	$V_{OUT} = 5.25V$
ΔV_T	Input Hysteresis	5.0	0.4	0.4	0.35	V	$V_{T+} - V_{T-}$
R_D	Maximum Output Impedance	5.0	22	22	24	Ω	B_n (Note 1)
	Minimum Output Impedance	5.0	8	8	6	Ω	B_n (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

Note 1: This parameter is guaranteed but not tested, characterized only. R_D is the measure of the B-side output impedance with the output in the high state.

AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = 4.7V-5.5V		T _A = 0°C to +70°C V _{CC} = 4.7V-5.5V		T _A = -40°C to +85°C V _{CC} = 4.7V-5.5V		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t _{PHL}	A ₁ -A ₇ to B ₁ -B ₇	2.0	20.0	2.0	20.0	2.0	24.0	ns	1
t _{PLH}	A ₁ -A ₇ to B ₁ -B ₇	2.0	20.0	2.0	20.0	2.0	24.0	ns	2
t _{PHL}	B ₁ -B ₄ to A ₁ -A ₄	2.0	20.0	2.0	20.0	2.0	24.0	ns	3
t _{PLH}	B ₁ -B ₄ to A ₁ -A ₄	2.0	20.0	2.0	20.0	2.0	24.0	ns	3
t _{pEnable}	Output Enable Time HD to B ₁ -B ₇	2.0	20.0	2.0	20.0	2.0	24.0	ns	2
t _{pDisable}	Output Disable Time HD to B ₁ -B ₇	2.0	20.0	2.0	20.0	2.0	24.0	ns	2
t _{SLEW} t _{PLH} t _{PHL}	Output Slew Rate B ₁ -B ₇	0.05	0.40	0.05	0.40	0.05	0.40	V/ns	1, 2
t _r , t _f	t _{RISE} and t _{FALL} B ₁ -B ₇ *		120		120		120	ns	4 (Note 1)

*Open Drain

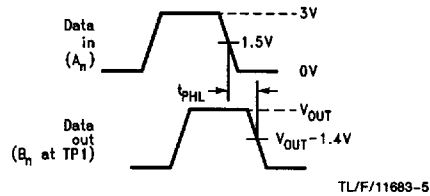
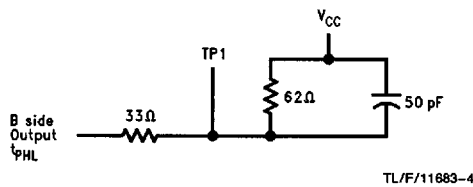
Note 1: This parameter is guaranteed but not tested, characterized only.

Note: Pulse Generator for all pulses; Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.0	pF	V _{CC} = OPEN (HD, DIR, A ₅ -A ₇)
C _{I/O} (Note 1)	I/O Pin Capacitance	12.0	pF	V _{CC} = 5.0V

AC Loading and Waveforms



t_{SLEW} measures between 10% to 90% on the t_{PHL} Transition

FIGURE 1. A to B Direction Test Load and Waveforms

AC Loading and Waveforms (Continued)

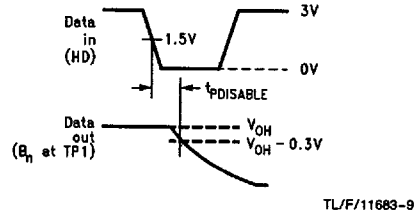
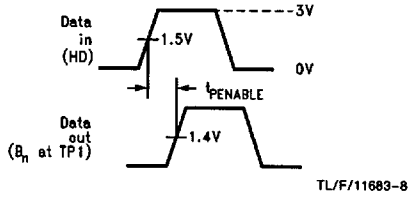
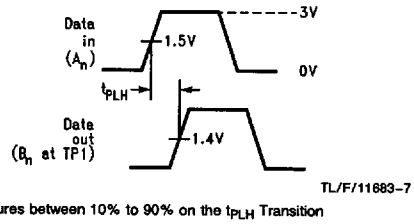
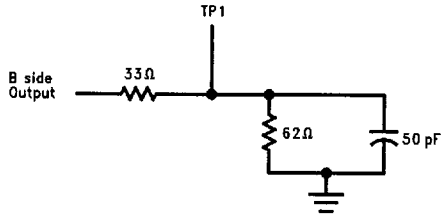


FIGURE 2. B Output Test Load and Waveforms

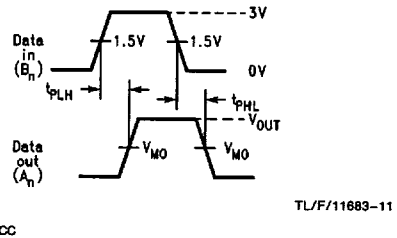
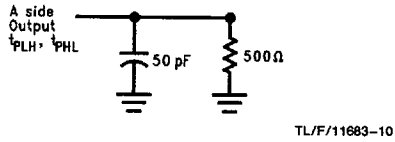


FIGURE 3. B to A Direction Test Load and Waveforms for Outputs A₁-A₄

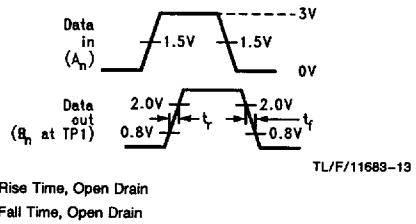
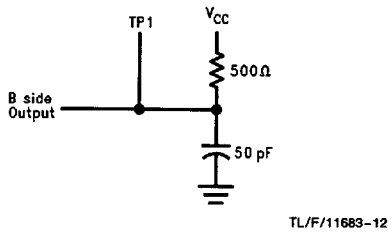
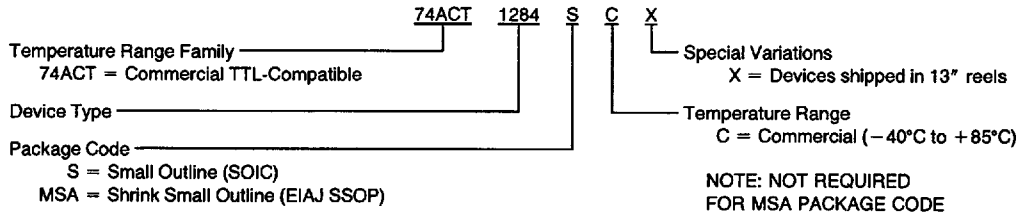


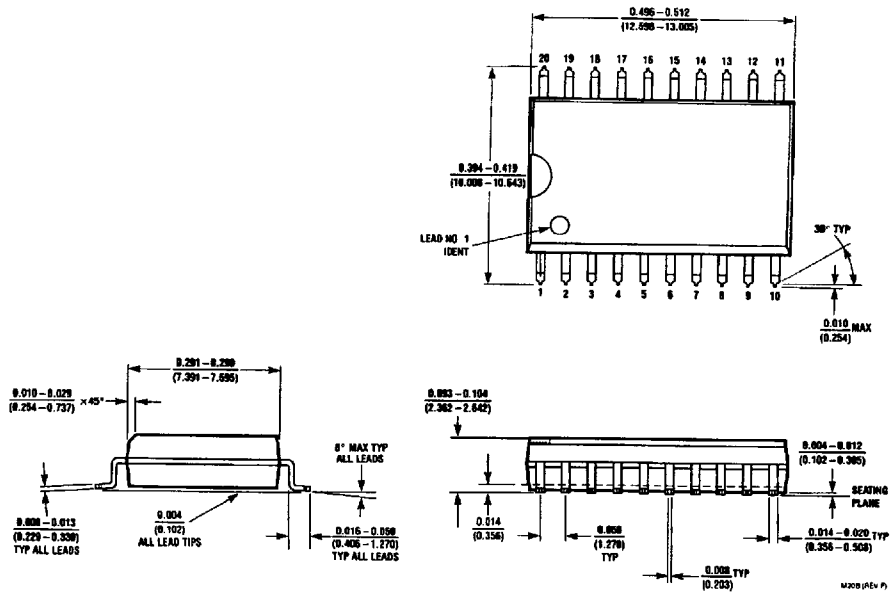
FIGURE 4. A to B Direction Test Load and Waveforms for Open Drain Outputs B₁-B₇

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

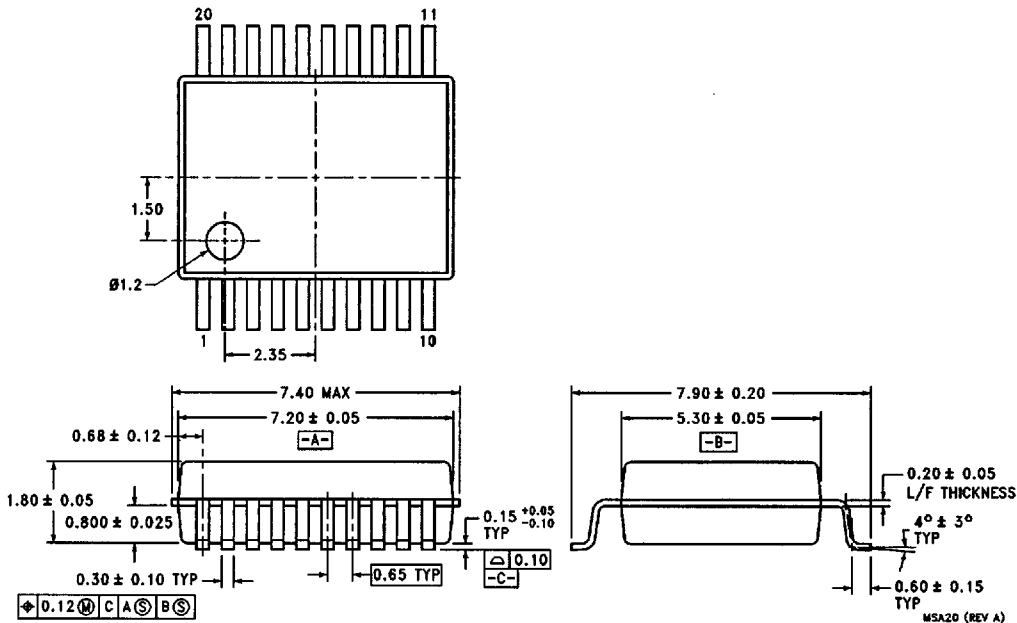


Physical Dimensions inches (millimeters) unless otherwise noted



**20 Lead Small Outline Integrated Circuit (S)
NS Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20 Lead Plastic EIAJ SSOP (MSA)
NS Package Number MSA20**

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