PRELIMINARY

# M5M416165CJ,TP-5,-6,-7, -5S,-6S,-7S

## HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

### DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

### FEATURES

| Type name | $\overline{RAS}$ access time (max.ns) | $\overline{CAS}$ access time (max.ns) | Address access time (max.ns) | $\overline{OE}$ access time (max.ns) | Cycle time (min.ns) | Power dissipation (typ.mW) |
|---|---|---|---|---|---|---|
| M5M416165CXX-5,-5S | 50 | 13 | 25 | 13 | 90 | 540 |
| M5M416165CXX-6,-6S | 60 | 15 | 30 | 15 | 110 | 430 |
| M5M416165CXX-7,-7S | 70 | 20 | 35 | 20 | 130 | 385 |

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ---------- CMOS input level
- Low operating power dissipation
  M5M416165Cxx-5,-5S ---------- 660.0mW (Max)
  M5M416165Cxx-6,-6S ---------- 525.0mW (Max)
  M5M416165Cxx-7,-7S ---------- 470.0mW (Max)
- Hyper-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms ($A_0$~$A_{11}$)
  * : Applicable to self refresh version (M5M416165CJ,TP-5S,-6S, -7S : option) only

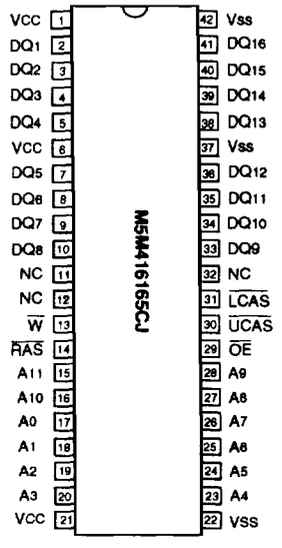
### APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

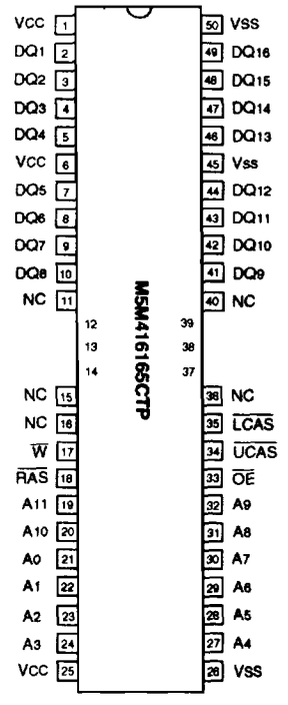
### PIN DESCRIPTION

| Pin name | Function |
|---|---|
| $A_0$~$A_{11}$ | Address inputs |
| $DQ_1$~$DQ_{16}$ | Data inputs/outputs |
| $\overline{RAS}$ | Row address strobe input |
| $\overline{UCAS}$ | Upper byte control column address strobe input |
| $\overline{LCAS}$ | Lower byte control column address strobe input |
| $\overline{W}$ | Write control input |
| $\overline{OE}$ | Output enable input |
| Vcc | Power supply (+5.0V) |
| Vss | Ground (0V) |

### PIN CONFIGURATION (TOP VIEW)




Outline 42P0N-A (400mil SOJ)




Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION



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PRELIMINARY

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

## FUNCTION

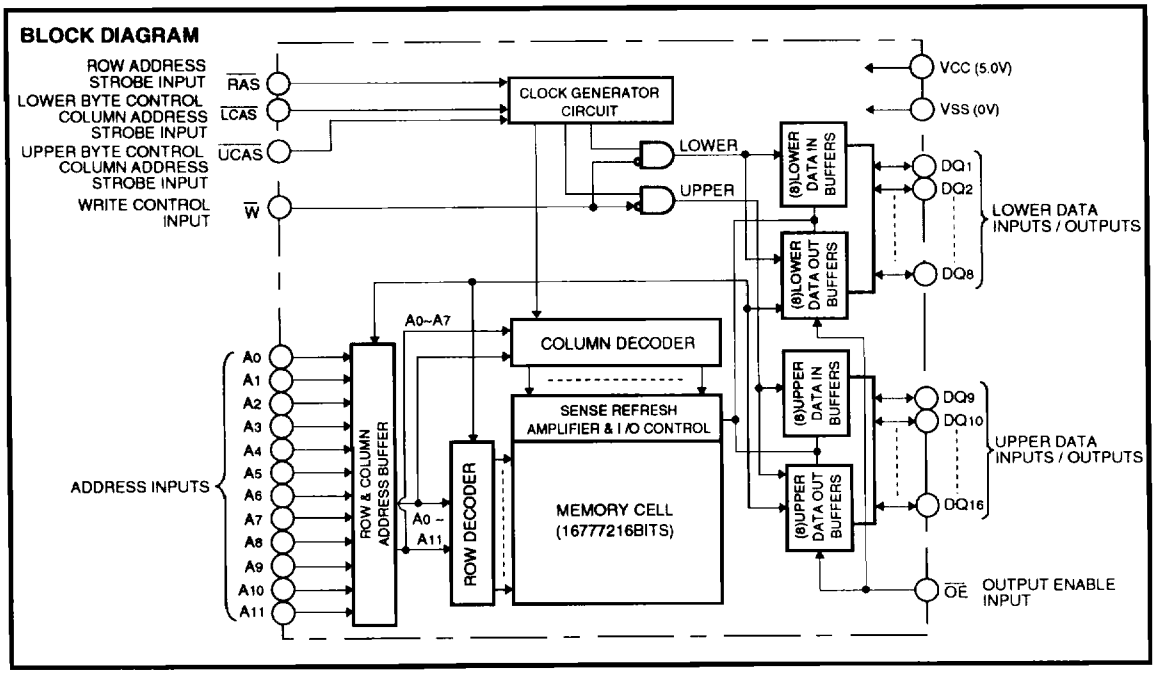
The M5M416165CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

| Operation | Inputs | | | | | Input/Output | |
|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{W}$ | $\overline{OE}$ | DQ1~DQ8 | DQ9~DQ16 |
| Lower byte read | ACT | ACT | NAC | NAC | ACT | DOUT | OPN |
| Upper byte read | ACT | NAC | ACT | NAC | ACT | OPN | DOUT |
| Word read | ACT | ACT | ACT | NAC | ACT | DOUT | DOUT |
| Lower byte write | ACT | ACT | NAC | ACT | NAC | DIN | DNC |
| Upper byte write | ACT | NAC | ACT | ACT | NAC | DNC | DIN |
| Word write | ACT | ACT | ACT | ACT | NAC | DIN | DIN |
| $\overline{RAS}$-only refresh | ACT | NAC | NAC | DNC | DNC | OPN | OPN |
| Hidden refresh | ACT | ACT | ACT | NAC | ACT | DOUT | DOUT |
| $\overline{CAS}$ before $\overline{RAS}$ refresh | ACT | ACT | ACT | DNC | DNC | OPN | OPN |
| Stand-by | NAC | DNC | DNC | DNC | DNC | OPN | OPN |

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

## BLOCK DIAGRAM



PRELIMINARY

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Vcc | Supply voltage | With respect to Vss | -1～7 | V |
| V I | Input voltage | | -1～7 | V |
| Vo | Output voltage | | -1～7 | V |
| I o | Output current | | 50 | mA |
| Pd | Power dissipation | Ta=25 °C | 1000 | mW |
| Topr | Operating temperature | | 0～70 | °C |
| Tstg | Storage temperature | | -65～150 | °C |

## RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| Vcc | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| Vss | Supply voltage | 0 | 0 | 0 | V |
| VIH | High-level input voltage, all inputs | 2.4 | | 6.0 | V |
| VIL | Low-level input voltage, all inputs | -1 | | 0.8 | V |

Note 1 : All voltage values are with respect to VSS.

## ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| VOH | High-level output voltage | | IOH=-5.0mA | 2.4 | | Vcc | V |
| VOL | Low-level output voltage | | IOL=4.2mA | 0 | | 0.4 | V |
| IOZ | Off-state output current | | Q floating 0V≦VOUT≦5.5V | -10 | | 10 | μA |
| II | Input current | | 0V≦VIN≦6V, Other inputs pins=0V | -10 | | 10 | μA |
| ICC1(AV) | Average supply current from Vcc operating (Note 3,4,5) | M5M416165C-5,-5S | $\overline{RAS}$, $\overline{CAS}$ cycling tRC=tWC=min. output open | | | 120 | mA |
| | | M5M416165C-6,-6S | | | | 95 | |
| | | M5M416165C-7,-7S | | | | 85 | |
| ICC2 | Supply current from Vcc, stand-by (Note 6) | | $\overline{RAS}$= $\overline{CAS}$ =VIH, output open | | | 2 | mA |
| | | | $\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.2V output open | | | 1 | |
| | | | | | | 0.3* | |
| ICC3(AV) | Average supply current from Vcc refreshing (Note 3,5) | M5M416165C-5,-5S | $\overline{RAS}$ cycling, $\overline{CAS}$=VIH tRC=min. output open | | | 120 | mA |
| | | M5M416165C-6,-6S | | | | 95 | |
| | | M5M416165C-7,-7S | | | | 85 | |
| ICC4(AV) | Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5) | M5M416165C-5,-5S | $\overline{RAS}$=VIL, $\overline{CAS}$ cycling tPC=min. output open | | | 165 | mA |
| | | M5M416165C-6,-6S | | | | 130 | |
| | | M5M416165C-7,-7S | | | | 110 | |
| ICC6(AV) | Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3) | M5M416165C-5,-5S | $\overline{CAS}$ before $\overline{RAS}$ refresh cycling tRC=min. output open | | | 120 | mA |
| | | M5M416165C-6,-6S | | | | 95 | |
| | | M5M416165C-7,-7S | | | | 85 | |
| ICC8(AV) * | Average supply current from Vcc Extended-refresh cycle (Note 6) | M5M416165C (S) | Stand-by: $\overline{RAS}$≧Vcc-0.2V $\overline{CAS}$≧Vcc-0.2V or $\overline{CAS}$≦0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V A0～A11≦0.2V or ≧Vcc-0.2V DQ=open, tRC=125μs, tRAS=tRASmin～1μs | | | 600 | μA |
| ICC9(AV) * | Average supply current from Vcc Self-refresh cycle | M5M416165C (S) | $\overline{RAS}$=$\overline{CAS}$≦0.2V | | | 400 | μA |

Note 2: Current flowing into an IC is positive, out is negative.
3: ICC1 (AV), ICC3 (AV) and ICC4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: ICC1 (AV) and ICC4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=VIL and $\overline{LCAS}$/$\overline{UCAS}$=VIH.

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**CAPACITANCE** (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{I(A)}$ | Input capacitance, address inputs | $V_I$=Vss<br>f=1MHz<br>$V_I$=25mVrms | | | 5 | pF |
| $C_{I(\overline{OE})}$ | Input capacitance, $\overline{OE}$ input | | | | 7 | pF |
| $C_{I(\overline{W})}$ | Input capacitance, write control input | | | | 7 | pF |
| $C_{I(\overline{RAS})}$ | Input capacitance, $\overline{RAS}$ input | | | | 7 | pF |
| $C_{I(\overline{CAS})}$ | Input capacitance, $\overline{CAS}$ input | | | | 7 | pF |
| $C_{I/O}$ | Input/Output capacitance, data ports | | | | 7 | pF |

**SWITCHING CHARACTERISTICS** (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M416165C-5,-5S | | M5M416165C-6,-6S | | M5M416165C-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CAC}$ | Access time from $\overline{CAS}$ | (Note 7,8) | | 13 | | 15 | | 20 | ns |
| $t_{RAC}$ | Access time from $\overline{RAS}$ | (Note 7,9) | | 50 | | 60 | | 70 | ns |
| $t_{AA}$ | Columu address access time | (Note 7,10) | | 25 | | 30 | | 35 | ns |
| $t_{CPA}$ | Access time from $\overline{CAS}$ precharge | (Note 7,11) | | 30 | | 35 | | 40 | ns |
| $t_{OEA}$ | Access time from $\overline{OE}$ | (Note 7) | | 13 | | 15 | | 20 | ns |
| $t_{OHC}$ | Output hold time from $\overline{CAS}$ | | 5 | | 5 | | 5 | | ns |
| $t_{OHR}$ | Output hold time from $\overline{RAS}$ | (Note 13) | 5 | | 5 | | 5 | | ns |
| $t_{CLZ}$ | Output low impedance time from $\overline{CAS}$ low | (Note 7) | 5 | | 5 | | 5 | | ns |
| $t_{OEZ}$ | Output disable time after $\overline{OE}$ high | (Note 12) | 0 | 13 | 0 | 15 | 0 | 20 | ns |
| $t_{WEZ}$ | Output disable time after $\overline{WE}$ low | (Note 12) | 0 | 13 | 0 | 15 | 0 | 20 | ns |
| $t_{OFF}$ | Output disable time after $\overline{CAS}$ high | (Note 12,13) | 0 | 13 | 0 | 15 | 0 | 20 | ns |
| $t_{REZ}$ | Output disable time after $\overline{RAS}$ high | (Note 12,13) | 0 | 13 | 0 | 15 | 0 | 20 | ns |

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to $V_{OH}$=2.4V($I_{OH}$=-5mA) / $V_{OL}$=0.4V($I_{OL}$=4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V($V_{OH}$) and 0.8V($V_{OL}$).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$. and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by amount that $t_{RCD}$ exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ( $I_{OUT} \leq |\pm 10\,\mu A|$ ) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

PRELIMINARY

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 14,15)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M416165C-5,-5S | | M5M416165C-6,-6S | | M5M416165C-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| tREF | Refresh cycle time | | | 64 | | 64 | | 64 | ms |
| tREF* | Refresh cycle time | | | 128 | | 128 | | 128 | ms |
| tRP | $\overline{RAS}$ high pulse width | | 30 | | 40 | | 50 | | ns |
| tRCD | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low | (Note 16) | 18 | 37 | 20 | 45 | 20 | 50 | ns |
| tCRP | Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low | | 5 | | 5 | | 5 | | ns |
| tRPC | Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low | | 0 | | 0 | | 0 | | ns |
| tCPN | $\overline{CAS}$ high pulse width | | 8 | | 10 | | 10 | | ns |
| tRAD | Column address delay time from $\overline{RAS}$ low | (Note 17) | 13 | 25 | 15 | 30 | 15 | 35 | ns |
| tASR | Row address setup time before $\overline{RAS}$ low | | 0 | | 0 | | 0 | | ns |
| tASC | Column address setup time before $\overline{CAS}$ low | (Note 18) | 0 | 10 | 0 | 13 | 0 | 13 | ns |
| tRAH | Row address hold time after $\overline{RAS}$ low | | 8 | | 10 | | 10 | | ns |
| tCAH | Column address hold time after $\overline{CAS}$ low | | 8 | | 10 | | 10 | | ns |
| tDZC | Delay time, data to $\overline{CAS}$ low | (Note 19) | 0 | | 0 | | 0 | | ns |
| tDZO | Delay time, data to $\overline{OE}$ low | (Note 19) | 0 | | 0 | | 0 | | ns |
| tRDD | Delay time, $\overline{RAS}$ high to data | (Note 20) | 13 | | 15 | | 20 | | ns |
| tCDD | Delay time, $\overline{CAS}$ high to data | (Note 20) | 13 | | 15 | | 20 | | ns |
| tODD | Delay time, $\overline{OE}$ high to data | (Note 20) | 13 | | 15 | | 20 | | ns |
| tT | Transition time | (Note 21) | 1 | 50 | 1 | 50 | 1 | 50 | ns |

Note 14: The timing requirements are assumed tT =2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDD or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

### Read and Refresh Cycles

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | M5M416165C-5,-5S | | M5M416165C-6,-6S | | M5M416165C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| tRC | Read cycle time | 90 | | 110 | | 130 | | ns |
| tRAS | $\overline{RAS}$ low pulse width | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| tCAS | $\overline{CAS}$ low pulse width | 8 | 10000 | 10 | 10000 | 13 | 10000 | ns |
| tCSH | $\overline{CAS}$ hold time after $\overline{RAS}$ low | 40 | | 48 | | 55 | | ns |
| tRSH | $\overline{RAS}$ hold time after $\overline{CAS}$ low | 13 | | 15 | | 20 | | ns |
| tRCS | Read setup time before $\overline{CAS}$ low | 0 | | 0 | | 0 | | ns |
| tRCH | Read hold time after $\overline{CAS}$ high (Note 22) | 0 | | 0 | | 0 | | ns |
| tRRH | Read hold time after $\overline{RAS}$ high (Note 22) | 10 | | 10 | | 10 | | ns |
| tRAL | Column address to $\overline{RAS}$ hold time | 25 | | 30 | | 35 | | ns |
| tCAL | Column address to $\overline{CAS}$ hold time | 13 | | 18 | | 23 | | ns |
| tORH | $\overline{RAS}$ hold time after $\overline{OE}$ low | 13 | | 15 | | 20 | | ns |
| tOCH | $\overline{CAS}$ hold time after $\overline{OE}$ low | 13 | | 15 | | 20 | | ns |

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

### Write Cycle (Early Write and Delayed Write)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M416165C-5,-5S | | M5M416165C-6,-6S | | M5M416165C-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| tWC | Write cycle time | | 90 | | 110 | | 130 | | ns |
| tRAS | $\overline{RAS}$ low pulse width | | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| tCAS | $\overline{CAS}$ low pulse width | | 8 | 10000 | 10 | 10000 | 13 | 10000 | ns |
| tCSH | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | 40 | | 48 | | 55 | | ns |
| tRSH | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | 13 | | 15 | | 20 | | ns |
| tWCS | Write setup time before $\overline{CAS}$ low | (Note 24) | 0 | | 0 | | 0 | | ns |
| tWCH | Write hold time after $\overline{CAS}$ low | | 8 | | 10 | | 13 | | ns |
| tCWL | $\overline{CAS}$ hold time after $\overline{W}$ low | | 8 | | 10 | | 13 | | ns |
| tRWL | $\overline{RAS}$ hold time after $\overline{W}$ low | | 8 | | 10 | | 13 | | ns |
| tWP | Write pulse width | | 8 | | 10 | | 13 | | ns |
| tDS | Data setup time before $\overline{CAS}$ low or $\overline{W}$ low | | 0 | | 0 | | 0 | | ns |
| tDH | Data hold time after $\overline{CAS}$ low or $\overline{W}$ low | | 8 | | 10 | | 13 | | ns |

### Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M416165C-5,-5S | | M5M416165C-6,-6S | | M5M416165C-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| tRWC | Read write/read modify write cycle time | (Note 23) | 109 | | 133 | | 161 | | ns |
| tRAS | $\overline{RAS}$ low pulse width | | 75 | 10000 | 89 | 10000 | 107 | 10000 | ns |
| tCAS | $\overline{CAS}$ low pulse width | | 38 | 10000 | 44 | 10000 | 57 | 10000 | ns |
| tCSH | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | 70 | | 82 | | 99 | | ns |
| tRSH | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | 38 | | 44 | | 57 | | ns |
| tRCS | Read setup time before $\overline{CAS}$ low | | 0 | | 0 | | 0 | | ns |
| tCWD | Delay time, $\overline{CAS}$ low to $\overline{W}$ low | (Note 24) | 28 | | 32 | | 42 | | ns |
| tRWD | Delay time, $\overline{RAS}$ low to $\overline{W}$ low | (Note 24) | 65 | | 77 | | 92 | | ns |
| tAWD | Delay time, address to $\overline{W}$ low | (Note 24) | 40 | | 47 | | 57 | | ns |
| tOEH | $\overline{OE}$ hold time after $\overline{W}$ low | | 13 | | 15 | | 20 | | ns |

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD(min), tAWD≧tAWD(min) and tCPWD≧ tCPWD(min) (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

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Notice: This is not a final specification
Some parametric limits are subject to change

### Hyper page Mode Cycle
### (Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | M5M416165C-5,-5S | | M5M416165C-6,-6S | | M5M416165C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{HPC}$ | Hyper page mode read/write cycle time | 20 | | 25 | | 30 | | ns |
| $t_{HPRWC}$ | Hyper page mode read write/read modify write cycle time | 57 | | 66 | | 79 | | ns |
| $t_{DOH}$ | Output hold time from $\overline{CAS}$ low | 5 | | 5 | | 5 | | ns |
| $t_{RAS}$ | $\overline{RAS}$ low pulse width for read write cycle (Note 26) | 65 | 100000 | 77 | 100000 | 92 | 100000 | ns |
| $t_{CP}$ | $\overline{CAS}$ high pulse width (Note 27) | 8 | 13 | 10 | 16 | 10 | 16 | ns |
| $t_{CPRH}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ precharge | 30 | | 35 | | 40 | | ns |
| $t_{CPWD}$ | Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24) | 45 | | 52 | | 62 | | ns |
| $t_{CHOL}$ | Hold time to maintain the data Hi-Z until $\overline{CAS}$ access | 7 | | 7 | | 7 | | ns |
| $t_{OEPE}$ | $\overline{OE}$ Pulse width (Hi-Z control) | 7 | | 7 | | 7 | | ns |
| $t_{WPE}$ | $\overline{W}$ Pulse width (Hi-Z control) | 7 | | 7 | | 7 | | ns |
| $t_{HCWD}$ | Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read | 28 | | 32 | | 42 | | ns |
| $t_{HAWD}$ | Delay time, address to $\overline{W}$ low after read | 52 | | 62 | | 72 | | ns |
| $t_{HPWD}$ | Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read | 62 | | 72 | | 82 | | ns |
| $t_{HCOD}$ | Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read | 13 | | 15 | | 20 | | ns |
| $t_{HAOD}$ | Delay time, address to $\overline{OE}$ high after read | 25 | | 30 | | 35 | | ns |
| $t_{HPOD}$ | Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read | 30 | | 35 | | 40 | | ns |

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
27: $t_{CP(max)}$ is specified as a reference point only.

### $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | M5M416165C-5,-5S | | M5M416165C-6,-6S | | M5M416165C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{CSR}$ | $\overline{CAS}$ setup time before $\overline{RAS}$ low | 5 | | 5 | | 5 | | ns |
| $t_{CHR}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | 10 | | 10 | | 15 | | ns |

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

PRELIMINARY

## SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

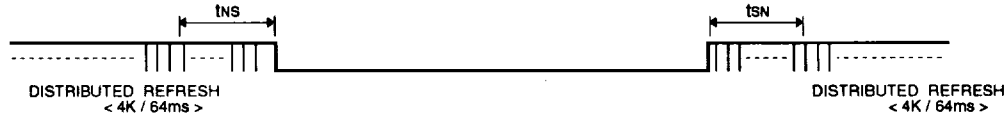
**TIMING REQUIREMENTS** (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | M5M416165C-5S | | M5M416165C-6S | | M5M416165C-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{RASS}$ | Self refresh $\overline{RAS}$ low pulse width | 100 | | 100 | | 100 | | μs |
| $t_{RPS}$ | Self refresh $\overline{RAS}$ high precharge time | 90 | | 110 | | 130 | | ns |
| $t_{CHS}$ | Self refresh $\overline{RAS}$ hold time | - 50 | | - 50 | | - 50 | | ns |

## SELF REFRESH ENTRY & EXIT CONDITIONS

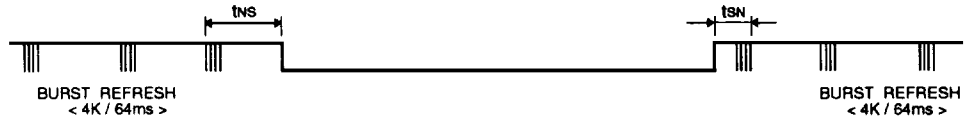
**(1) In case of distributed refresh**

The last / first full refresh cycles (4K) must be made within $t_{NS}$ / $t_{SN}$ before / after self refresh, on the condition of $t_{NS} \leqq 64ms$ and $t_{SN} \leqq 64ms$.



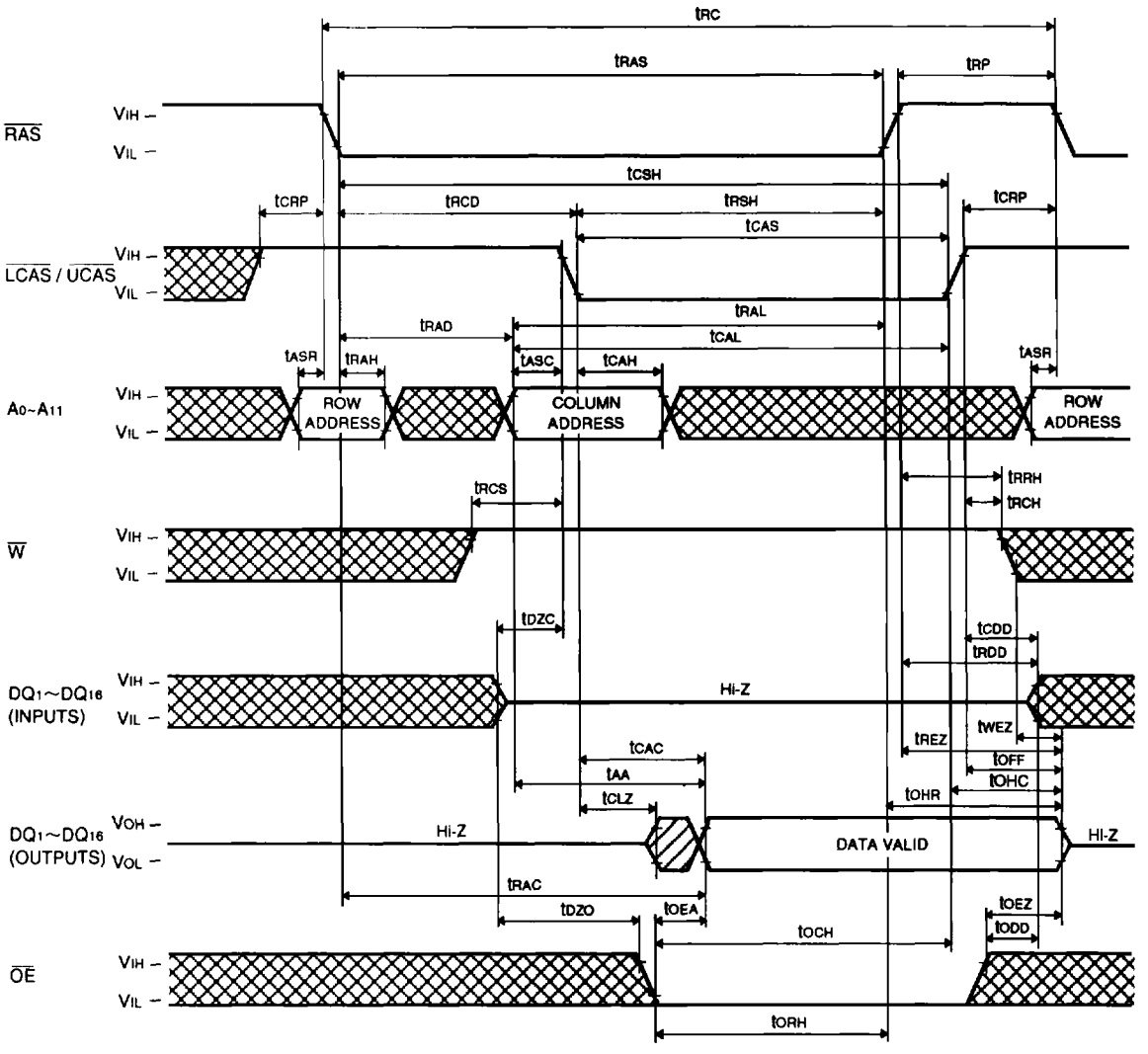

**(2) In case of burst refresh**

The last / first full refresh cycles (4K) must be made within $t_{NS}$ / $t_{SN}$ before / after self refresh, on the condition of $t_{NS} + t_{SN} \leqq 64ms$.



**Timing Diagrams** (Note 29)

**Read Cycle**



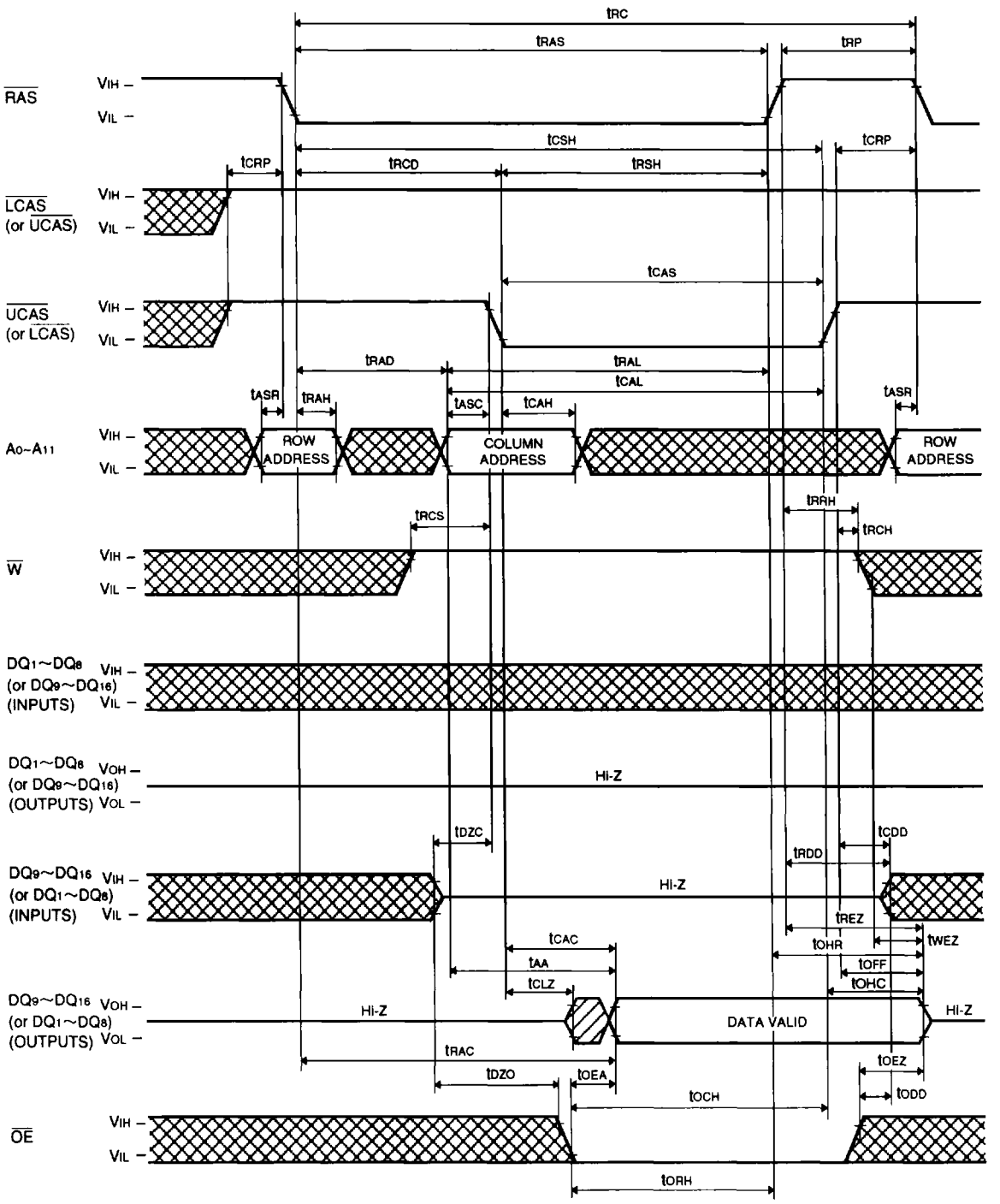

Note 29

Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

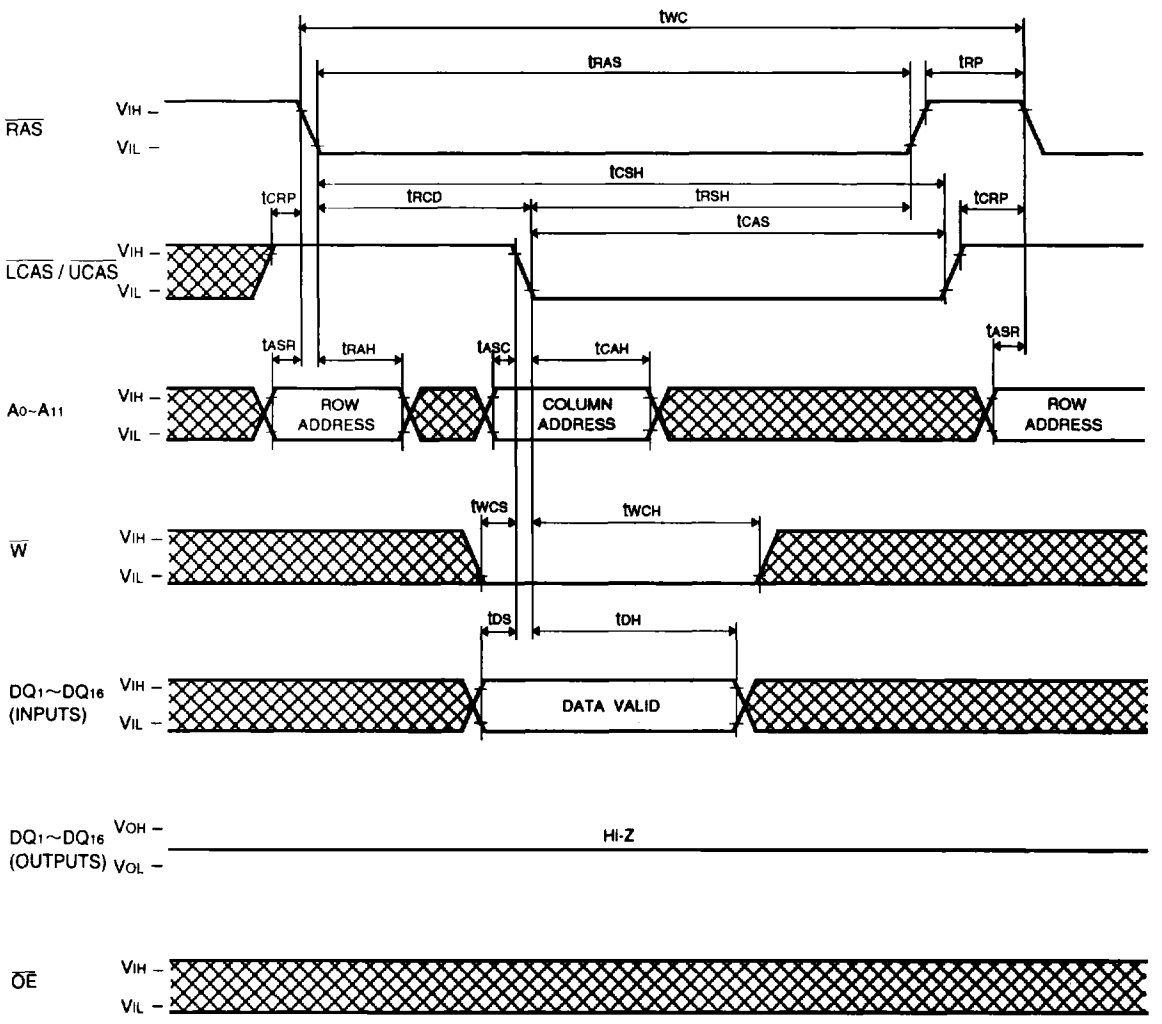
Indicates the invalid output.

PRELIMINARY

**Byte Read Cycle**

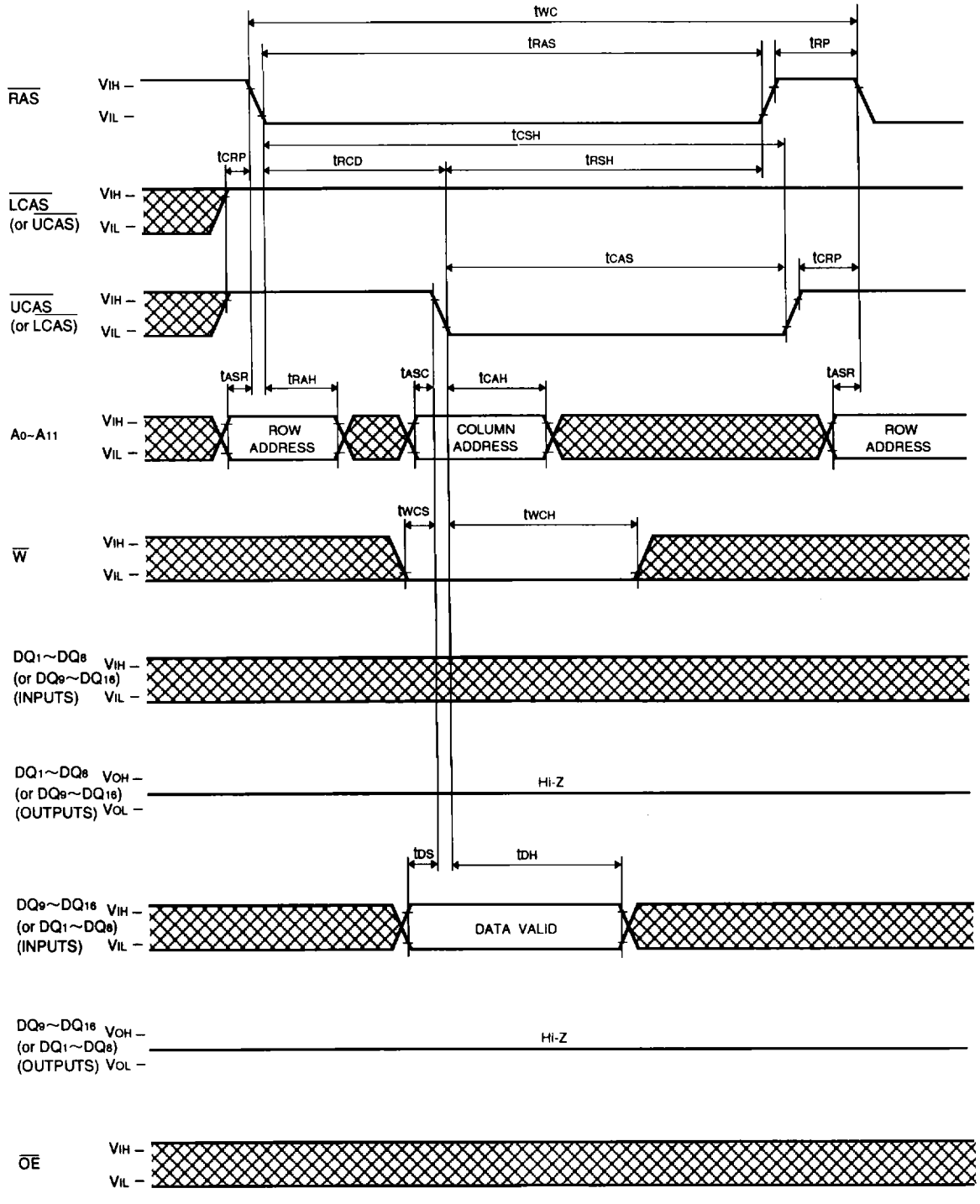


**Early Write Cycle**

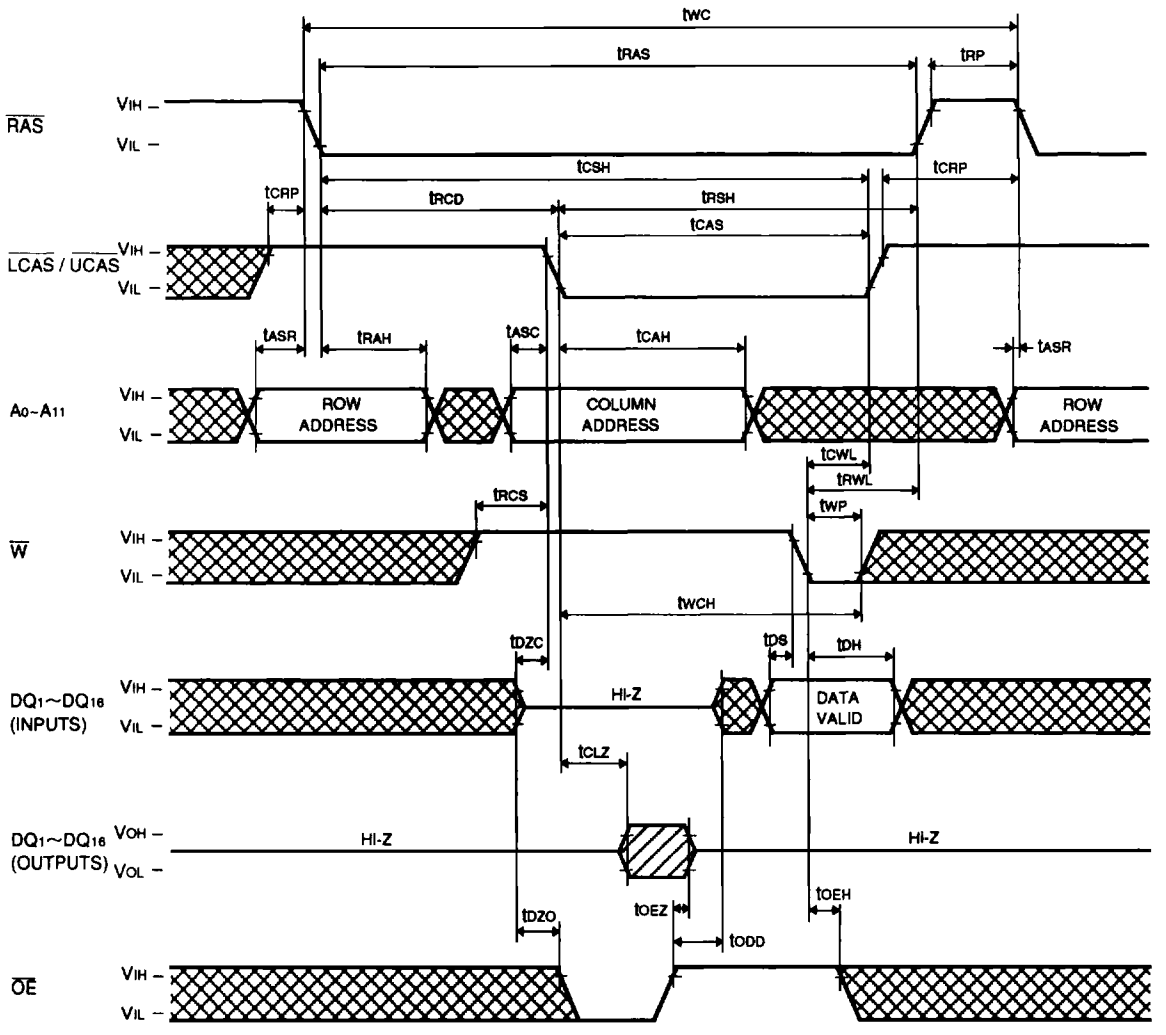


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

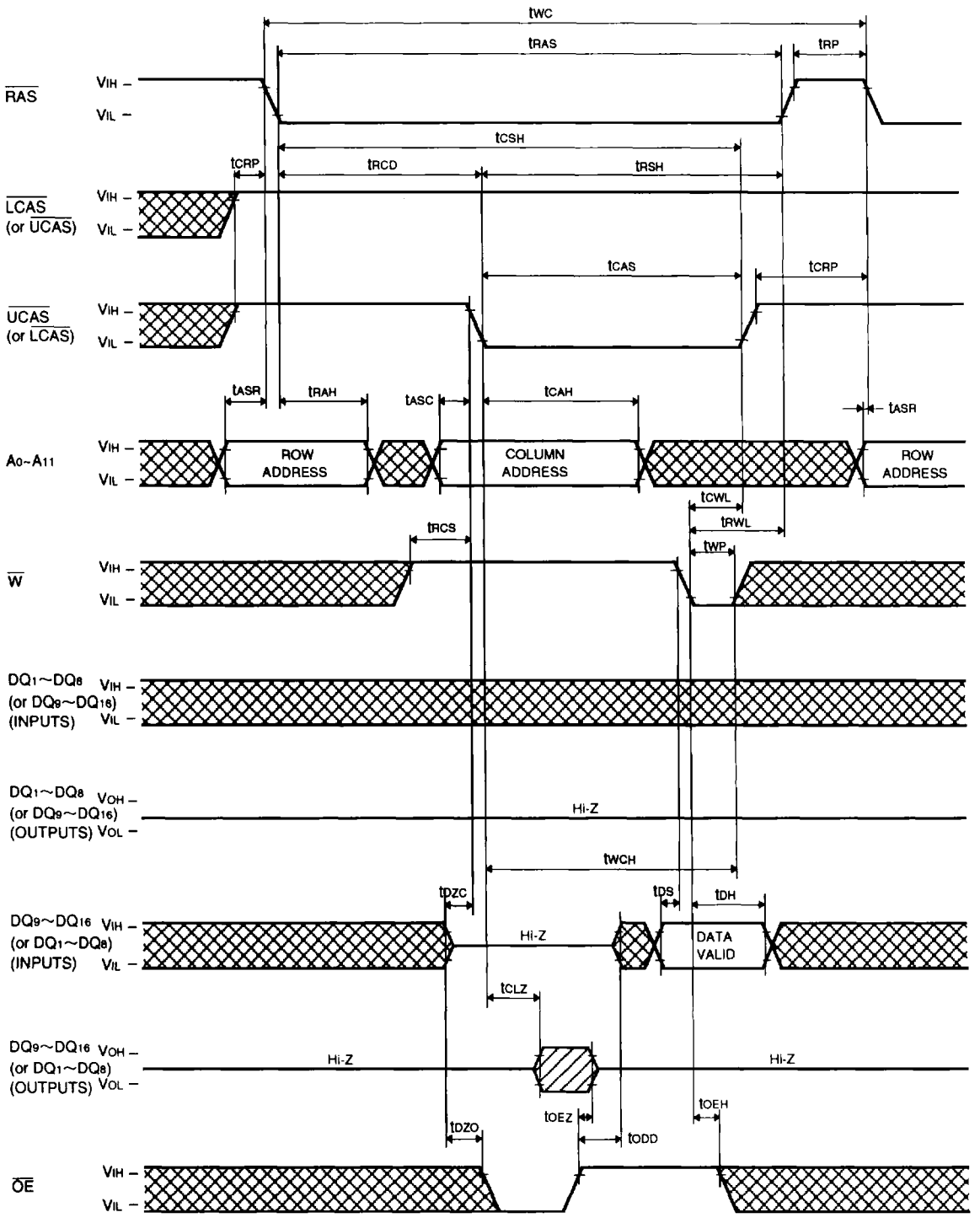
**Byte Early Write Cycle**



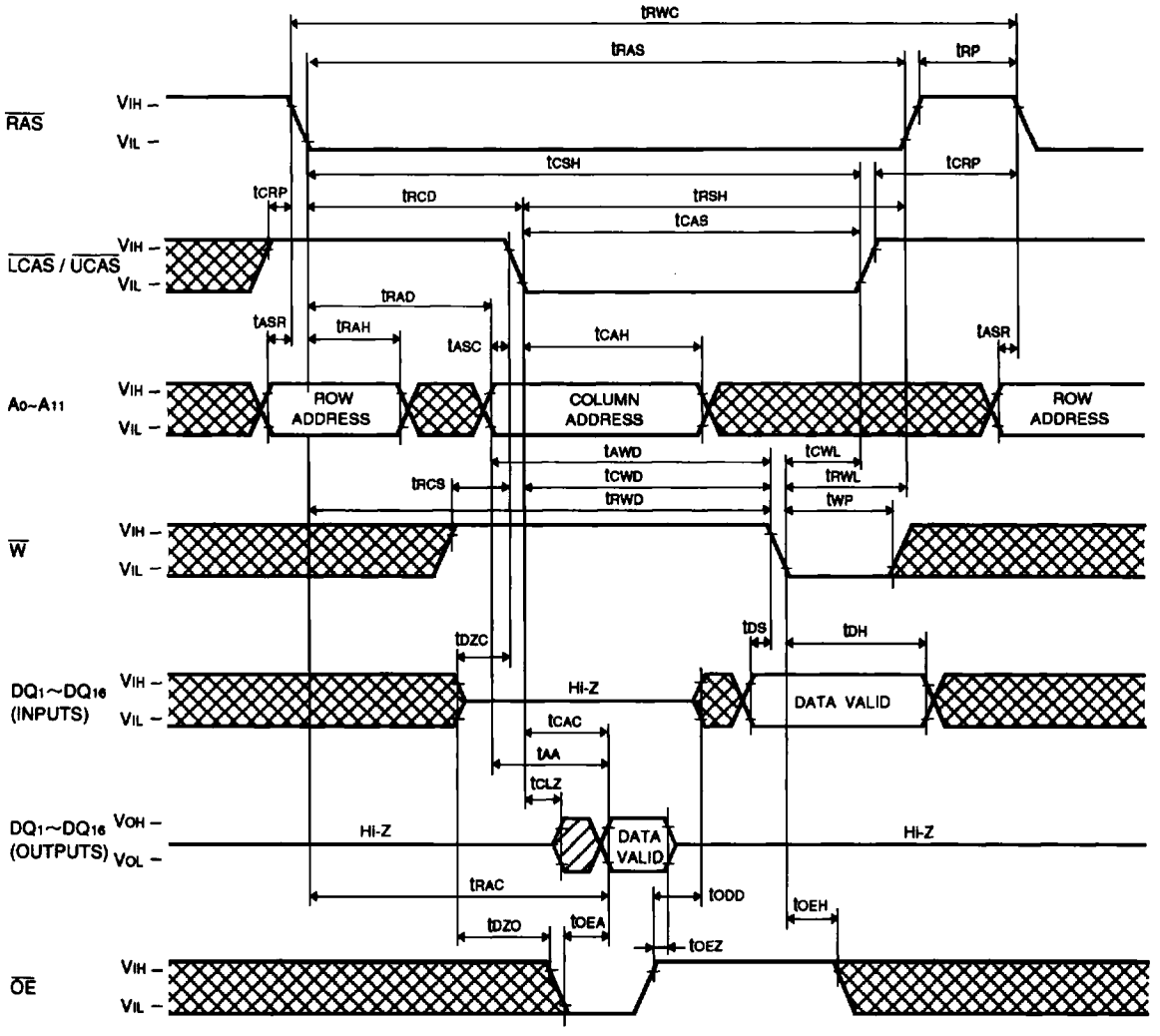
**Delayed Write Cycle**



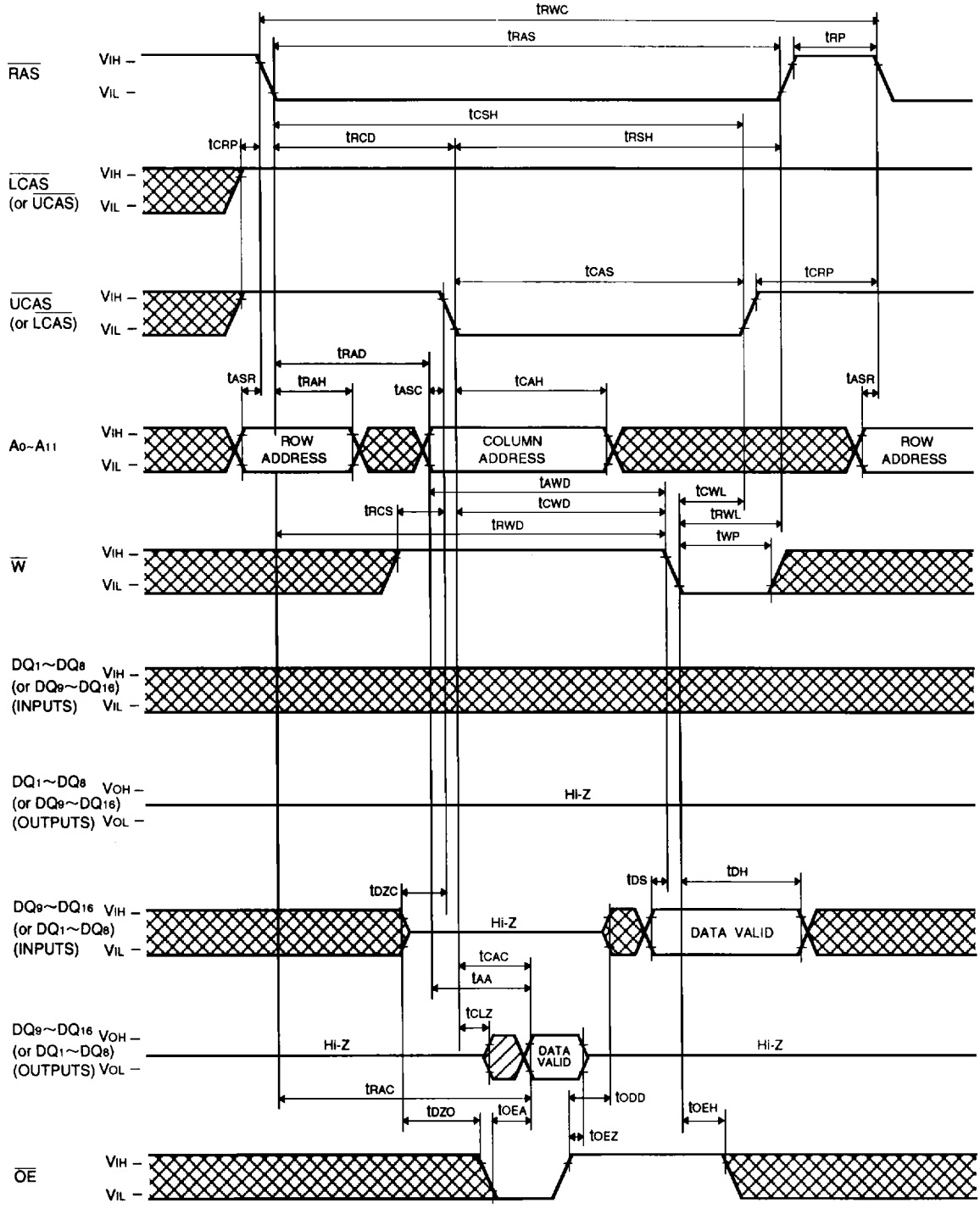
**Byte Delayed Write Cycle**



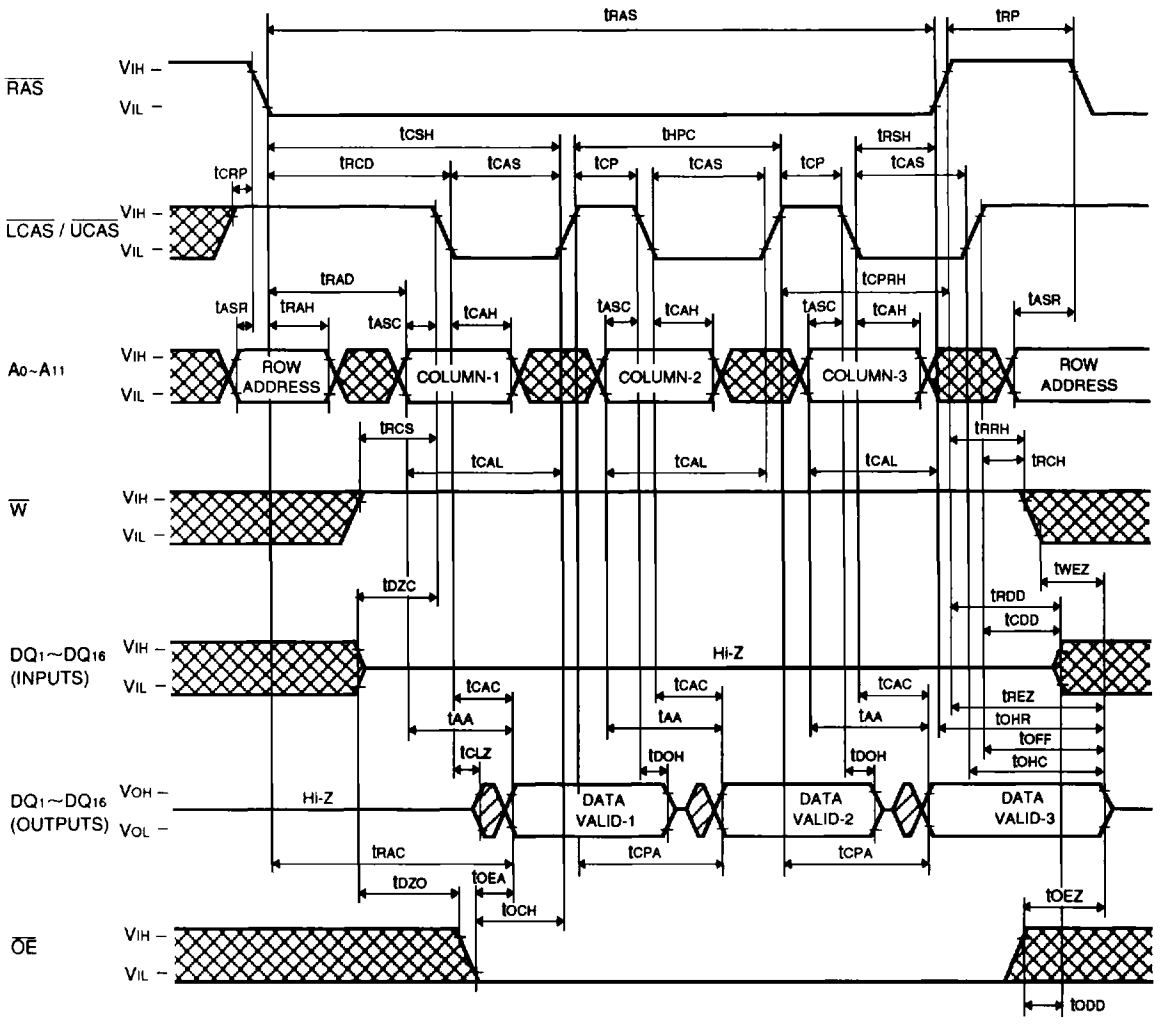
**Read-Write, Read-Modify-Write Cycle**



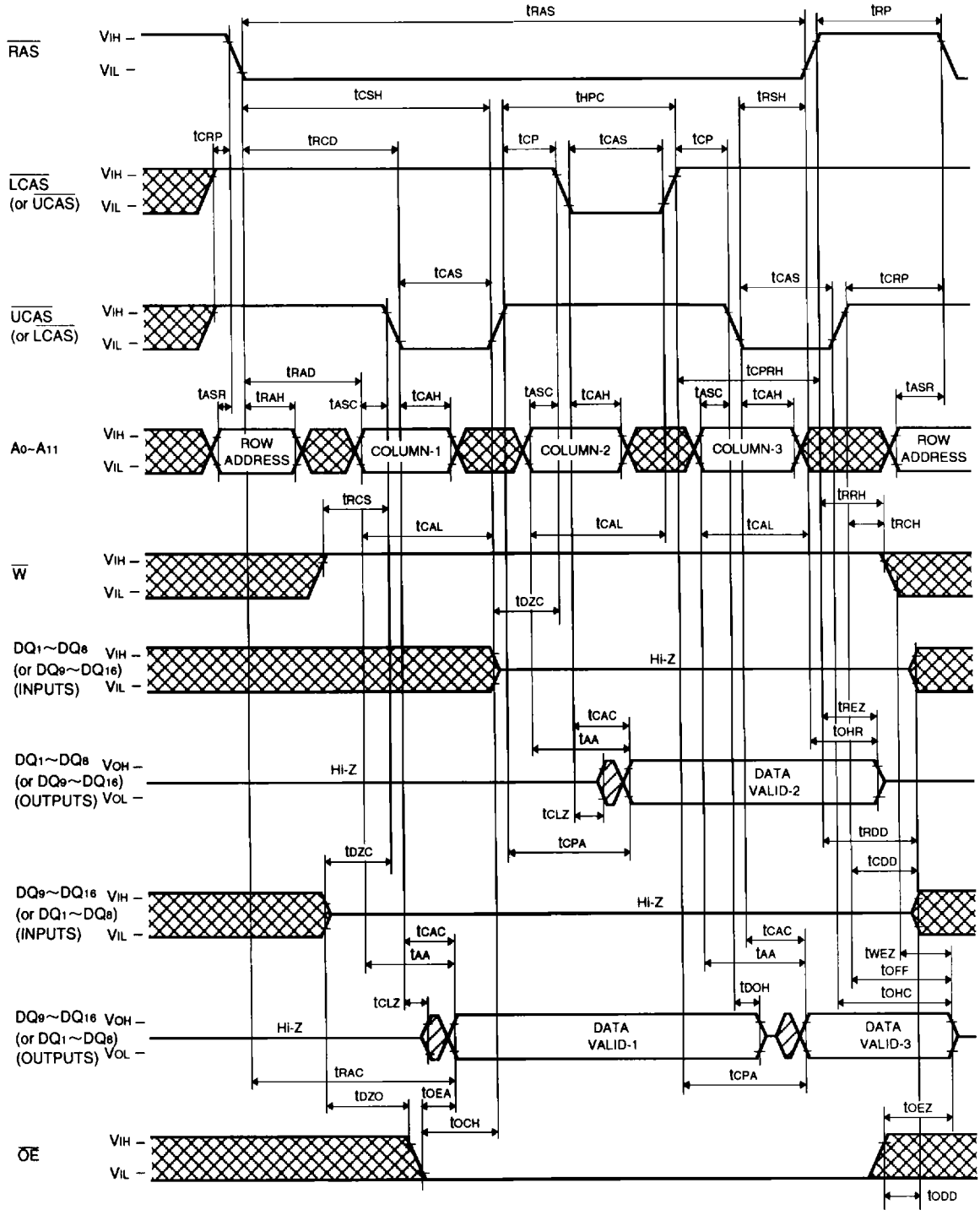
**Byte Read-Write, Read-Modify-Write Cycle**



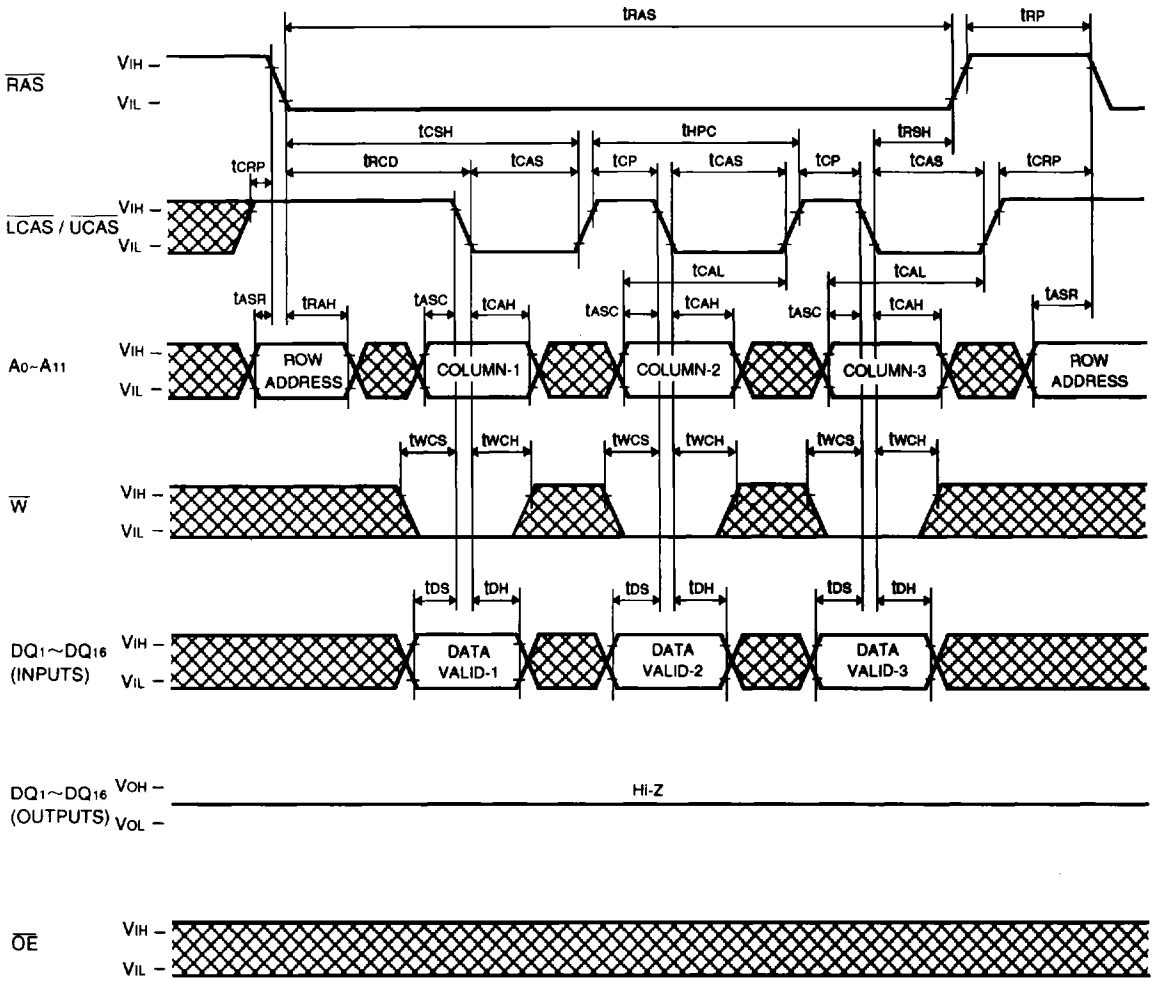
**Hyper Page Mode Read Cycle**



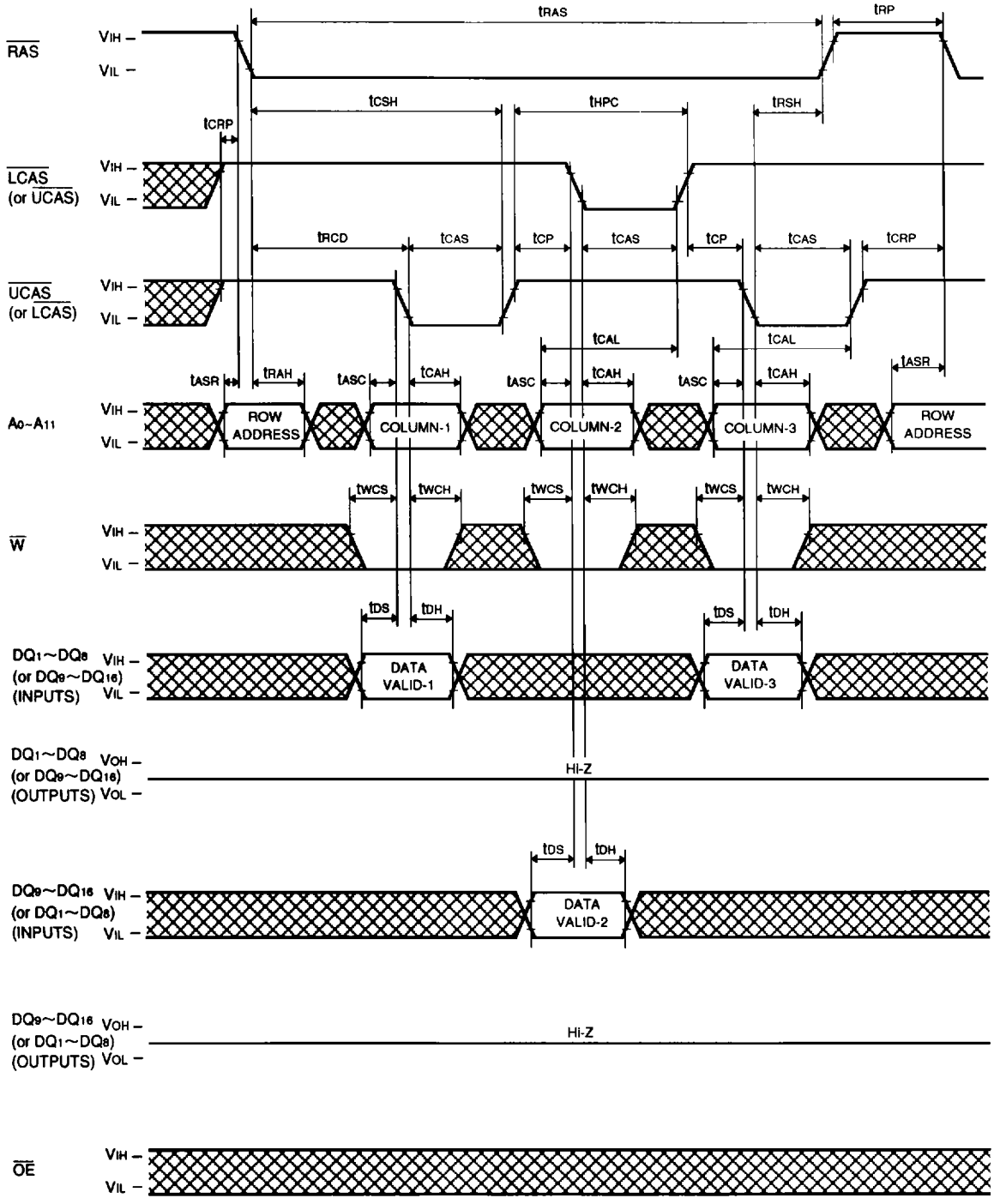
**Hyper Page Mode Byte Read Cycle**



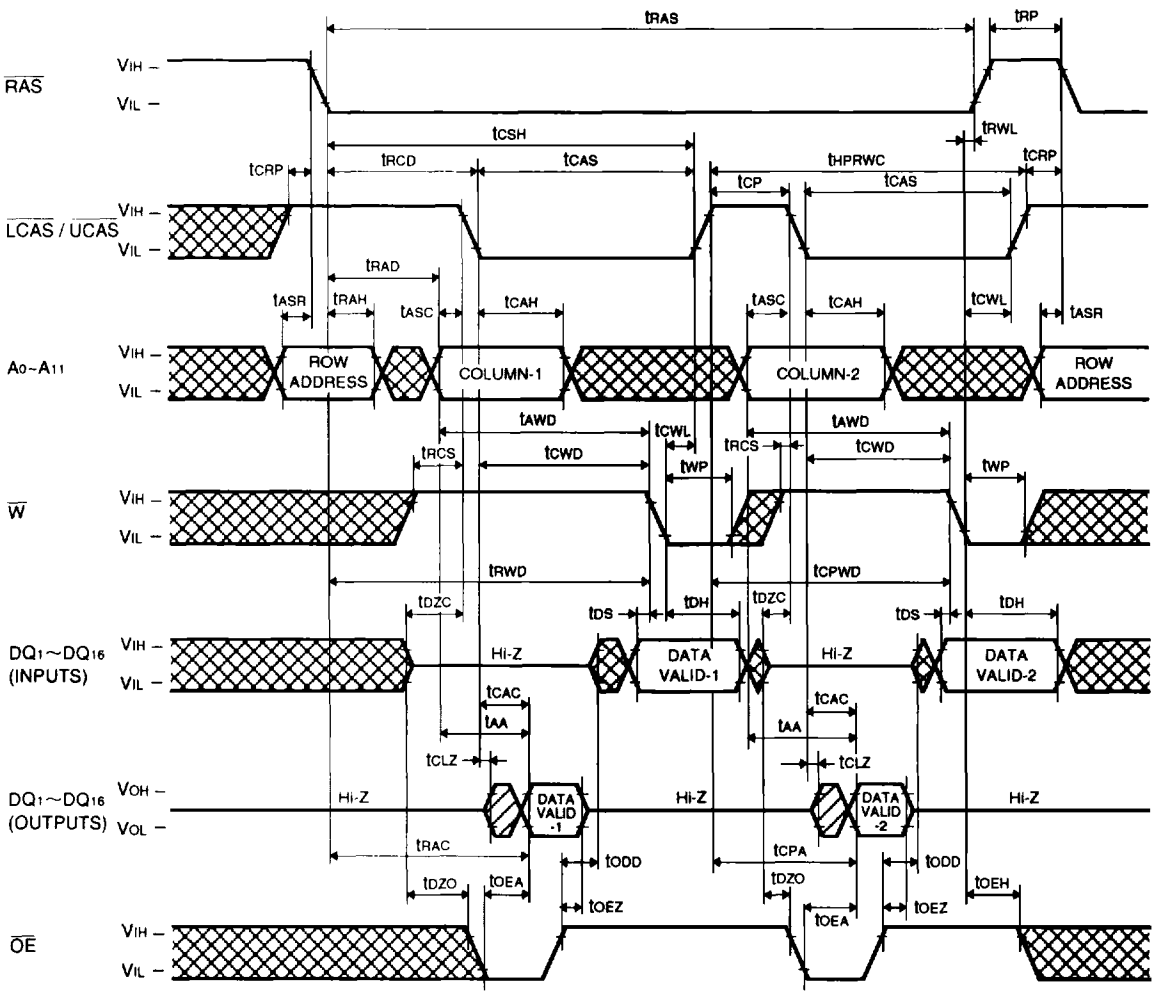
**Hyper Page Mode Early Write Cycle**



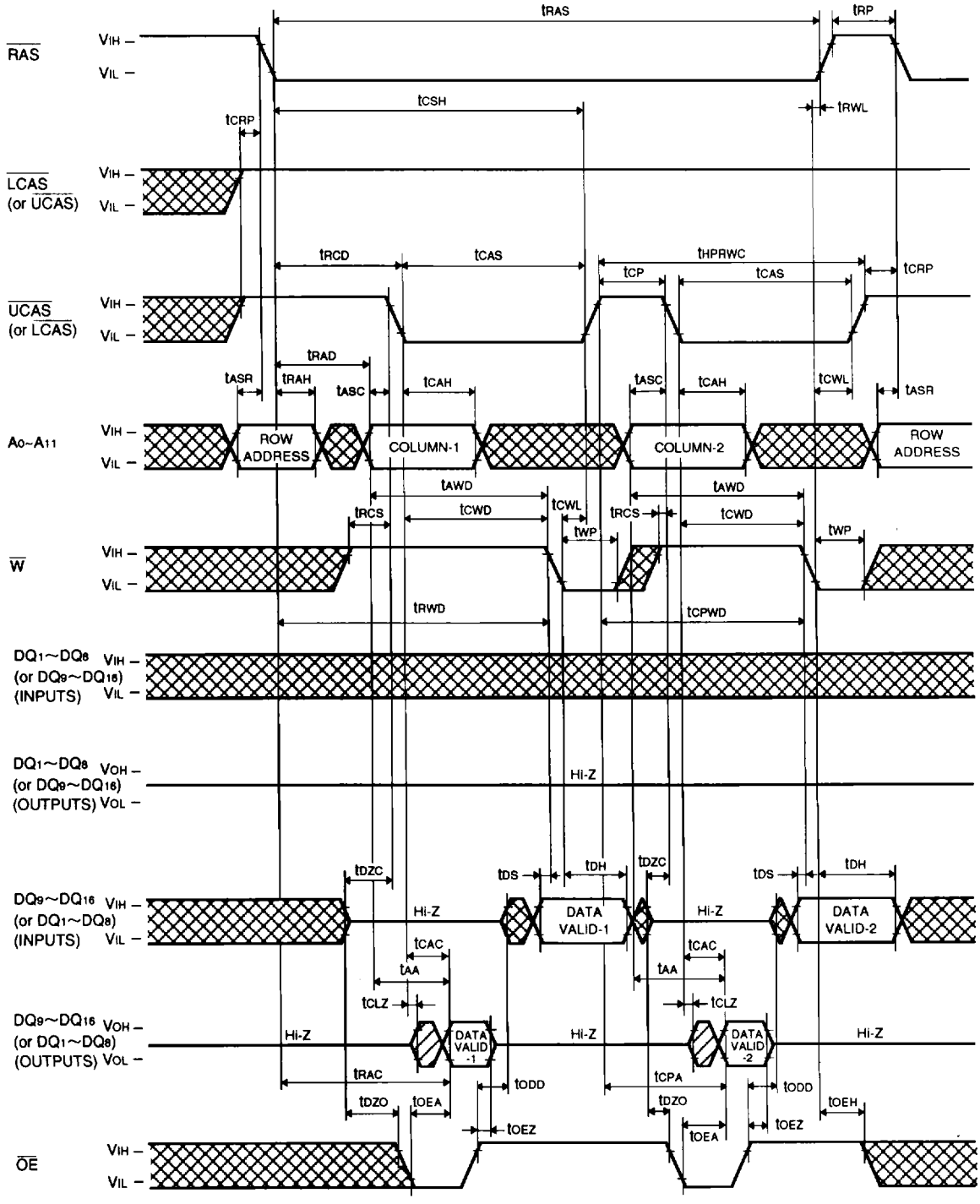
**Hyper Page Mode Byte Early Write Cycle**



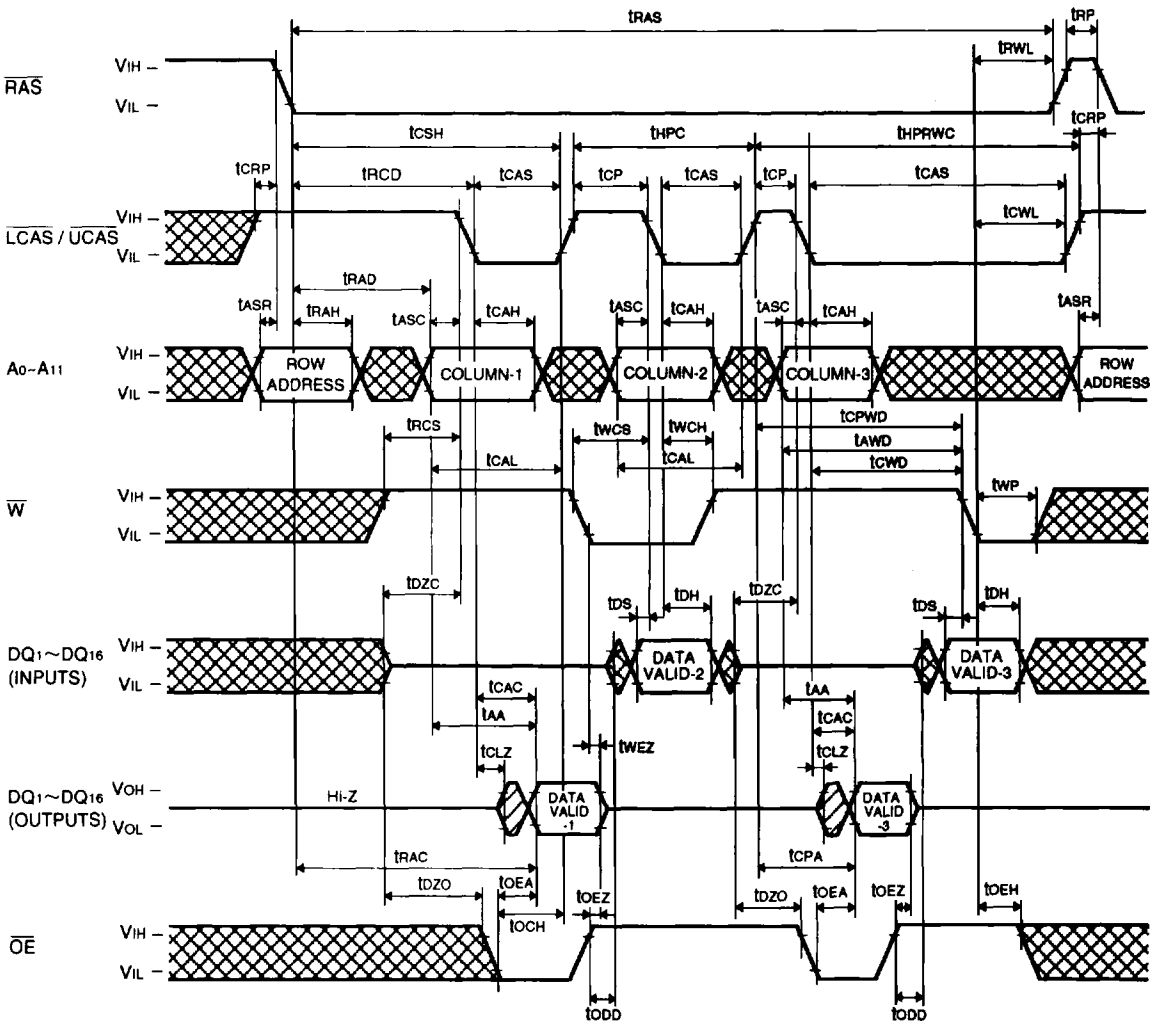
**Hyper Page Mode Read-Write, Read-Modify-Write Cycle**



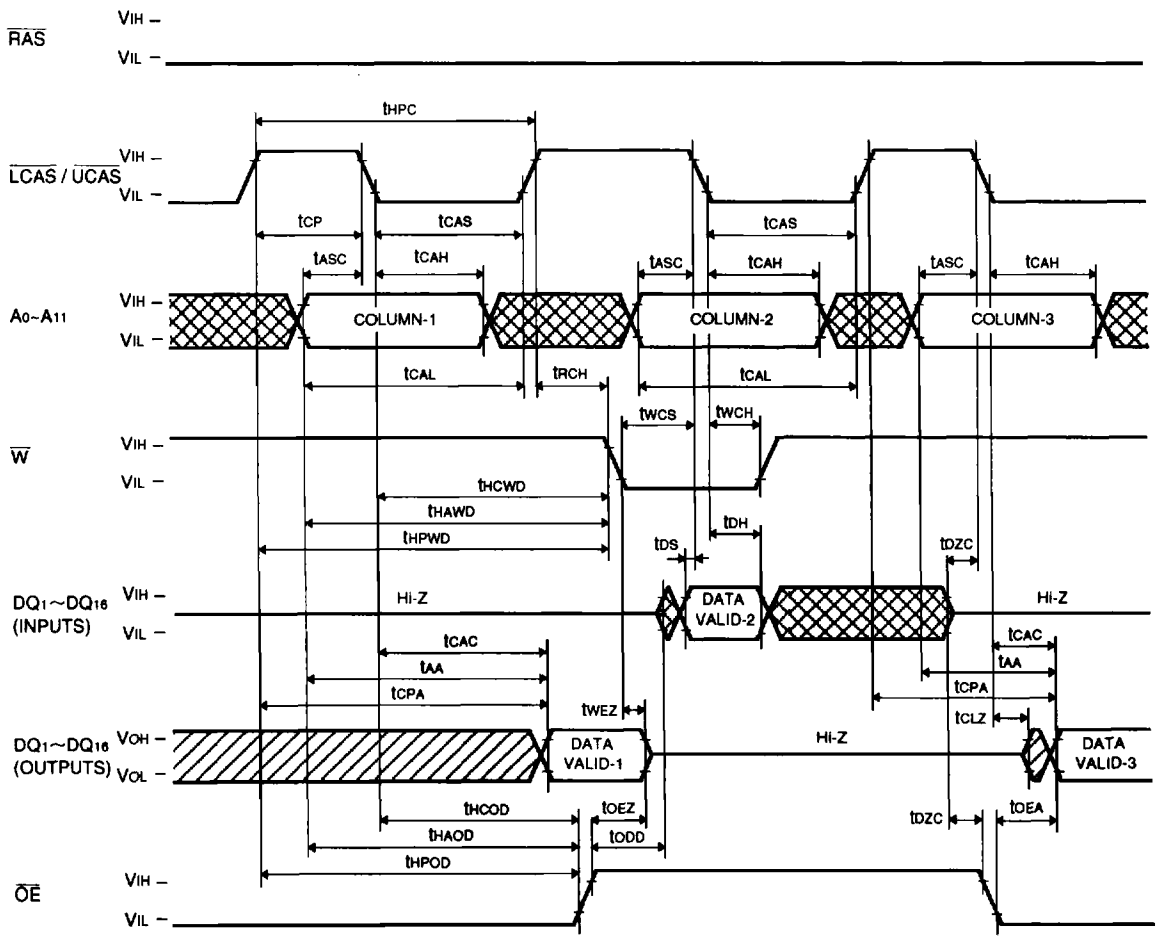
**Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle**



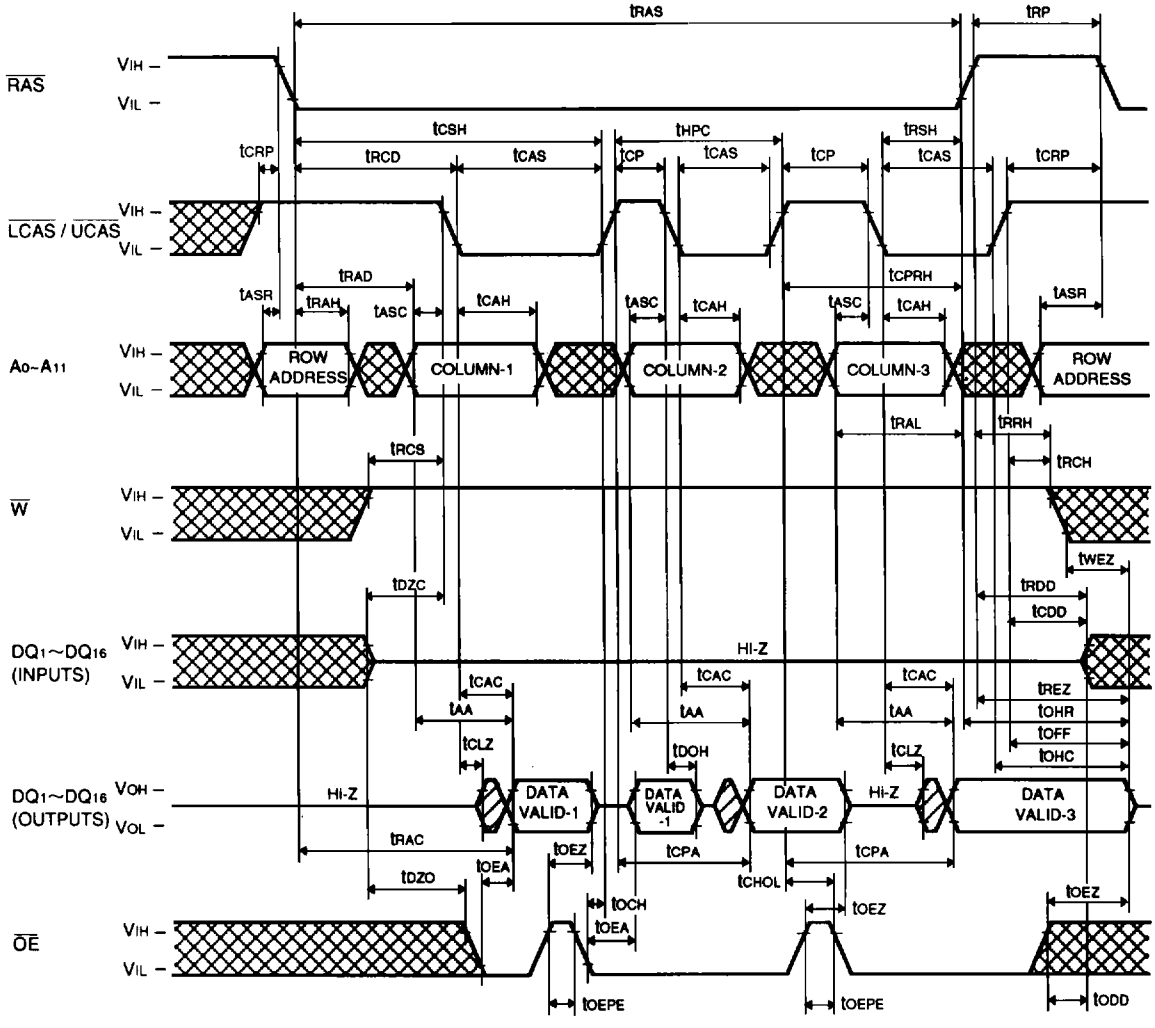
**Hyper Page Mode Mix Cycle (1)**



**Hyper Page Mode Mix Cycle (2)**



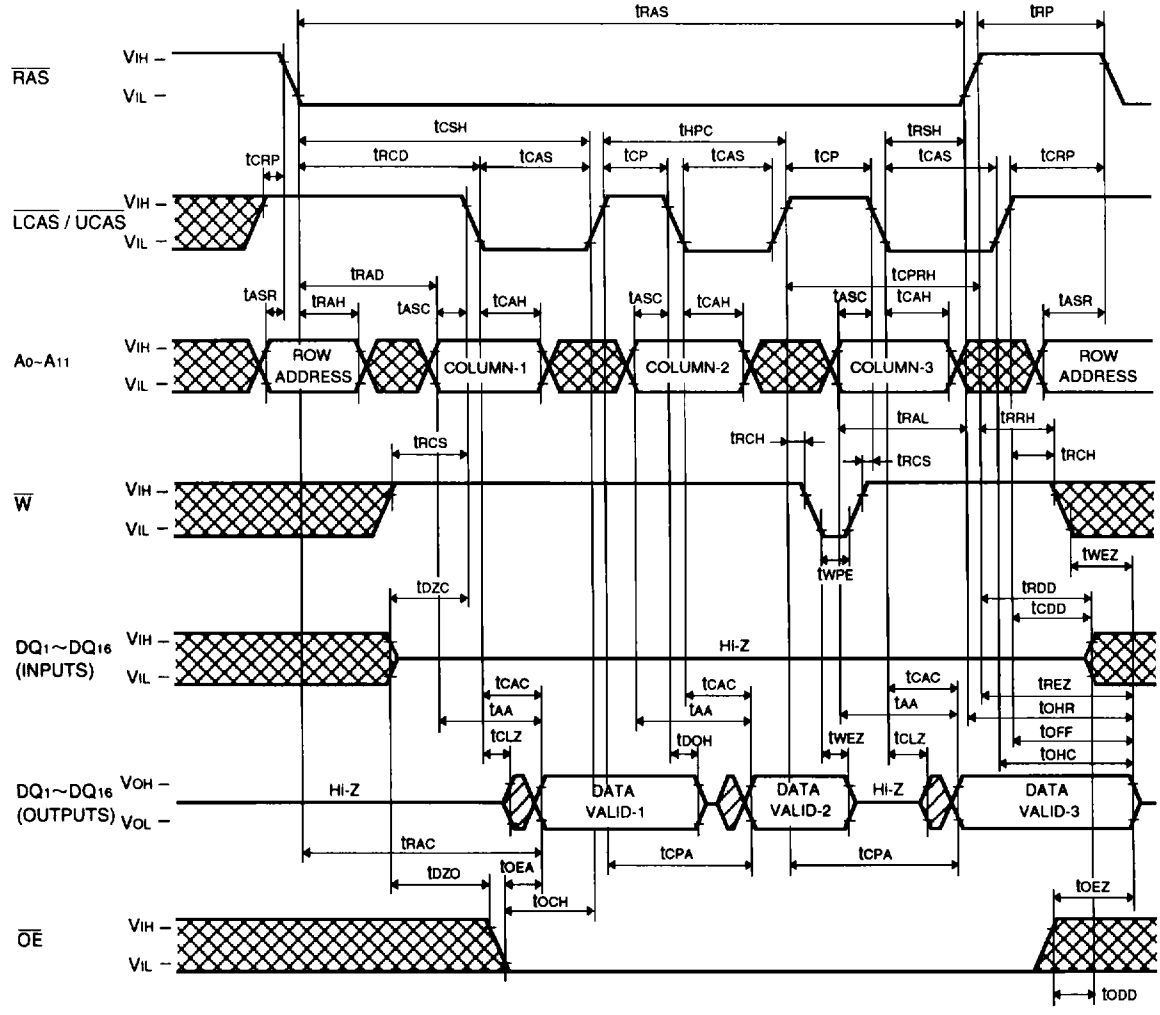
**Hyper Page Mode Read Cycle ( Hi-Z control by $\overline{OE}$ )**



PRELIMINARY

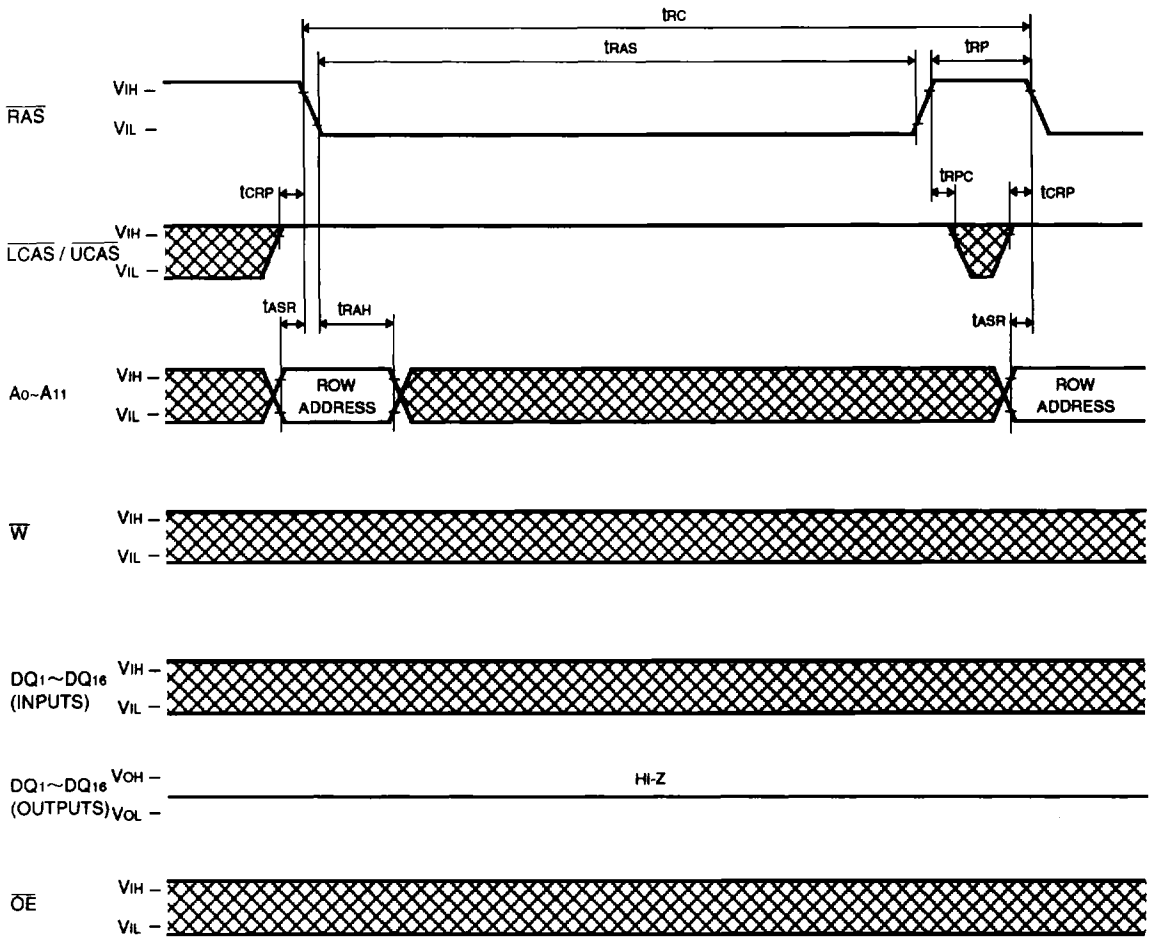
Notice: This is not a final specification
Some parameters are subject to change

**Hyper Page Mode Read Cycle ( HI-Z control by $\overline{W}$ )**



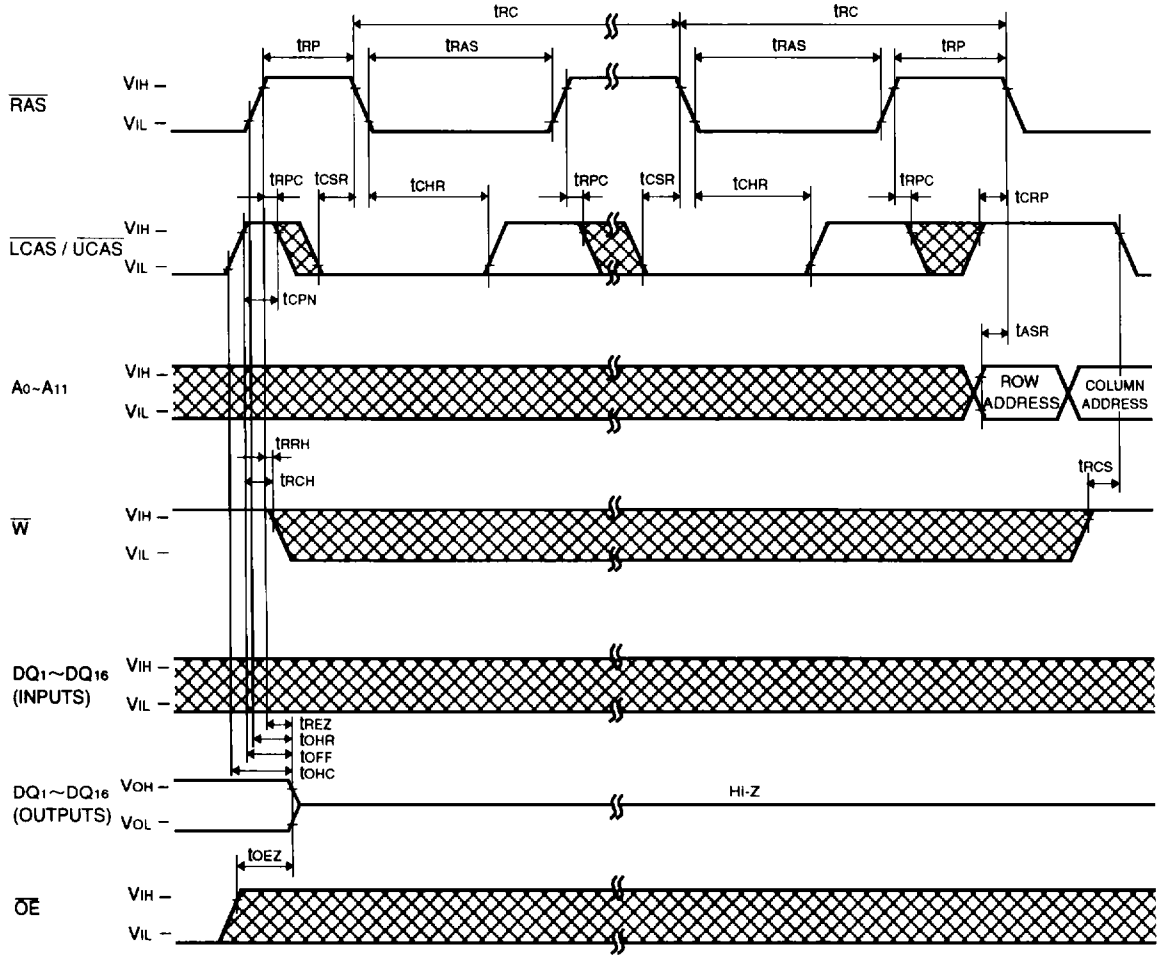
PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

## $\overline{RAS}$-only Refresh Cycle



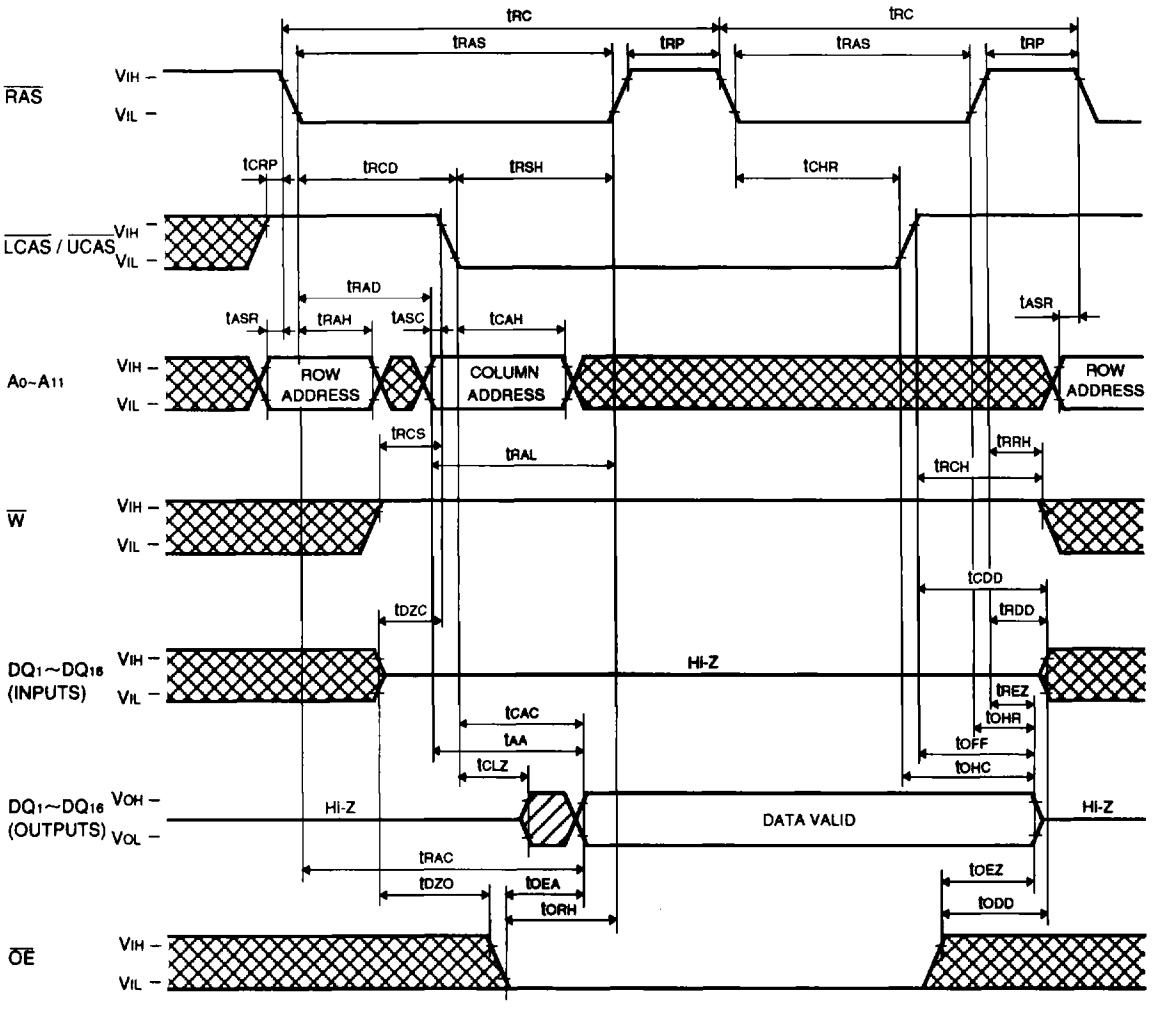
PRELIMINARY

**$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle***



PRELIMINARY
Notice: This is not a final specification
Some parameter limits are subject to change

**Hidden Refresh Cycle (Read)** (Note 30)

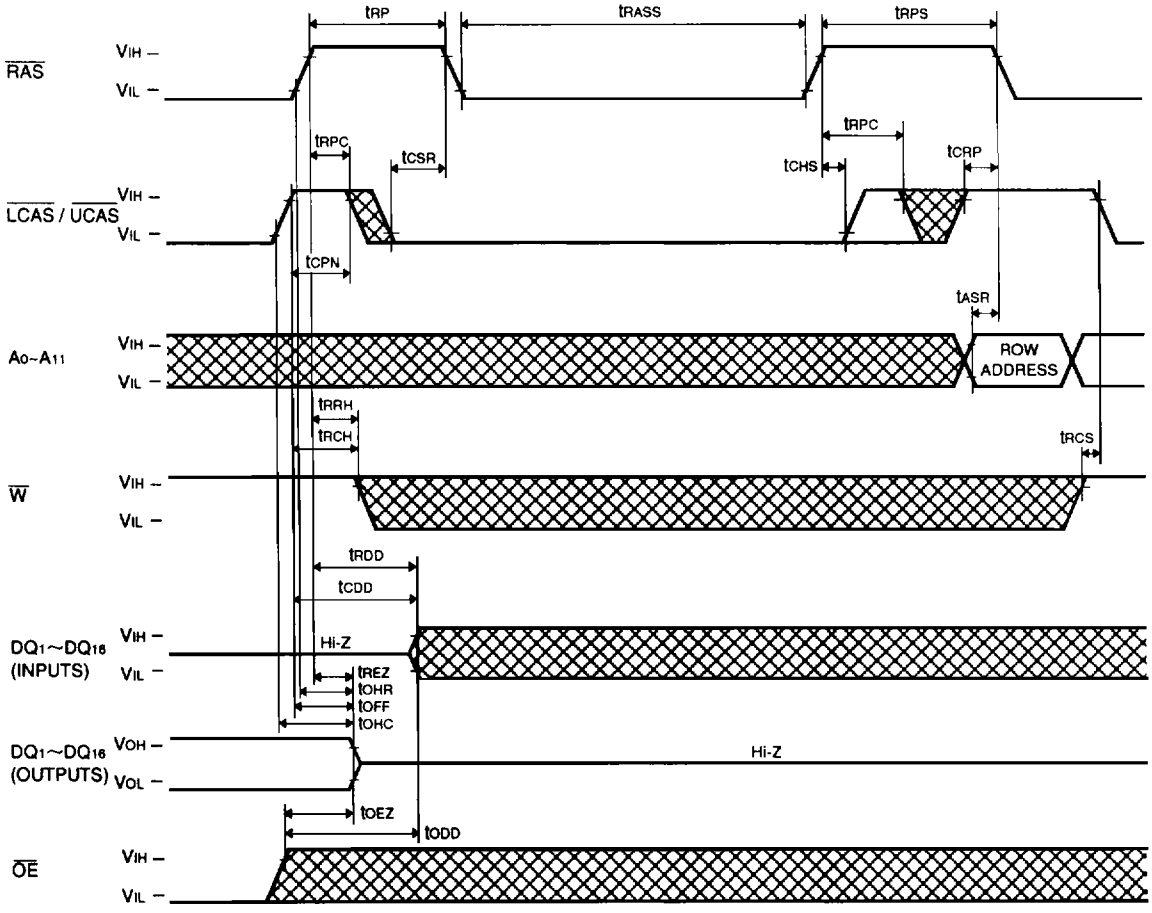
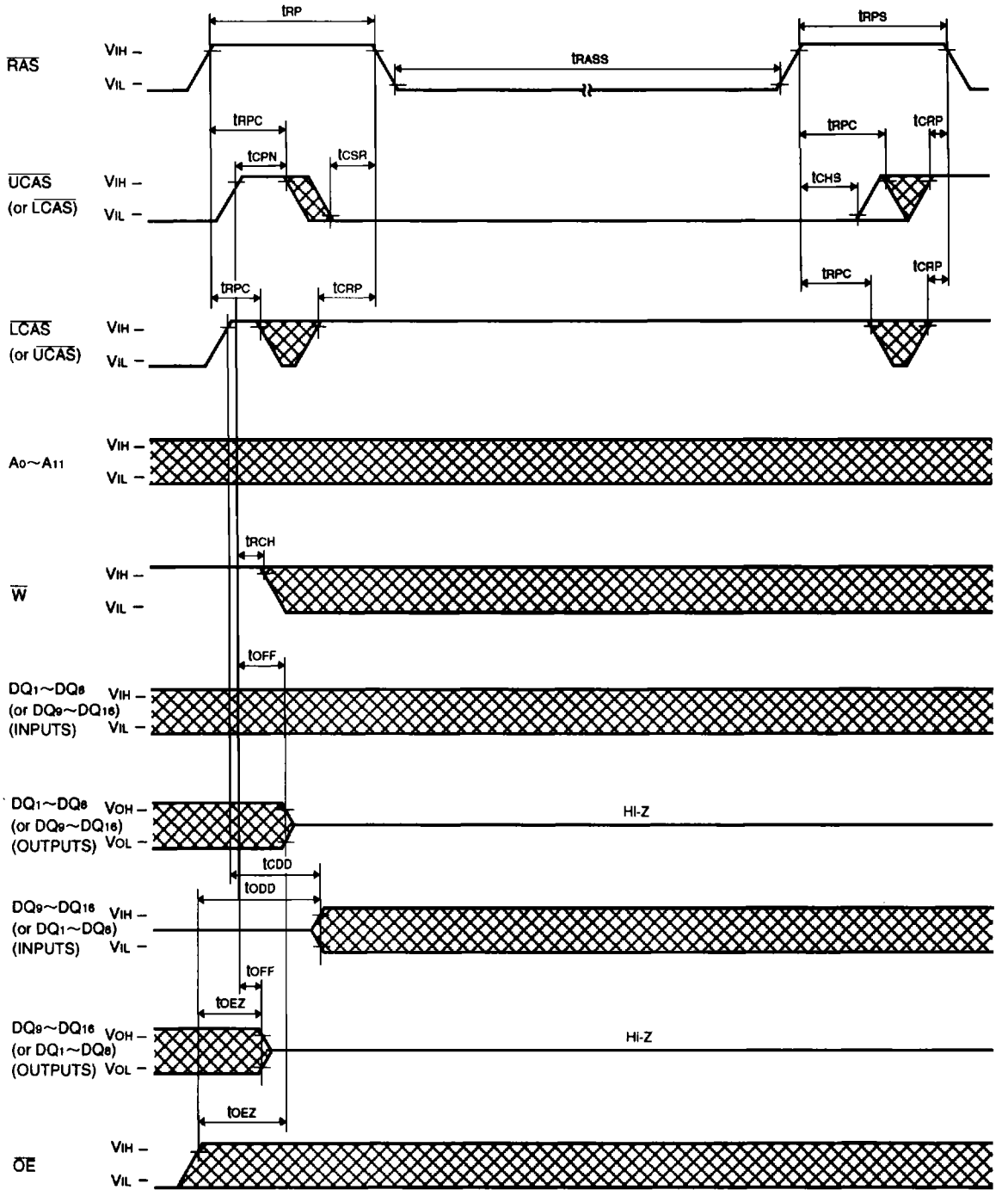



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

PRELIMINARY

Notice: This is not a final specification.
Some parameters are subject to change.

**Self Refresh Cycle ***



**Upper / (Lower) Self Refresh Cycle***