

# MULTILEVEL PIPELINE REGISTER

#### **KEY FEATURES**

- Four 8-Bit Registers
- Contents of Each Register Available at Output
- 24-Pin 300 Mil Package

- Dual Two Stage or Single Four Stage Push Only Stack Operation
- Hold, Transfer and Load Instructions
- High Performance CMOS
- TTL Compatible

#### GENERAL DESCRIPTION

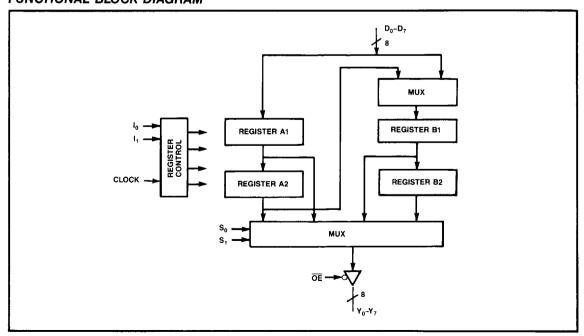
The WS59520 and WS59521 are CMOS drop-in replacements for the bipolar AM29520 and AM29521 devices offered by Advanced Micro Devices. The high performance CMOS process with which these products are manufactured enables them to operate at bipolar speeds while consuming one tenth the power of the bipolar circuits.

The WS59520/521 consists of four 8-bit registers which can be configured as a single four level pipeline or two dual level pipelines. The architectural configuration is determined by the instruction inputs ( $I_0$  and  $I_1$ ).

Each of the four registers contents is available at the multiplexed output. The register to be used as the output register is determined by the control inputs  $(S_0 \text{ and } S_1)$ . The output is 8-bits wide and is enabled by the  $\overline{OE}$  input.

The WS59520 and WS59521 differ only in the dual two level stack mode of operation.

#### FUNCTIONAL BLOCK DIAGRAM



## **ABSOLUTE MAXIMUM RATINGS\***

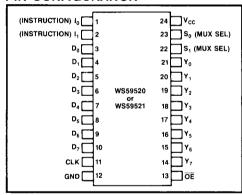
Operating Temp (Comm'l) 0 °C to + 70 °C
(Mil) 55°C to + 125°C
Storage Temp. (No bias) $-65$ °C to $+150$ °C
Voltage on any pin with
respect to GND 0.6V to + 7V
Latch Up Protection >200 mA

\* Notice: Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may effect device reliability.

#### PIN DESCRIPTION

SIGNAL NAME	1/0	DESCRIPTION			
D <sub>0</sub> -D <sub>7</sub>	ŀ	Data input port			
Y <sub>0</sub> -Y <sub>7</sub>	0	Data output port			
CLK	l l	Data Latches on Low-to-High Transition			
I <sub>0</sub> -I <sub>1</sub>	1	Instruction inputs. Refer to Instruction Control Tables.			
S <sub>0</sub> , S <sub>1</sub>	ı	Selects one of four registers to be read at the output port.			
ŌĒ	ı	Active Low, output enable. A high signal disables the output port.			

### PIN CONFIGURATION



## REGISTER SELECT

S1	S0	WS59520 or WS59521
0	0	B2
0	1	B1
1	0	A2
1	1	A1

### **INSTRUCTION CONTROL**

11	10	WS59520	WS59521
0	0	A1 B1 A2 B2	A1 B1 B2 B2
0	1	A1 B1 A2 B2	A1 B1 A2 B2
1	0	A1 B1 A2 B2	A1 B1 A2 B2
1	1	ALL REGISTERS HOLD	ALL REGISTERS HOLD

## DC CHARACTERISTICS Over Operating Range (See Notes)

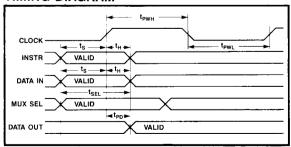
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V <sub>OH</sub>	Output High Voltage	$V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -6.5 \text{ mA}$		2.4			
V	Output Low Voltage	$V_{CC} = Min$	$V_{CC} = Min$ $I_{OL} = 20 \text{ mA (Comm'l)}$		0.5	v I	
V <sub>OL</sub>	Output Low Voltage	$V_{IN} = V_{IH} \text{ or } V_{IN}$	/ <sub>IL</sub>	I <sub>OL</sub> = 16 mA (Military)		0.5	v
V <sub>IH</sub>	Input High Voltage	Guaranteed In	Guaranteed Input High Voltage				
V <sub>IL</sub>	Input Low Voltage	Guaranteed Input Low Voltage				0.8	
I <sub>IX</sub>	Input Load Current	V <sub>CC</sub> = Max, V <sub>IN</sub> = Gnd or V <sub>CC</sub>			-10	10	
loz	High Impedance Output Current	$V_{CC} = Max, V_O = Gnd \text{ or } V_{CC}$		-50	50	μА	
1	Dynamic Power	$V_{CC} = Max$ $0^{\circ} \text{ to } +70^{\circ}\text{C (Comm'I)}$ $-55^{\circ} \text{ to } +125^{\circ}\text{C (Military)}$			12	mA	
Icc	Supply Current				15	i iiiA	
	Static Power	V May	0°	to +70°C (Comm'l)		100	
Icc	Supply Current	$V_{CC} = Max$	-55° to +125°C (Military)			200	μΑ

**NOTES:** 1. Commercial:  $V_{CC} = +5V \pm 5\%$ ,  $T_A = 0^{\circ}$  to  $+70^{\circ}$ C.

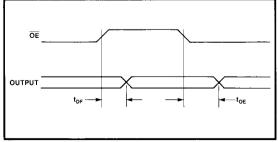
# SWITCHING CHARACTERISTICS Over Operating Range (See Notes)

	DESCRIPTION					
PARAMETER		СОММ	ERCIAL	MILITARY		UNITS
		MIN	MAX	MIN	MAX	
t <sub>PD</sub>	Clock to Data Out		22		24	
t <sub>SEL</sub>	Mux Select to Data Out		20		22	
t <sub>S</sub>	Input (Data/Instr.) Set Up	10		10		
t <sub>H</sub>	Input (Data/Instr.) Hold	3		3		ns
t <sub>DF</sub>	Output Disable	_	15		16	]
t <sub>OE</sub>	Output Enable		21		22	]
t <sub>PWH</sub>	Clock Pulse Width High	10		10		
t <sub>PWL</sub>	Clock Pulse Width Low	10		10		

## **TIMING DIAGRAM**



## **OUTPUT TIMING DIAGRAM**



Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

<sup>2.</sup> Military:  $V_{CC} = +5V \pm 10\%$ ,  $T_A = -55$ °C to +125°C.

<sup>3.</sup>  $C_L = 50 \text{ pF}$  except for  $t_{DF}$  where  $C_L = 5 \text{ pF}$ .

# **ORDERING INFORMATION**

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59520K	22	24 Pin CERDIP, 0.3"	K1	Comm'l	Standard
WS59520KM	24	24 Pin CERDIP, 0.3"	K1	Military	Standard
WS59520KMB	24	24 Pin CERDIP, 0.3"	K1	Military	MIL-STD-883C
WS59520S	22	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS59521K	22	24 Pin CERDIP, 0.3"	K1	Comm'l	Standard
WS59521KM	24	24 Pin CERDIP, 0.3"	K1	Military	Standard
WS59521KMB	24	24 Pin CERDIP, 0.3"	K1	Military	MIL-STD-883C
WS59521S	22	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard