HD74LV273

Octal D-type Flip Flops with Clear

Description

The HD74LV273 has eight edge trigger D type flip flops with clear in a 20 pin package. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the clock input. The clear input when low, sets all outputs to a low state. Low voltage and high speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

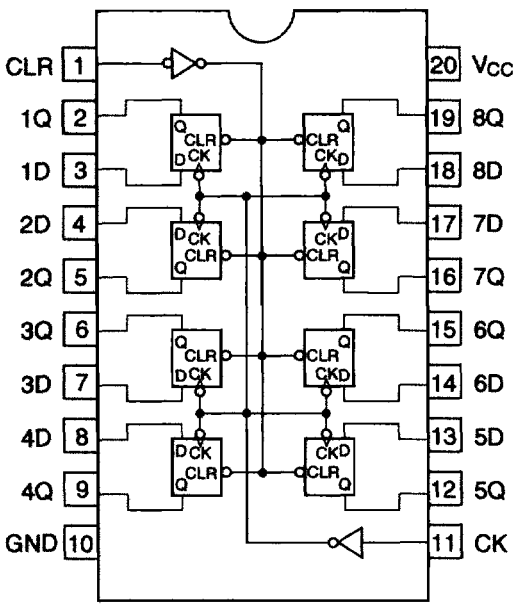
- V_{CC} = 2.0 V to 5.5 V
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Output current ±6 mA (@V_{CC} = 3.0 V to 3.6 V)
  ±12 mA (@V_{CC} = 4.5 V to 5.5 V)

Function Table

Inputs			
CLR	**CK**	**D**	**Output Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0
H	↓	X	Q_0

H : High level
L : Low level
X : Immaterial
↑ : Low to high transition
↓ : High to low transition
Q0 : Level of Q before the indicated steady input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 7.0	V	
Input diode current	I_{IK}	–20	mA	V_I = –0.5 V
Input voltage	V_I	–0.5 to 7.0	V	
Output diode current	I_{OK}	–50	mA	V_O = –0.5 V
		50	mA	V_O = V_{CC} + 0.5 V
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Output current	I_O	±25	mA	
V_{CC}, GND current / pin	I_{CC} or I_{GND}	50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2.0 to 5.5	V	
Input / output voltage	V_I	0 to 5.5	V	CLR, CK, D
	V_O	0 to V_{CC}	V	Q
Operating temperature	Ta	–40 to 85	°C	
Output current	I_{OH}	–6	mA	V_{CC} = 3.0 V to 3.6 V
		–12[*2]	mA	V_{CC} = 4.5 V to 5.5 V
	I_{OL}	6	mA	V_{CC} = 3.0 V to 3.6 V
		12[*2]	mA	V_{CC} = 4.5 V to 5.5 V
Input rise / fall time[*1]	t_r, t_f	50	ns/V	V_{CC} = 5.5 V
		100	ns/V	V_{CC} = 3.6 V

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform : Refer to test circuit of switching characteristics.
2. duty cycle ≤ 50%

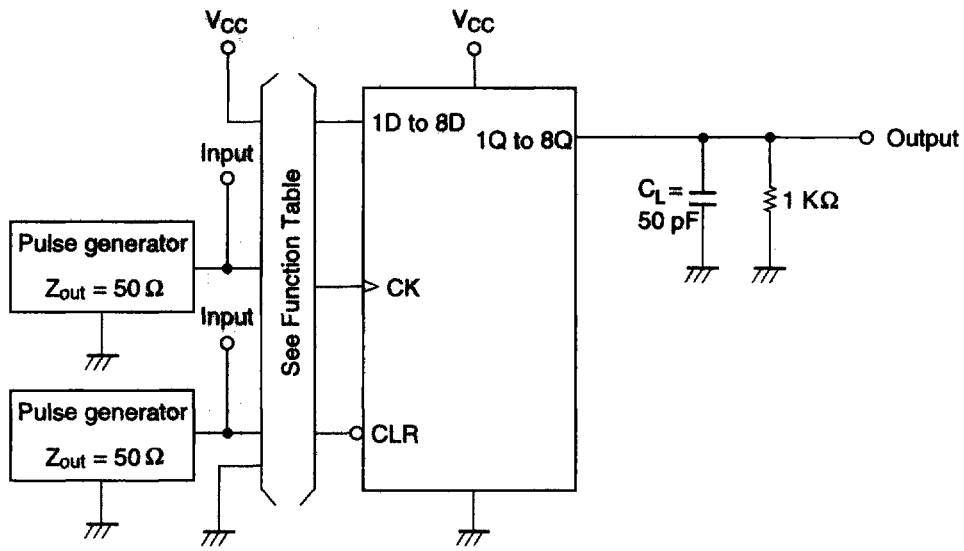
Electrical Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	V_{CC}×0.7	—	V	
	V_{IL}	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	V_{CC}×0.3	V	
Output voltage	V_{OH}	2.7 to 5.5	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		3.0	2.4	—	V	I_{OH} = –6 mA
		4.5	3.6	—	V	I_{OH} = –12 mA
	V_{OL}	2.7 to 5.5	—	0.2	V	I_{OL} = 100 µA
		3.0	—	0.4	V	I_{OL} = 6 mA
		4.5	—	0.5	V	I_{OL} = 12 mA
Input current	I_{IN}	0 to 5.5	—	±1.0	µA	V_{IN} = 5.5 V or GND
Quiescent supply current	I_{CC}	5.5	—	20	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	500	µA	V_{IN} = one input at (V_{CC} – 0.6) V, other inputs at V_{CC} or GND

Switching Characteristics

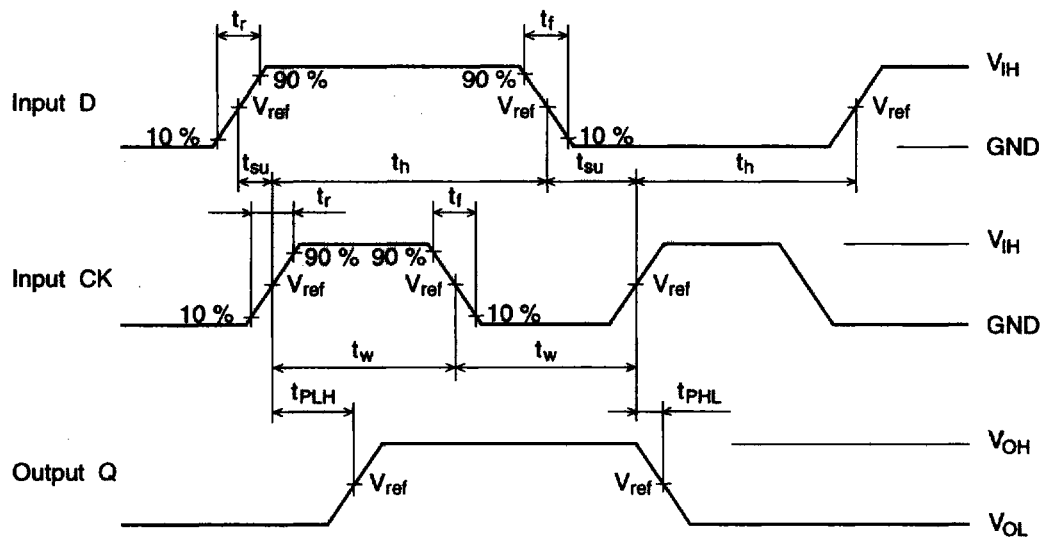
Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max	Min	Typ	Max			
Maximum clock frequency	f_{max}	2.7	40.0	60.0	—	40.0	—	—	MHz		
		3.3±0.3	50.0	75.0	—	50.0	—	—	MHz		
		5.0±0.5	60.0	100.0	—	60.0	—	—	MHz		
Propagation delay time	t_{PLH}	2.7	—	17.0	27.0	1.0	—	30.0	ns	CK	Q
	t_{PHL}	3.3±0.3	—	12.0	23.0	1.0	—	25.5	ns		
		5.0±0.5	—	9.5	16.0	1.0	—	18.0	ns		
	t_{PHL}	2.7	—	14.0	20.0	1.0	—	22.5	ns	CLR	Q
		3.3±0.3	—	12.0	18.5	1.0	—	20.5	ns		
		5.0±0.5	—	8.5	14.0	1.0	—	15.5	ns		
Setup time	t_{su}	2.7	8.0	—	—	9.0	—	—	ns		
		3.3±0.3	7.0	—	—	8.0	—	—	ns		
		5.0±0.5	5.0	—	—	5.0	—	—	ns		
Hold time	t_h	2.7	0.0	—	—	0.0	—	—	ns		
		3.3±0.3	0.0	—	—	0.0	—	—	ns		
		5.0±0.5	0.0	—	—	0.0	—	—	ns		
Pulse width	t_w	2.7	12.0	—	—	12.0	—	—	ns	CK	
		3.3±0.3	10.0	—	—	10.0	—	—	ns		
		5.0±0.5	8.0	—	—	8.0	—	—	ns		
		2.7	15.0	—	—	15.0	—	—	ns	CLR	
		3.3±0.3	12.0	—	—	12.0	—	—	ns		
		5.0±0.5	10.0	—	—	10.0	—	—	ns		
Recovery time	t_{rec}	2.7	3.0	—	—	3.0	—	—	ns		
		3.3±0.3	3.0	—	—	3.0	—	—	ns		
		5.0±0.5	3.0	—	—	3.0	—	—	ns		
Input capacitance	C_{IN}	3.3±0.3	—	—	—	—	2.5	—	pF		

Test Circuit



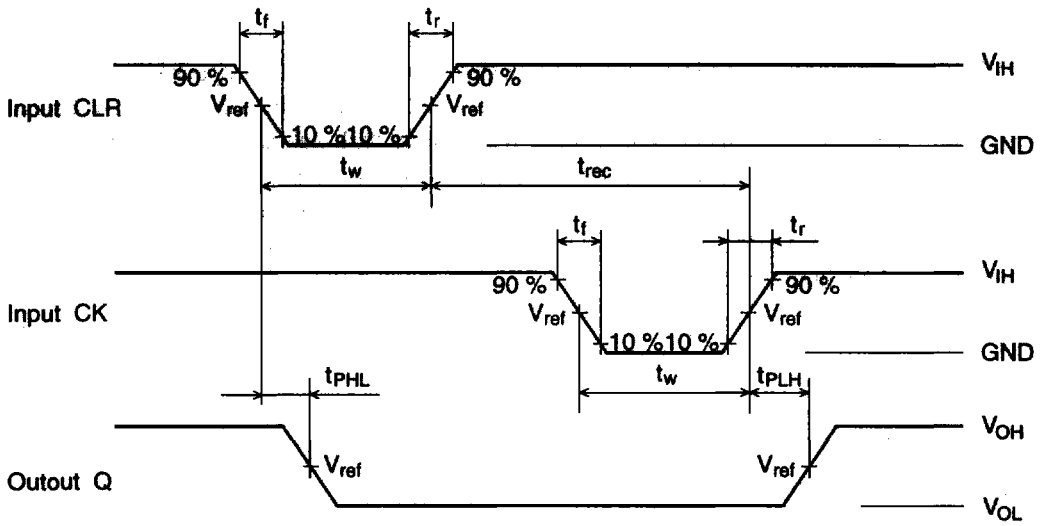
Note: 1. C_L includes probe and jig capacitance.

Waveforms-1



Notes: 1. t_r = 2.5 ns, t_f = 2.5 ns
2. Input CK : PRR = 10 MHz, duty cycle 50%
3. Input D : PRR = 5 MHz, duty cycle 50%

Waveforms-2



Symbol	Vcc = 2.7 V, 3.3±0.3 V	Vcc = 5.0±0.5 V
V_{IH}	2.7 V	Vcc
V_{ref}	1.5 V	50%Vcc

Notes: 1. t_r = 2.5 ns, t_f = 2.5 ns
2. Input waveforms : PRR = 10 MHz, duty cycle 50%