128K x 8 Static RAM

Key Parameters S128K8 and S128K8L	Device Types							
	25C	35M 35I 35C	45M 45I 45C	55M 55I 55C	70M 70I 70C	85M 85I 85C	100M 100I 100C	Unit
Access Time	25	35	45	55	70	85	100	nS
Cycle Time	25	35	45	55	70	85	100	nS
Output Enable Access	10	15	15	20	25	30	50	nS

Features

- **32 pin DIP, LCC, SOJ, Flatpack**
- **Advanced 4-T CMOS technology**
- **S128K8 is compliant to DESC Standardized Military Drawing No. 5962-89598**
- **300 mil DIP for 25, 35, 45 ns parts**
- **Military, industrial, and commercial temperature range**
- **Military grades compliant to MIL-STD-883C**

General Description

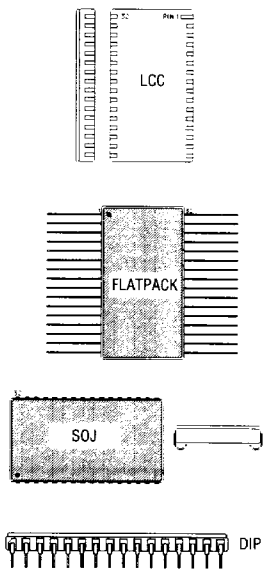
The Inova S128K8 is a high performance one megabit Static Random Access Memory (SRAM) organized as 128K eight -bit bytes.

The S128K8 is manufactured using a highly reliable, four transistor cell CMOS process. This provides a component which combines low active and standby power characteristics with high performance.

All inputs are fully TTL-compatible. Operation is fully static, without need for extra control logic to generate clock signals.

Every military grade device is fully compliant to MIL-STD-883C, paragraph 1.2.1. Industrial and commercial grade devices are fabricated in the same production line which assures that they are also of the highest quality.

Package Options



Pinout

1	NC	32	VCC
2	A16	31	A15
3	A14	30	NC
4	A12	29	$\overline{WE}$
5	A7	28	A13
6	A6	27	A8
7	A5	26	A9
8	A4	25	A11
9	A3	24	$\overline{OE}$
10	A2	23	A10
11	A1	22	$\overline{CS}$
12	A0	21	I/O7
13	I/O0	20	I/O6
14	I/O1	19	I/O5
15	I/O2	18	I/O4
16	VSS	17	I/O3

A0-A16	Address Inputs
I/O0-I/O7	Data Input/ Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
VCC	+5V Power
VSS	Ground

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage(1)	V_{CC}	4.5	5.5	V
Input HIGH Voltage	V_{IH}	2.2	V_{CC}+0.5	V
Input LOW Voltage	V_{IL}	-0.5	0.8	V
Operating Temp. Mil.	T_C	-55	125	°C
Operating Temp. Ind.	T_C	-40	85	°C
Operating Temp. Comm.	T_C	0	70	°C

Absolute Maximum Ratings (2)

Temperature Under Bias	-55 °C to 125 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage(1)	-0.5V to 7.0 V
Signal Voltage On Any Pin	-0.5 V to V_{CC} + 0.5V
Power Dissipation	1 Watt
D.C. Continuous Output Current Per Output	20 mA
Lead Temperature (Soldering 10 sec)	260 °C

Notes:

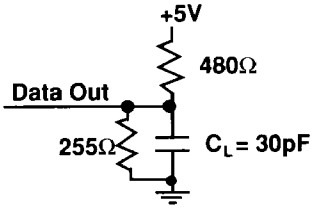
1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}/I_{FSB}
Read	L	L	H	Output	I_{CC2}
Write	L	X	L	Input	I_{CC2}
Output Disable	L	H	H	High Z	I_{CC2}

Load Test Circuits



C_L = 5pF for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{WLZ}.

Memory Scale

Access Time	25	35	45	55	70	85	100	Unit
S128K8	40	29	22	18	14	11	10	kbits/ns

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

DC and Operating Characteristics

L=Low Power, S = Standard Power

Symbol		25		35		45		55		70		85		100		Units
		L	S	L	S	L	S	L	S	L	S	L	S	L	S	
I_{CC1} (1)	C	90	100	80	90	80	90	80	90	80	90	80	90	80	90	mA(max)
	I	----	----	85	95	85	95	85	95	85	95	85	95	85	95	
	M	----	----	90	100	90	100	90	100	90	100	90	100	90	100	
I_{CC2} (2)		140	150	125	140	125	125	125	125	125	125	125	125	125	125	mA(max)
I_{SB} (3)	C	30	40	3	30	1.5	4	1.5	4	1.5	4	1.5	4	1.5	4	mA(max)
	I	----	----	4	35	2.0	5	2.0	5	2.0	5	2.0	5	2.0	5	
	M	----	----	10	40	10	10	10	10	10	10	10	10	10	10	
I_{FSB} (4)	C	0.75	----	0.75	----	0.75	----	0.75	----	0.75	----	0.75	----	0.75	----	mA(max)
	I	----	----	1.25	----	1.25	----	1.25	----	1.25	----	1.25	----	1.25	----	
	M	----	----	5	----	5	----	5	----	5	----	5	----	5	----	
I_{CCDR} (5)	C	0.10	----	0.10	----	0.10	----	0.10	----	0.10	----	0.10	----	0.10	----	mA(max)
	I	----	----	0.15	----	0.15	----	0.15	----	0.15	----	0.15	----	0.15	----	
	M	----	----	2.0	----	2.0	----	2.0	----	2.0	----	2.0	----	2.0	----	
V_{DR} (6)		2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	V(min)

Notes:

(1) Static Supply Current: $\overline{CS}$=V_{IL}, $\overline{OE}$ = V_{IH}, No address transitions

(2) Dynamic Supply Current: $\overline{CS}$ < V_{IL}, $\overline{OE}$ = V_{IH}, Address Change every t_{RC}

(3) Standby Supply Current With TTL Inputs:
$\overline{CS}$ > V_{IH}, Address change every t_{RC}

(4) Standby Supply Current With CMOS Inputs: $\overline{CS}$ = V_{CC}+0.2V, No address transitions

(5) Data Retention Current: $\overline{CS}$ = V_{DR} min, V_{CC} = V_{DR} min

(6) Data Retention Voltage: V_{CC} minimum supply voltage

DC and Operating Characteristics

L=Low Power, S = Standard Power

Symbol	25		35		45		55		70		85		100		Units
	L	S	L	S	L	S	L	S	L	S	L	S	L	S	
$\lvert I_{LI} \rvert$ (1)	2	2	2	2	2	2	2	2	2	2	2	2	2	2	µA(max)
$\lvert I_{LO} \rvert$ (2)	2	2	2	2	2	2	2	2	2	2	2	2	2	2	µA(max)
V_{OL} (3)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	V (max)
V_{OH} (4)	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	V (min)

Typical	*Test Conditions*	*Addresses*	*Data I/O*	*$\overline{CS}$, $\overline{WE}$, $\overline{OE}$*	
Pin Capacitance	Pin Voltage=0V, f=1.0 MHz	8	10	12	pF(typ)

Notes:

(1) Input Leakage Current: V_{CC} = max, V_{IN} = GND to V_{CC}

(2) Output Leakage Current: V_{OUT} = GND to V_{CC}, Outputs in tri-state

(3) Output Low Voltage: I_{OL} = 8 mA

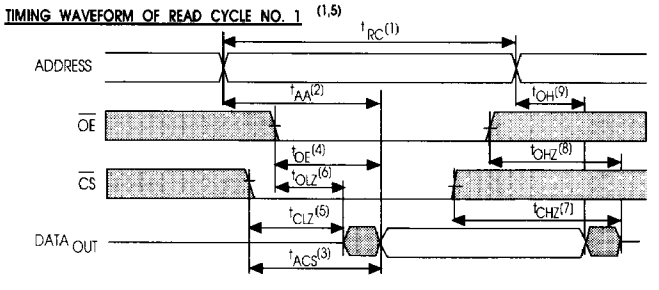
(4) Output High Voltage: I_{OH} = -4 mA

AC Characteristics[1]

No.	S128K8 and S128K8L Parameter	Symbol	25C		35C,I,M		45C,I,M		55C,I,M		70 C,I,M		85C,I,M	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min
1	Read Cycle Time	t_{RC}	25		35		45		55		70		85	
2	Address Access Time	t_{AA}		25		35		45		55		70		85
3	$\overline{CS}$ on to Output Valid	t_{ACS}		25		35		45		55		70		85
4	$\overline{OE}$ on to Output Valid	t_{OE}		10		15		15		20		25		30
5	$\overline{CS}$ on to Output in Low Z	t_{CLZ}(2,3)	5		5		5		5		5		5	
6	$\overline{OE}$ on to Output in Low Z	t_{OLZ}(2,3)	0		0		0		0		0		0	
7	$\overline{CS}$ off to Output in High Z	t_{CHZ}(2,3)	0	10	0	15	0	20	0	35	0	35	0	35
8	$\overline{OE}$ off to Output in High Z	t_{OHZ}(2,3)	0	10	0	15	0	20	0	35	0	35	0	35
9	Output Hold from Address Change	t_{OH}	3		5		5		5		5		5	
10	Write Cycle Time	t_{WC}	25		35		45		55		70		85	
11	Chip Selection to End of Write	t_{CW}	20		25		35		45		60		75	
12	Address Set-up Time	t_{AS}	0		0		0		0		0		0	
13	Address Valid to End of Write	t_{AW}	20		25		35		45		60		75	
14	Write Pulse Width	t_{WP}	20		25		30		35		35		40	
15	Write Recovery Time	t_{WR}	0		0		5		5		5		5	
16	Write Pulse on to Output in High Z	t_{WHZ}(2,3)	0	10	0	15	0	20	0	35	0	35	0	35
17	Write Pulse off to Output in Low Z	t_{WLZ}(2,3)	5		5		5		5		5		5	
18	Data Valid Set-Up to End of Write	t_{DW}	15		20		25		25		30		35	
19	Data Hold from End of Write	t_{DH}	0		0		0		3		3		3	
20	Chip Deselect to Data Retention	t_{CDR}(2)	0		0		0		0		0		0	
21	Operation Recovery Time	t_{R}(2)		25		35		45		55		70		85

Notes: (1) At Recommended Operating Conditions. All Values in Nanoseconds. 100nS and 120nS parts are also available. (2) This Parameter is characterized initially and after any design or process change which could affect it. It is guaranteed to, but not tested to, the limits specified. (3) All Transitions are measured ± 500mV from steady state with loading as specified in "Load Test Circuits."

READ CYCLE



Reading the S128K8 device is accomplished by taking chip select ($\overline{CS}$) and output enable($\overline{OE}$) LOW , while write enable ($\overline{WE}$) remains inactive or high. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

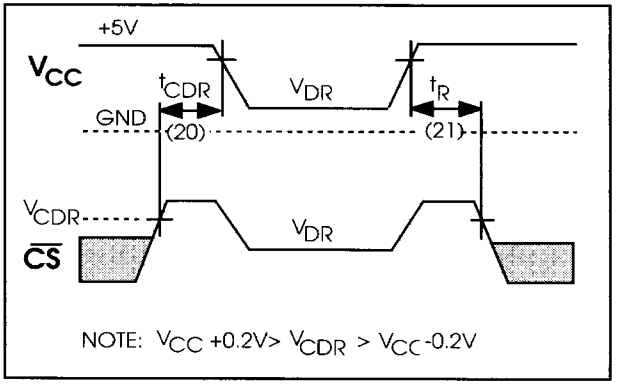
Notes:

1. $\overline{WE}$ is high for READ CYCLES.
2. Device is continuously selected, $\overline{CS}$= V_{IL} for all outputs active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ =V_{IL}
5. Data Output transitions measured ±500mV from steady state. This parameter is sampled and not 100% tested

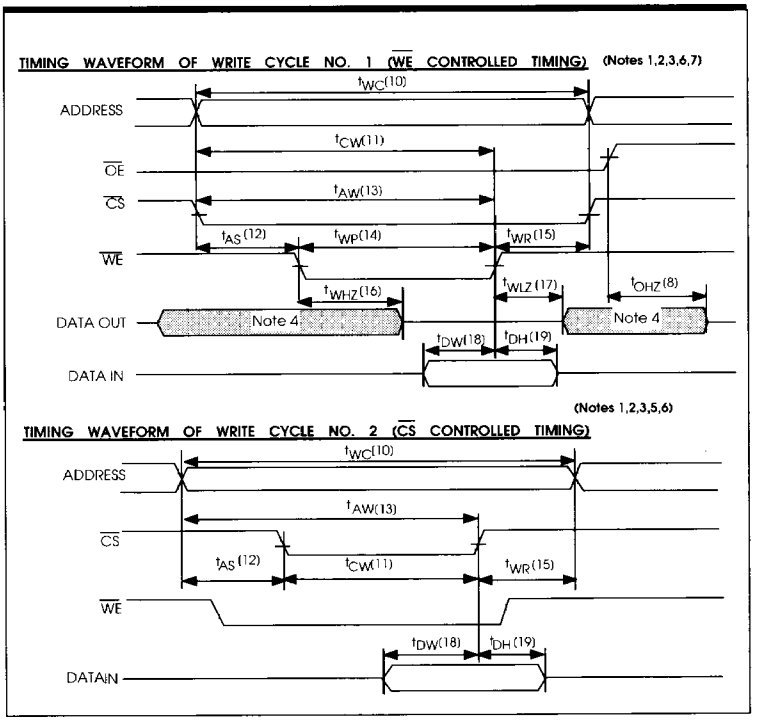
Data Retention

S128K8 devices exhibit very low current drain when operated in Data Retention Mode. This Mode is entered by first driving Chip Select to V_{CC} and subsequently driving both V_{CC} and Chip Select to V_{DR}. Chip Select must be set up before the V_{CC} drops below its minimum level. When exiting from Data Retention Mode, the user must wait one full Read Cycle Time prior to asserting Chip Select.

DATA RETENTION TIMING



WRITE CYCLE



Writing to the S128K8 is achieved when the chip select (CS) and write enable (WE) inputs are LOW. Data on the input/output pins is written into the memory location specified on the address pins (A0-A16).

The input/output pins remain in a high impedance state when chip select (CS) or output enable (OE) is HIGH, or write enable (WE) is LOW.

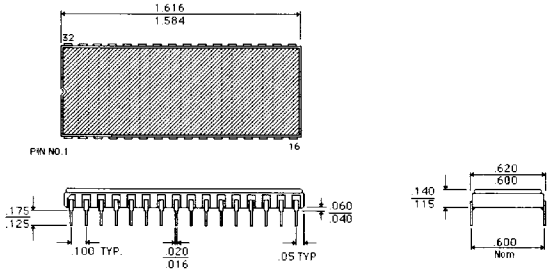
Notes:

1. WE or CS must be high during all address transitions.
2. A write occurs during the overlap (TWP) of a low CS and a low WE.
3. TWR is measured from the earlier of CS or WE going high to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CS low transitions occurs simultaneously with or after the WE low transition, the outputs remain in a high impedance state.
6. Data output transitions are measured ± 500mV from steady state. This parameter is sampled and characterized but not 100% tested.
7. During a WE controlled write cycle, write pulse low is ≥TDW + TWHZ to allow the I/O drivers to turn off and data to be placed on the the bus for the required TDW. If OE is high during a WE controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified TWP.

Package Dimension and Ordering Information

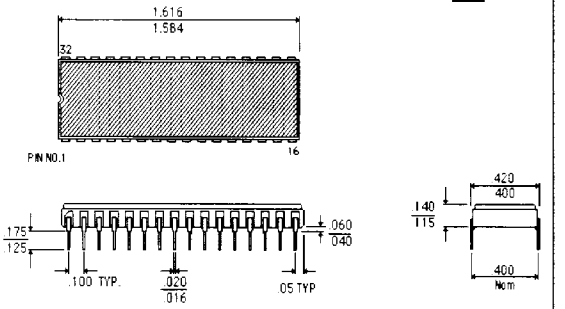
32 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
600 MIL WIDE

C



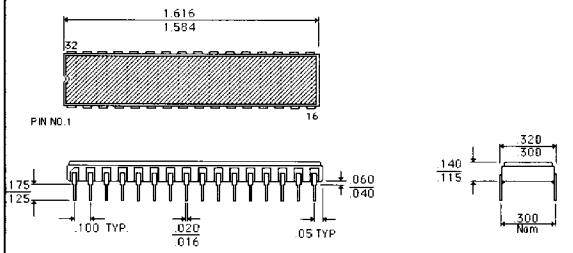
32 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
400 MIL WIDE

E

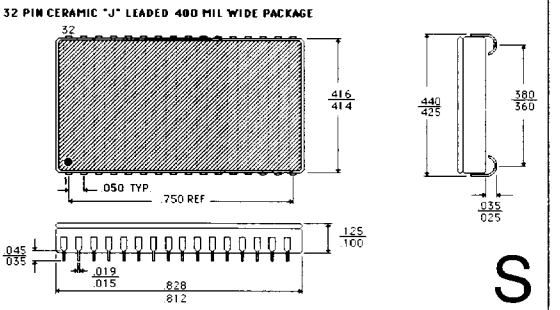


32 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
300 MIL WIDE

T

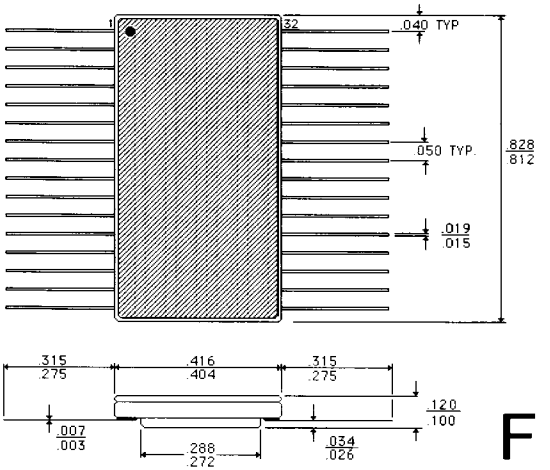


32 PIN CERAMIC "J" LEADED 400 MIL WIDE PACKAGE



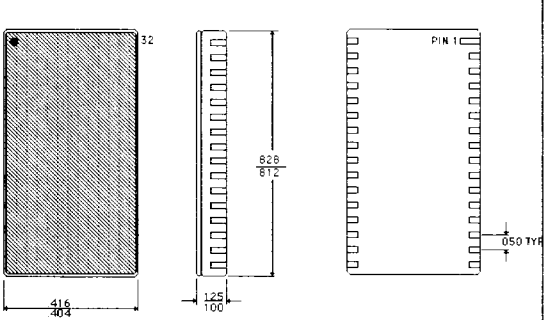
S

32 PIN CERAMIC FLATPACK, 400 MIL WIDE PACKAGE



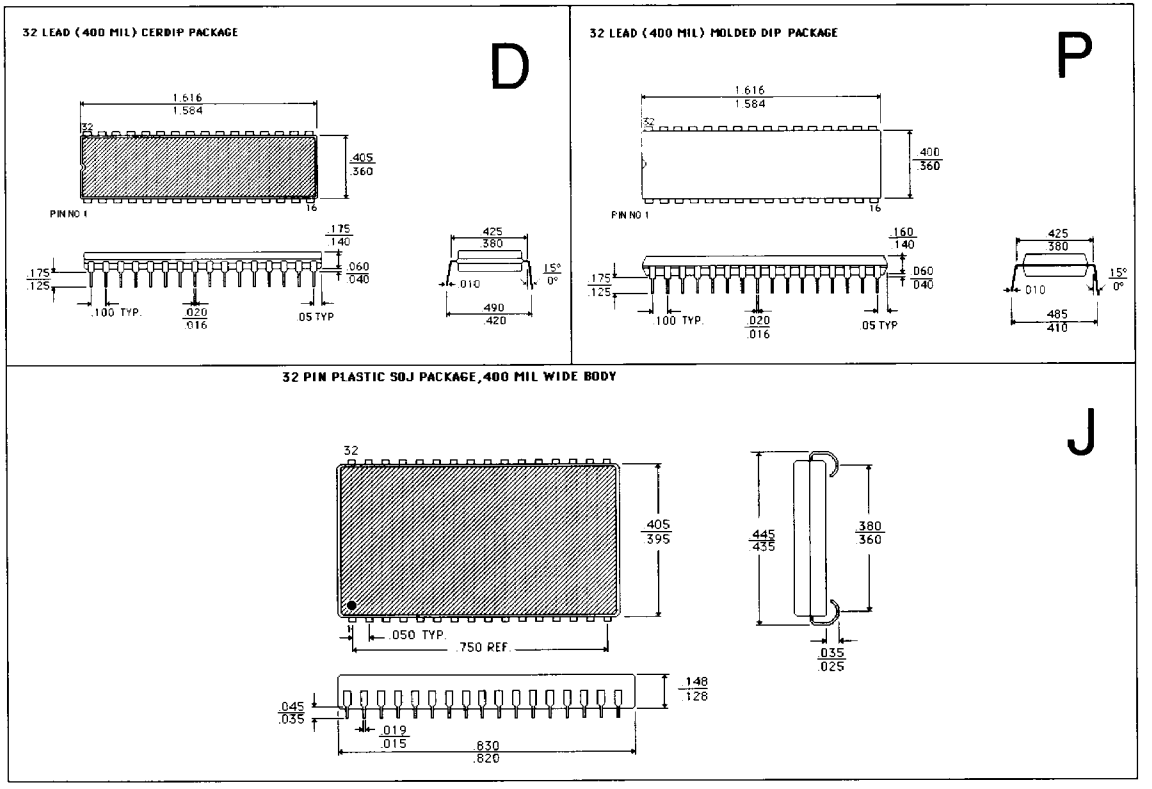
F

32 PIN LEADLESS CHIP CARRIER PACKAGE



L

Package Dimension and Ordering Information



S128K8X-25XX

- C = Commercial Temperature Range (0°C to 70°C)
- I = Industrial Temperature Range (-40°C to 85°C)
- M = Military Temperature Range (-55°C to 125°C)

- C = 600 mil Ceramic Sidebrazed DIP
- D = 400 mil CERDIP
- E = 400 mil Ceramic Sidebrazed DIP
- T = 300 mil Ceramic Sidebrazed DIP
- P = 400 mil Plastic DIP
- F = Flatpack
- S = Ceramic SOJ
- J = Plastic SOJ
- L = Leadless Chip Carrier

- L suffix on base part number = Low Power Device

All Specifications are subject to change without notice.
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