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MA6116 & MA6216

RADIATION HARD 2048 x 8 BIT STATIC RAM

The MA6116 16k Static RAM is configured as 2048 x 8 bits and manufactured using CMOS-SOS high performance, radiation hard, 3µm technology. The MA6216 is manufactured using 2.5µm technology resulting in faster performance.

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when chip select is in the HIGH state.

Operation Mode	CS	OE	WE	I/O	Power
Read	L	L	H	D OUT	
Write	L	H	L	D IN	ISB1
Write	L	L	L	D IN	
Standby	H	X	X	High Z	ISB2

Figure 1: Truth Table

FEATURES

- 3µm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 110ns (MA6116) and 85ns (MA6216) Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset >10^{10} Rad(Si)/sec
- SEU <10^{-10} Errors/bitday
- Single 5V Supply
- Three State Output
- Low Standby Current 100µA Typical
- -55°C to +125°C Operation
- TTL and CMOS Compatible Inputs
- Fully Static Operation

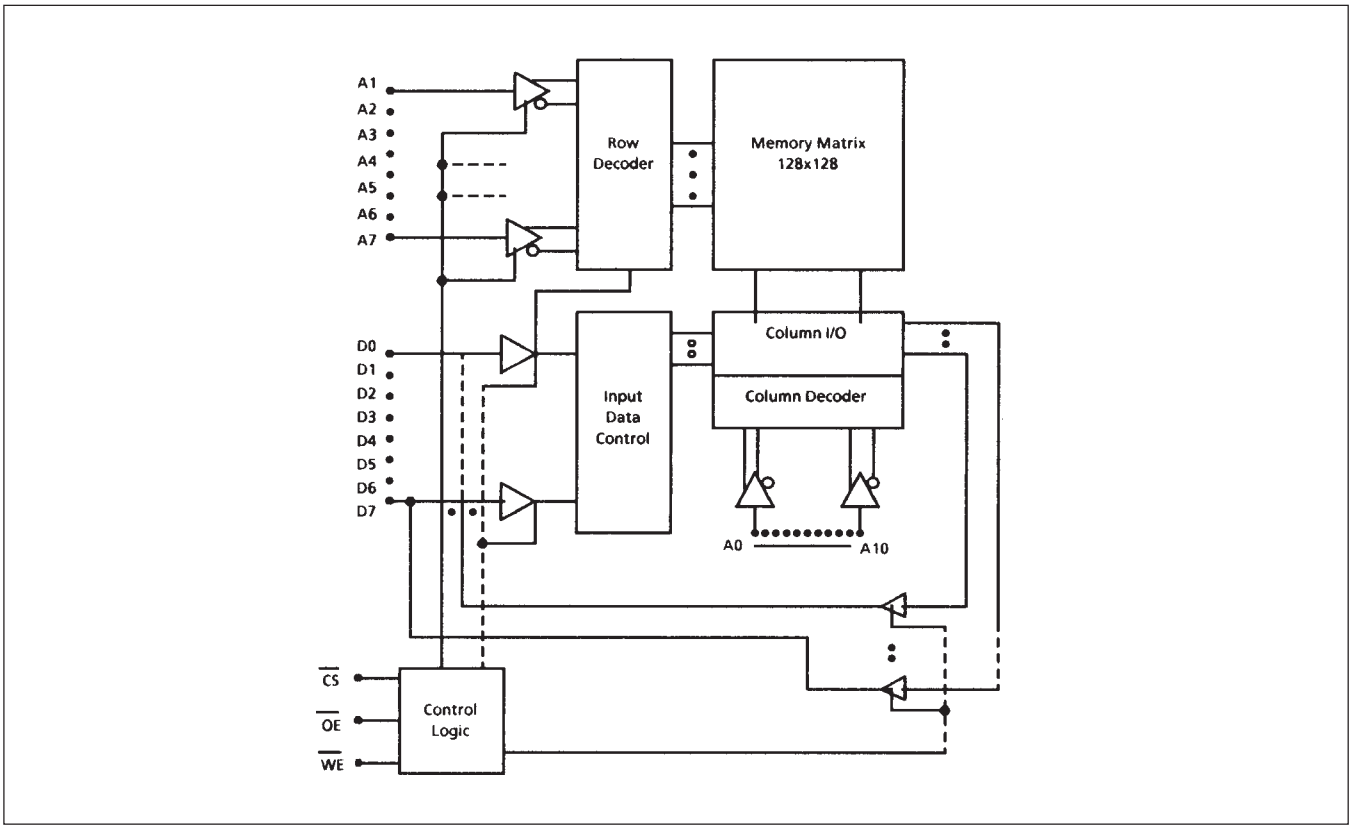


Figure 2: Block Diagram

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply Voltage	-0.5	7	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Figure 3: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functlonal operation of the device at these condltions, or at any other condition above those indicated in the operations section of this specification, is not Implied Exposure to absolute maxlmum rating conditions for extended perlods may affect device reliability.

Notes for Tables 4 and 5:
1. Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request).
2. Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C.
3. GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	V_{DD}/2	-	V_{DD}	V
V_{IL}	Input Low Voltage	-	V_{SS}	-	0.8	V
V_{OH}	Output High Voltage	I_{OH1} = -1mA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA	-	-	0.4	V
I_{LI}	Input Leakage Current (note 2)	All inputs except $\overline{CS}$	-	-	±10	µA
I_{LO}	Output Leakage Current (note 2)	Output disabled, V_{OUT} = V_{SS} or V_{DD}	-	-	±20	µA
I_{DD}	Power Supply Current	f_{RC} = 1MHz, $\overline{CS}$ = 50% mark:space	-	20	40	mA
I_{SB1}	Selected Supply Current	All inputs = V_{DD}-0.2V except $\overline{CS}$ = V_{SS}+0.2V	-	50	70	mA
I_{SB2}	Standby Supply Current	Chip disabled, $\overline{CS}$ = V_{DD}-0.2V	-	0.1	5	mA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	-	50	3000	µA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V.
2. Times measurement reference level = 1.5V.
3. Output load 1TTL gate and C_L = 60pF.
4. Transition is measured at ±500mV from steady state.
5. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	MA6116		MA6216		Units
		Min	Max	Min	Max	
T_{AVAVR}	Read Cycle Time	150	-	100	-	ns
T_{AVQV}	Address Access Time	-	130	-	95	ns
T_{ELQV}	Chip Select Access Time	-	140	-	100	ns
T_{ELQX} (4,5)	Chip Select to Output in Low Z	10	-	10	-	ns
T_{GLQV}	Output Enable to Output Valid	-	80	-	60	ns
T_{GLQX} (4,5)	Output Enable to Output in Low Z	10	-	10	-	ns
T_{EHQZ} (4,5)	Chip Deselect to Output in High Z	0	60	0	50	ns
T_{GHQZ} (4,5)	Chip Disable to Output in High Z	0	60	0	50	ns
T_{AXQX}	Output Hold from Address Change	10	-	10	-	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	MA6116		MA6216		Units
		Min	Max	Min	Max	
T_{AVAVW}	Write Cycle Tlme	150	-	100	-	ns
T_{ELWH}	Chip Selection to End of Write	85	-	75	-	ns
T_{AVWH}	Address Valid to End of Write	80	-	70	-	ns
T_{AVWL}	Address Set Up Time	20	-	10	-	ns
T_{WLWH}	Write Pulse Width	50	-	40	-	ns
T_{WHAV}	Write Recovery Time	5	-	5	-	ns
T_{WLQZ} (4,5)	Write to Output in High Z	0	60	0	50	ns
T_{DVWH}	Data to Write Time Overlap	30	-	25	-	ns
T_{WHDX}	Data Hold from Write Time	10	-	10	-	ns
T_{WHQX} (4,5)	Output Active from End to Write	5	-	5	-	ns
T_{ELWL}	Chip Selection to Write Low	25	-	25	-	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_O = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

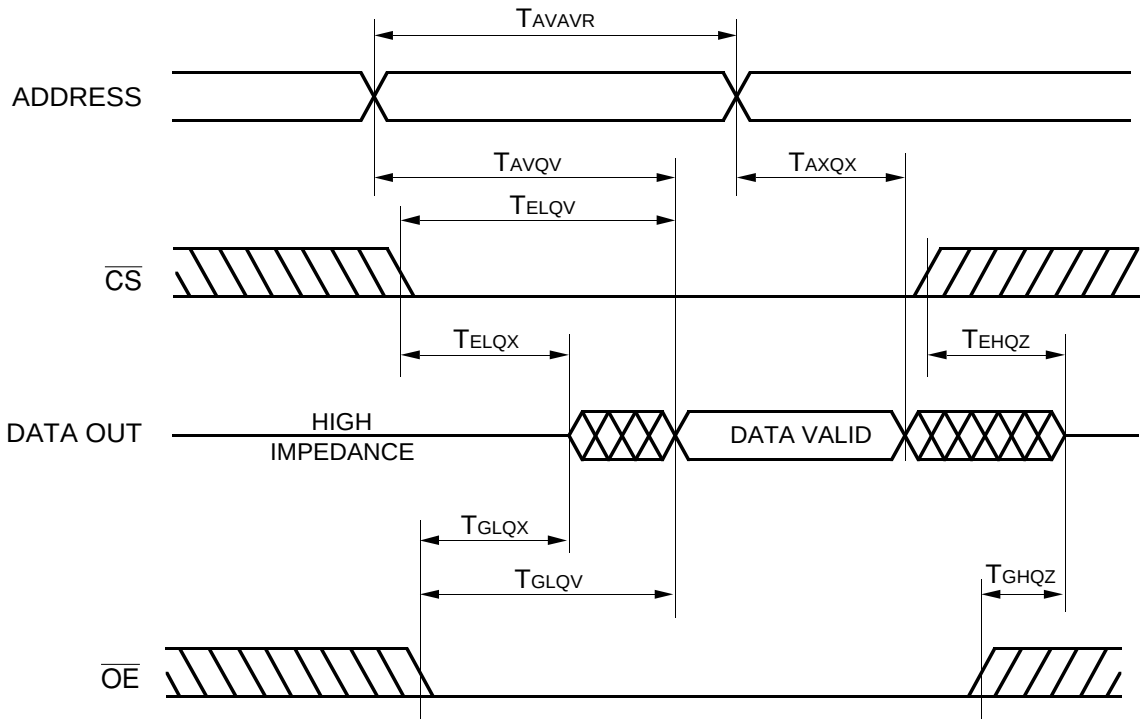
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

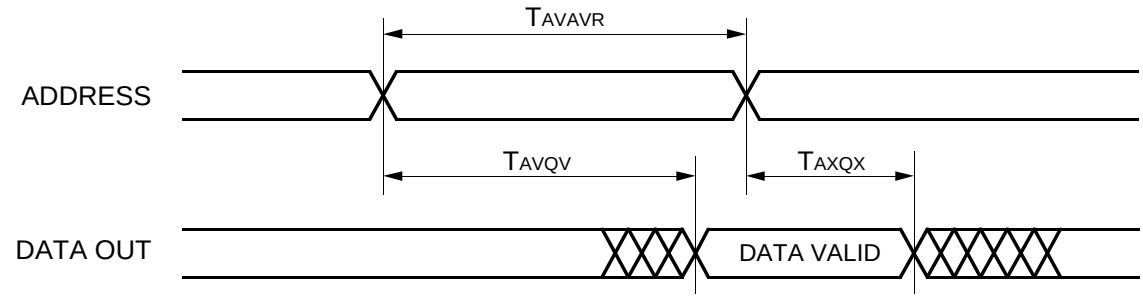
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



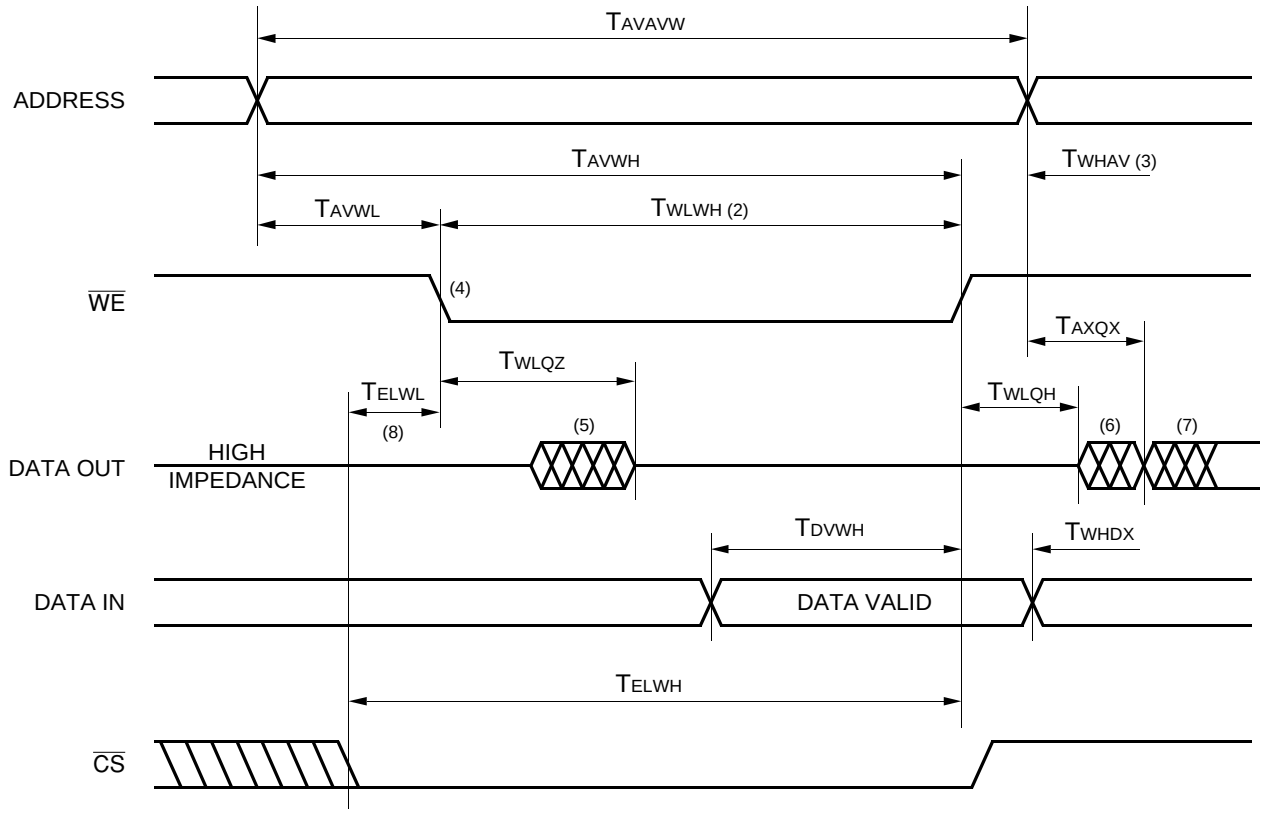
1. WE is high for Read Cycle.
2. Address Vaild prior to or coincident with CS transition low.

Figure 11a: Read Cycle 1



1. WE is high for Read Cycle.
2. Device is continually selected. CS is high.

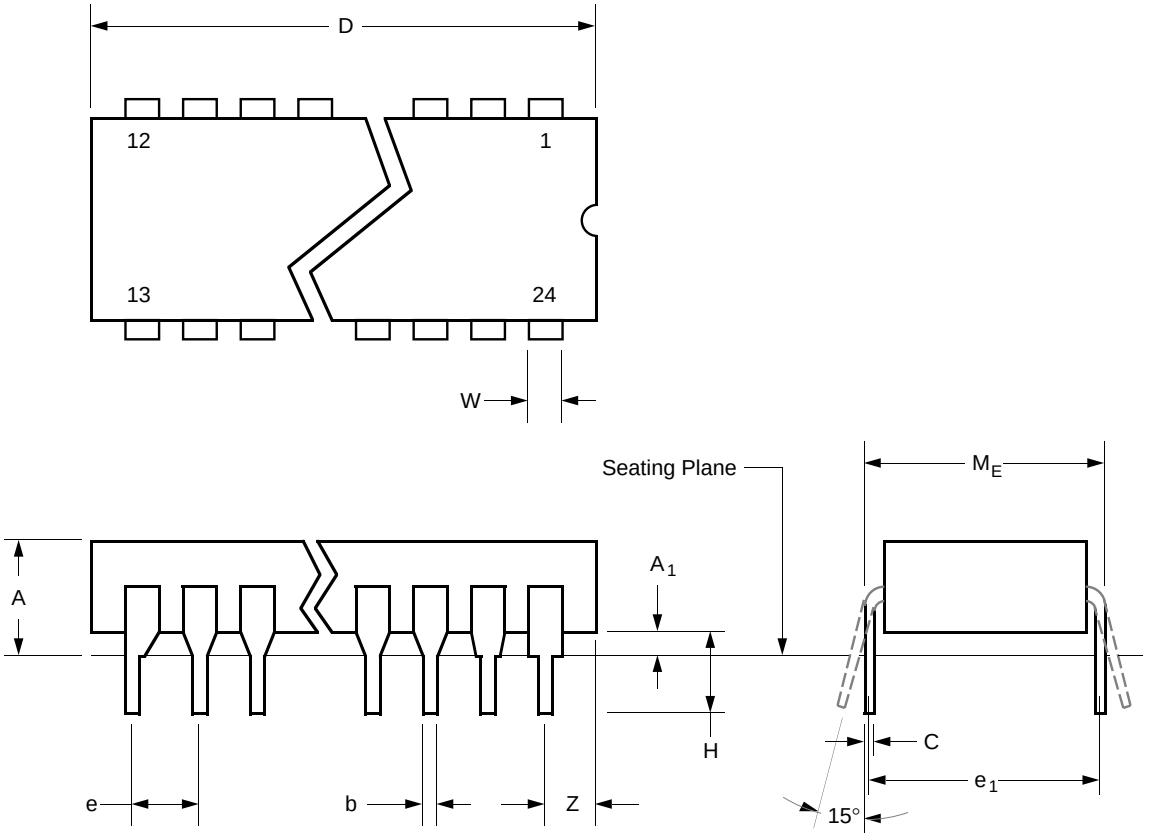
Figure 11b: Read Cycle 2



1. WE must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low CS and a low WE.
3. T_{WHAV} is measured from either CS or WE going high, whichever is the earlier, to the end of the write cycle.
4. If the CS low transition occurs simultaneously with, or after, the WE low transition, the output remains in the high impedance state.
5. DATA OUT is in the active state, so DATA IN must not be in opposing state.
6. DATA OUT is the write data of the current cycle, if selected.
7. DATA OUT is the read data of the next address, if selected.
8. T_{ELWL} must be met to prevent memory corruption.
9. OE is low. (If OE is high then DATA OUT remains in the high impedance state throughout the cycle).

Figure 12: Write Cycle

OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	30.79	-	-	1.212
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

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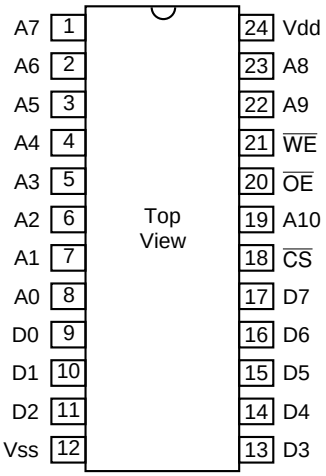
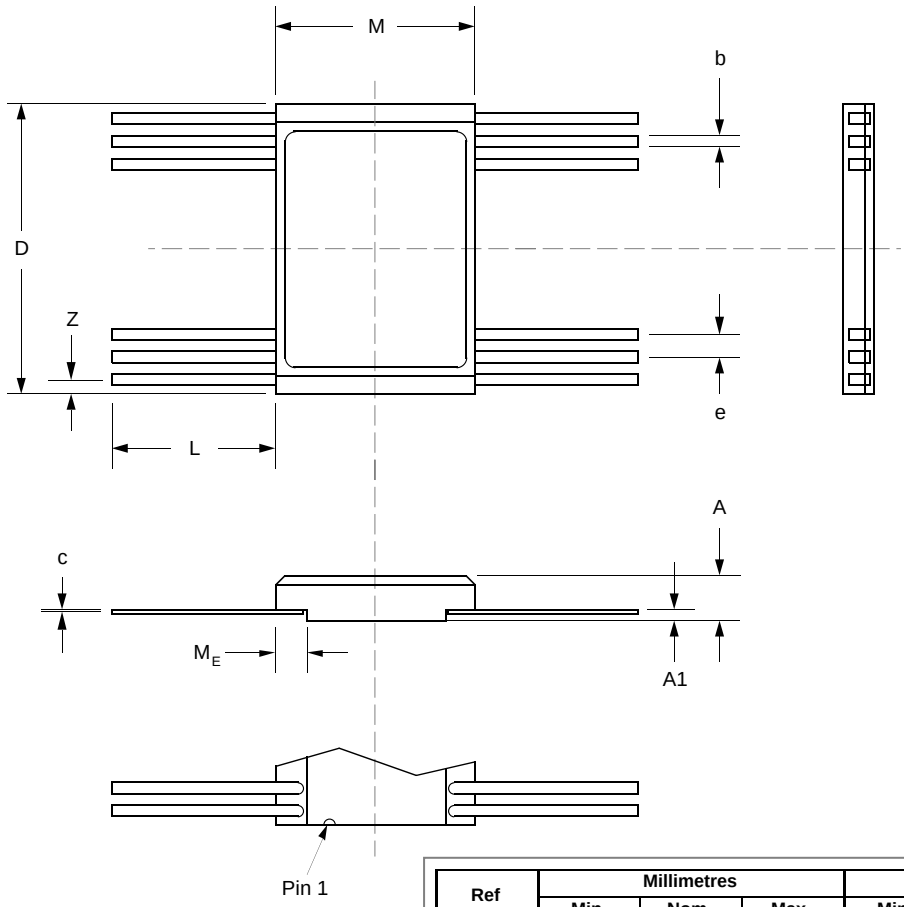


Figure 13: 24-Lead Ceramic DIL (Solder Seal) - Package Style C



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	3.07	-	-	0.121
A1	0.66	-	-	0.026	-	-
b	0.38	-	0.48	0.015	-	0.019
c	0.08	-	0.152	0.003	-	0.006
D	14.99	-	15.50	0.590	-	0.610
e	-	2.54	-	-	0.050	-
L	6.73	-	7.75	0.265	-	0.305
M	9.96	-	10.36	0.392	-	0.408
Me	7.6	-	-	0.30	-	-
Z	0.13	-	1.14	0.005	-	0.045

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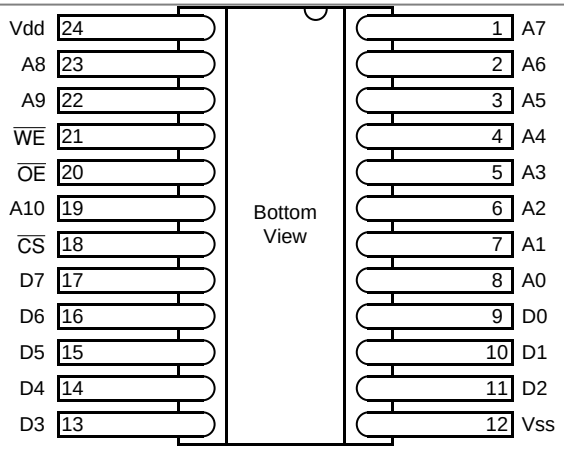
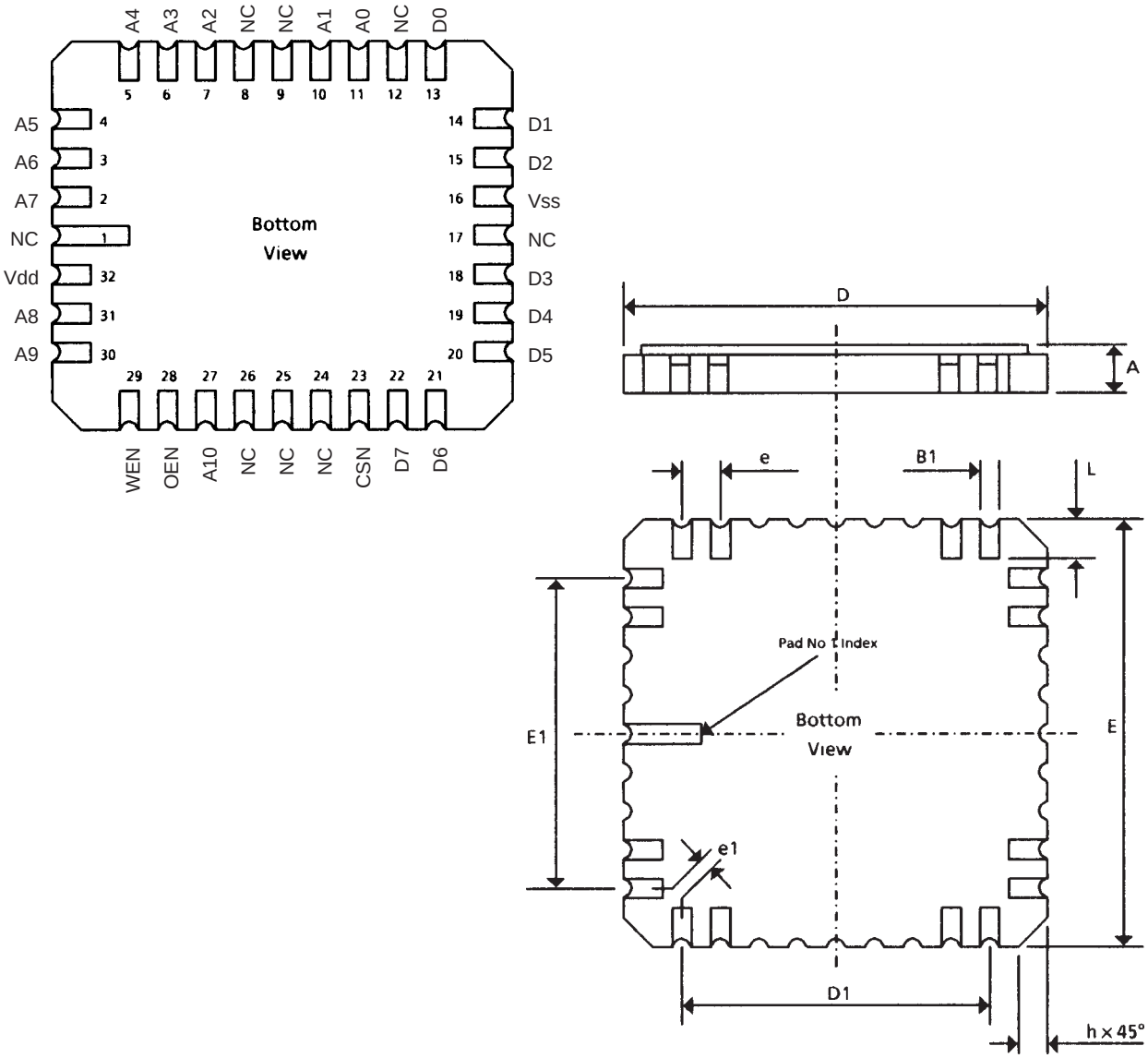


Figure 14: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style F



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.83	-	2.28	0.072	-	0.090
B1	0.56	-	0.71	0.022	-	0.028
D	11.30	-	11.63	0.445	-	0.458
D1	-	7.62	-	-	0.300	-
E	13.84	-	14.22	0.545	-	0.560
E1	-	10.61	-	-	0.400	-
e	-	1.27	-	-	0.050	-
e1	0.38	-	-	0.015	-	-
h	-	1.016	-	-	0.040	-
i	-	0.51	-	-	0.020	-
L	-	1.27	-	-	0.050	-
L2	1.96	-	2.36	0.077	-	0.093

XG520

Figure 15: 32-Pad Leadless Chip Carrier - Package Style L

Function	Package Options		Via	Burnin			Radiation
	L	C&F		Static1	Static 2	Dynamic	
A7	2	1	R	0V	5V	F7	5V
A6	3	2	R	0V	5V	F6	5V
A5	4	3	R	0V	5V	F5	5V
A4	5	4	R	0V	5V	F4	5V
A3	6	5	R	0V	5V	F3	5V
A2	7	6	R	0V	5V	F2	5V
A1	10	7	R	0V	5V	F1	5V
A0	11	8	R	0V	5V	F0	5V
D0	13	9	R	0V	5V	LOAD	5V
D1	14	10	R	0V	5V	LOAD	5V
D2	15	11	R	0V	5V	LOAD	5V
VSS	16	12	Direct	0V	0V	0V	0V
D3	18	13	R	0V	5V	LOAD	5V
D4	19	14	R	0V	5V	LOAD	5V
D5	20	15	R	0V	5V	LOAD	5V
D6	21	16	R	0V	5V	LOAD	5V
D7	22	17	R	0V	5V	LOAD	5V
CSB	23	18	R	0V	5V	0V	5V
A10	27	19	R	0V	5V	F10	5V
OEB	28	20	R	0V	5V	5V	5V
WEB	29	21	R	0V	5V	5V	5V
A9	30	22	R	0V	5V	F9	5V
A8	31	23	R	0V	5V	F8	5V
VDD	32	24	Direct	5V	5V	5V	5V

1. F0=150KHz, F1=F0/2, F2=F0/4, F3=F0/8 etc.
2. Burnin R=1k
3. Radiation R=10k

Figure 16: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$3.4x10^{-9}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 17: Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

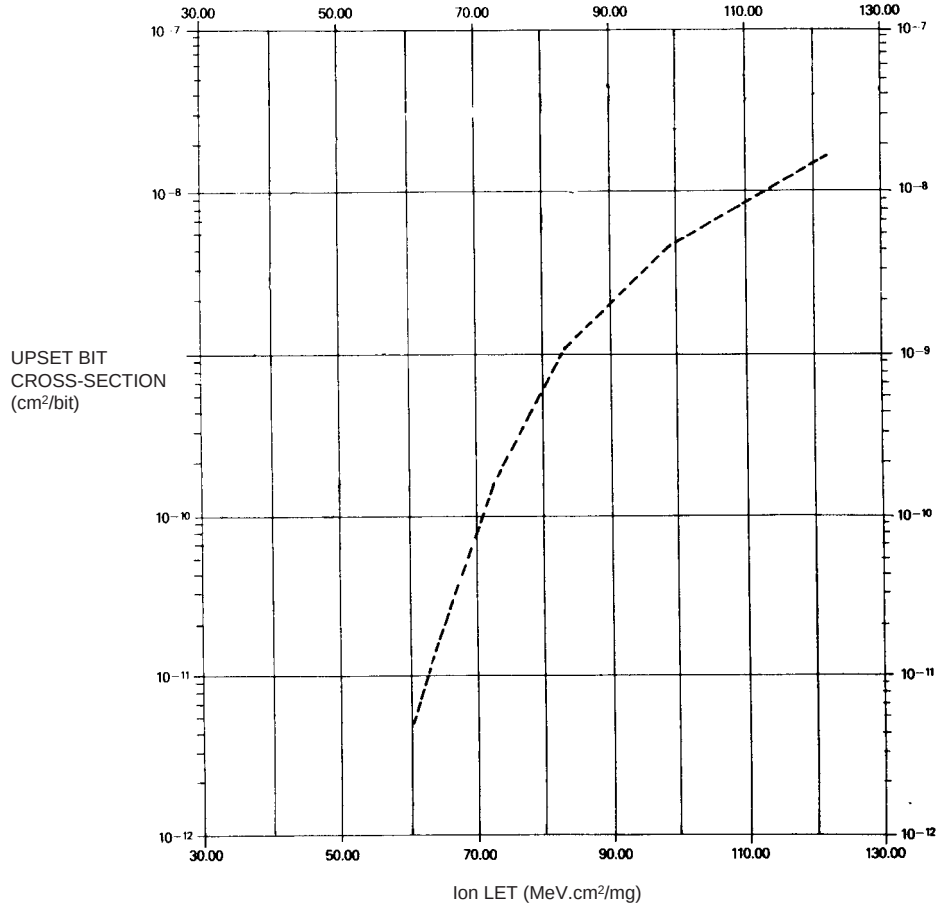
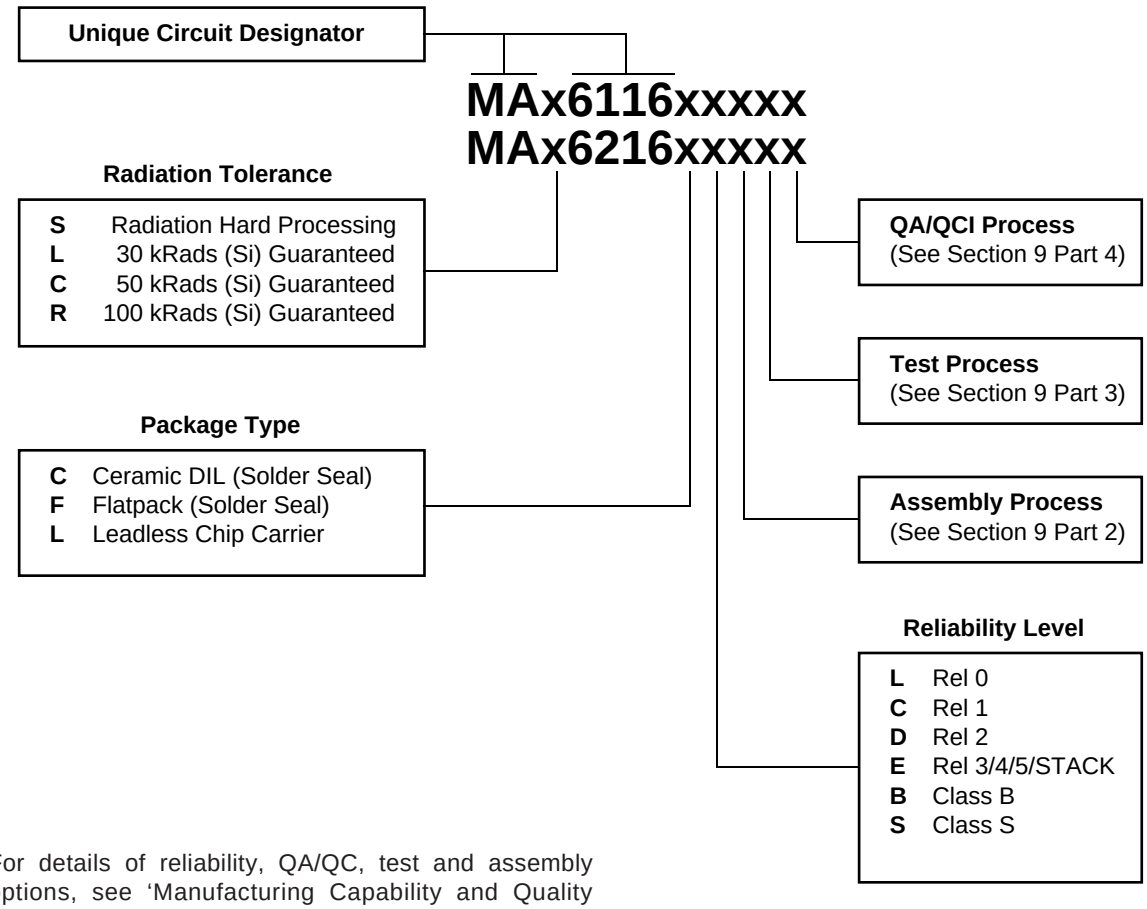


Figure 18: Typical Per-Bit Upset Cross-Section vs Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

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