FEATURES

- Full Four Quadrant Multiplication
- Low Glitch Energy
- 12-Bit Linearity (End-Point)
- Guaranteed Monotonic. All Grades. All Temperatures.
- TTL/CMOS Compatible
- Stable, More Accurate Segmented Architecture
 - 2.0 ppm/°C Typ. Gain Error Tempco
 - 0.2 ppm/°C Max. Linearity Tempco
 - **Lowest Sensitivity to Output Amplifier Offset**
- PDIP, CDIP & SOIC Packages Available
- ESD Protection: 2000 V Minimum
- Latch-Up Free

APPLICATIONS

- Industrial Automation
- Automatic Test Equipment
- Disk Drive Servo Systems
- **Digital/Synchro Conversion**
- Programmable Gain Amplifiers • Ratiometric A/D Conversion

Digital-to-Analog Converter

- Function Generation
- Digitally Controlled Filters

GENERAL DESCRIPTION

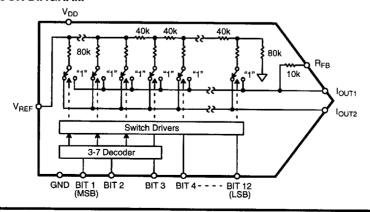
The MP7541B is a pin-compatible replacement which offers superior performance in latch-up and ESD protection versus the comparable 7541 and 7541A. The high ESD protection will reduce failures caused by mishandling. These devices are manufactured using MPS' patented advanced thin film resistors on a double metal CMOS process which result in ultra stable thin film and superior long life reliability and stability. The MP7541B incorporates a bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. The MP7541B's outstanding features are:

Stability: Both Integral-Non-Linearity and Differential-Non-Linearity are rated at 0.2 ppm/°C maximum. Monotonicity is guaranteed over the entire temperature range. Gain Temperature Coefficient (TCGE) is 2.0 ppm/°C typical.

Lower Sensitivity to Output Amplifier Offset: Multiplying DACs provide an output current into a virtual ground of the output op amp. Additional linearity error caused by the op amp is reduced by a factor of 3 in the MP7541B versus conventional R-2R DACs.

Specified for operation over the commercial / industrial (-40 to +85°C) and Military (-55 to +125°C) temperature ranges, the MP7541B is available in Plastic (PDIP) and Ceramic (CDIP) dual-in-line and Surface Mount (SOIC) packages.

SIMPLIFIED BLOCK DIAGRAM



MP7541B

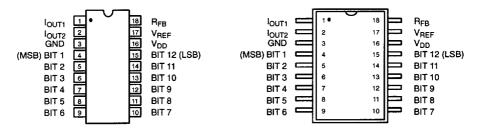
Micro Power Systems

ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	-40 to +85°C	MP7541BKN	±1/2	±1/2	±5
Plastic Dip	-40 to +85°C	MP7541BJN	±1	土1	±8
SOIC	-40 to +85°C	MP7541BKS*	±1/2	±1/2	±5
SOIC	-40 to +85°C	MP7541BJS*	土1	±1	土8
Ceramic Dip	-55 to +125°C	MP7541BTD*	±1/2	士1/2	±5
Ceramic Dip	-55 to +125°C	MP7541BTD/883*	±1/2	±1/2	±5
Ceramic Dip	-55 to +125°C	MP7541BSD*	±1	土1	±8
Ceramic Dip	-55 to +125°C	MP7541BSD/883*	±1	±1	±8

^{*}Contact factory for availability.

PIN CONFIGURATIONS



18 Pin PDIP, CDIP (0.300") N18, D18

18 Pin SOIC (Jedec, 0.300") **S18**

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	l _{OUT1}	Current Output 1
2	lout2	Current Output 2
3	GND	Ground
4	BIT 1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5
9	BIT 6	Data Input Bit 6

PIN NO.	NAME	DESCRIPTION
10	BIT 7	Data Input Bit 7
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10
14	BIT 11	Data Input Bit 11
15	BIT 12	Data Input Bit 12 (LSB)
16	V _{DD}	Positive Power Supply
17	V _{RÉF}	Reference Input Voltage
18	R _{FB}	Internal Feedback Resistor





MP7541B

ELECTRICAL CHARACTERISTICS

 V_{DD} = + 15 V, V_{REF} = +10 V, I_{OUT1} = I_{OUT2} = GND = 0 V Unless Otherwise Noted.

Parameter	Symbol	Mîn	25°C Typ	Max	Tmin to Min	Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE (1)								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy) K, T	INL			±1/2		±1/2	LSB	End Point Linearity
J, S				±1		±1		
Differential Non-Linearity K, T J, S	DNL			±1/2 ±1		±1/2 ±1	LSB	All grades monotonic over full temperature range.
Gain Error K, T J, S	GE	•		±3 ±6		±5 ±8	LSB	Using Internal R _{FB}
Gain Temperature Coefficient (2)	TC _{GE}					<u>+</u> 2	ppm/°C	ΔGain/∆Temperature
Power Supply Rejection Ratio	PSRR		5	±50		<u>+</u> 100	ppm/%	$ \Delta Gain/\Delta V_{DD} $ $\Delta V_{DD} = \pm 5\%$
Output Leakage Current	İLKG		5	±10		±200	пА	Digital Inputs = 0 or 5 V
DYNAMIC PERFORMANCE (2)								RL=100Ω, C _{EXT} =13pF
Current Settling Time	ts		0.65	1.0			μs	Full scale change to 1/2 LSB
AC Feedthrough at I _{OUT1}	F _T		1.0				mV p-p	V _{REF} = 20 V p-p 10kHz, Sinewave
Glitch Energy	Egl		500				nVs	000 to 111 Input Change
Propagation Delay	t _{PD}		60				ns	From 50% of digital input to 10% of final analog output current
REFERENCE INPUT								
Input Resistance	R _{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS								
Logical "1" Voltage Logical "0" Voltage Input Leakage Current	V _{IH} V _{IL} I _{INH} , I _{INI}	2.4		0.8 ±1.0	2.4	0.8 ±1.0	V V μΑ	
Input Capacitance (2)							`	
Data ANALOG OUTPUTS (2)	C _{IN}			8.0		8.0	pF	
Output Capacitance	C _{OUT1} C _{OUT2} C _{OUT2}		100 50 50 100				pF pF pF pF	DAC all 1's DAC all 0's DAC all 1's DAC all 0's
POWER SUPPLY (3)								
Functional Voltage Range (2) Supply Current	V _{DD}	4.5		16 1.0	4.5	16 1.0	V mA	All Digital Inputs = 0 or 5 V

MP7541B

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

- (1) Full Scale Range (FSR) is 10V for unipolar mode.
- Guaranteed but not production tested. (2)
- (3) Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2) (TA = +25°C unless otherwise noted)

V _{DD} to GND 0 to +17 V	Storage Temperature65°C to +150°C
Digital Input Voltage to GND GND -0.5 to V _{DD} +0.5 V	Lead Temperature (Soldering, 10 seconds) +300°C
I_{OUT1} , I_{OUT2} to GND GND -0.5 to V_{DD} +0.5 V	Package Power Dissipation Rating to 75°C
V _{REF} to GND <u>±</u> 25 V	CDIP, PDIP, SOIC 850mW
V _{RFB} to GND <u>±</u> 25 V	Derates above 75°C 11mW/°C

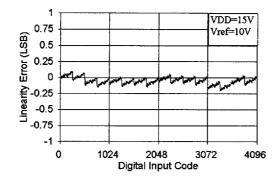
NOTES:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 20mA for less than 100µs.

APPLICATION NOTES Refer to Section 8 for Applications Information

PERFORMANCE CHARACTERISTICS



Graph 1. Linearity Error vs. **Digital Input Code**