

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am29821 - 26

High Performance Bus Interface Registers

DISTINCTIVE CHARACTERISTICS

- High-speed parallel registers with positive edge-triggered D-type flip-flops
 - Noninverting CP-Y $t_{PD} = 7.5ns$ typ
 - Inverting CP-Y $t_{PD} = 7.5ns$ typ
- Buffered common Clock Enable (EN) and asynchronous Clear input (CLR)
- Three-state outputs glitch free during power-up and down. Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL} , 32mA MIL I_{OL}
- Low input/output capacitance
 - 6pF inputs (typical)
 - 8pF outputs (typical)
- Metastable "Hardened" Registers

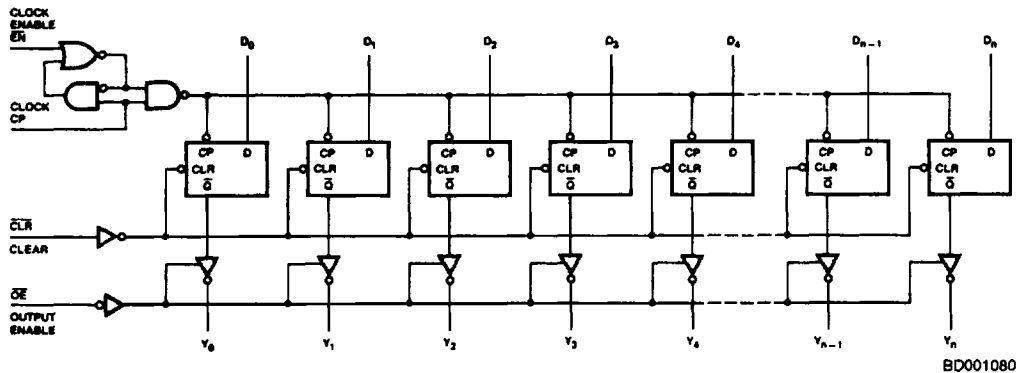
GENERAL DESCRIPTION

The Am29820 Series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The Am29821 and Am29822 are buffered, 10-bit wide versions of the popular '374/'534 functions. The Am29823 and Am29824 are 9-bit wide buffered registers with Clock Enable (EN) and Clear (CLR) - ideal for parity bus interfacing in high performance microprogrammed systems. The Am29825 and Am29826 are 8-bit buffered registers with all the '823/4 controls plus

multiple enables ($\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$) to allow multiuser control of the interface, e.g., CS, DMA, and RD/ \overline{WR} . They are ideal for use as an output port requiring high I_{OL}/I_{OH} .

All of the AM29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAM



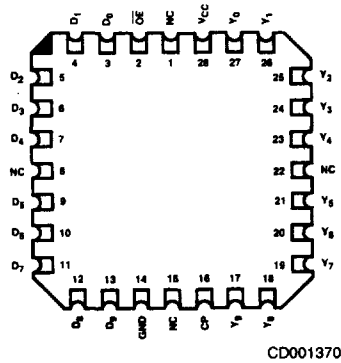
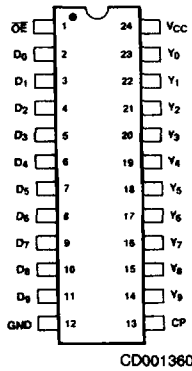
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PRODUCT SELECTOR GUIDE

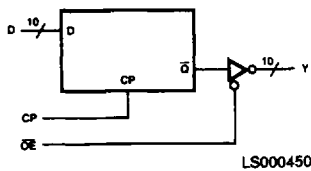
	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29821	Am29823	Am29825
Inverting	Am29822	Am29824	Am29826

CONNECTION DIAGRAM Top View

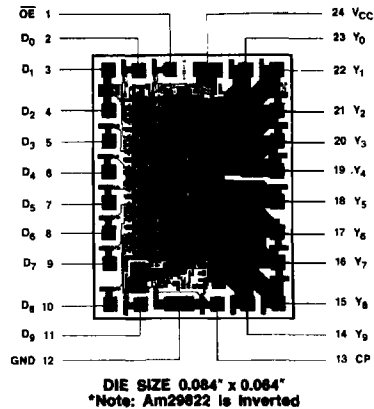
Am29821/Am29822 10-BIT REGISTERS



LOGIC SYMBOL

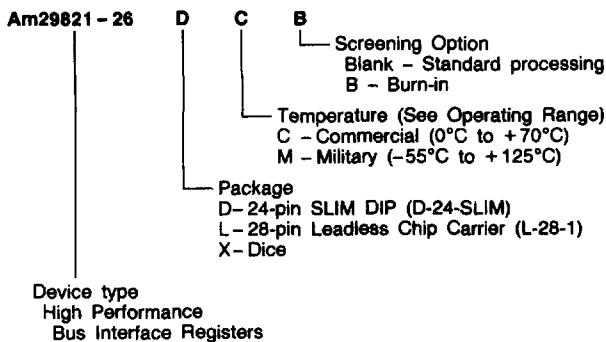


METALLIZATION AND PAD LAYOUT 10-Bit Registers Am29821*



ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

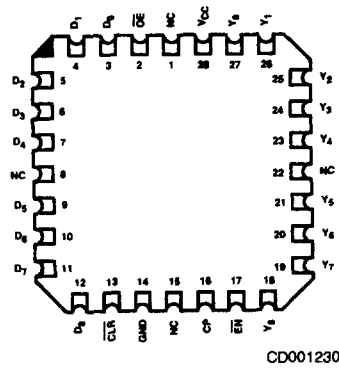
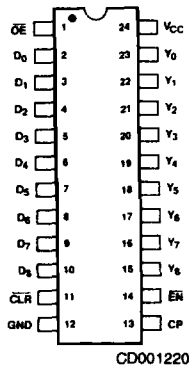


Valid Combinations	
Am29821	DC, DCB, DM,
Am29822	DMB
Am29823	LC, LCB, LM,
Am29824	LMB
Am29825	XC, XM
Am29826	

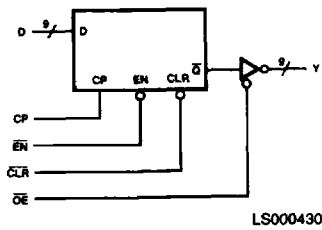
Valid Combinations
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

CONNECTION DIAGRAM Top View

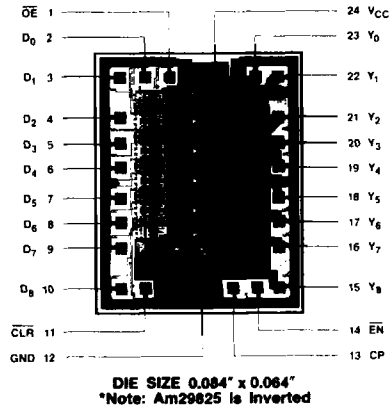
Am29823/Am29824 9-BIT REGISTERS



LOGIC SYMBOL

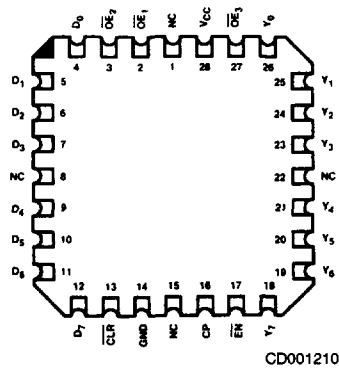
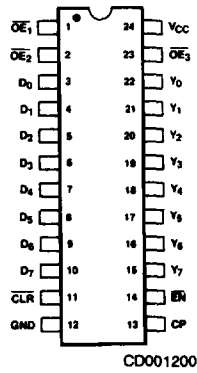


METALLIZATION AND PAD LAYOUT 9-Bit Registers Am29823*

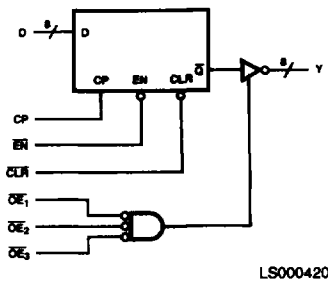


**CONNECTION DIAGRAM
Top View**

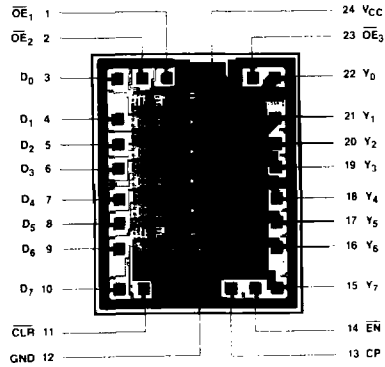
Am29825/Am29826 8-BIT REGISTERS



LOGIC SYMBOL



**METALLIZATION AND PAD LAYOUT
8-Bit Registers
Am29825***



DIE SIZE 0.084" x 0.064"
*NOTE: m29826 is inverted

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The D flip-flop data inputs.
11	CLR	I	For both inverting and noninverting registers, when the clear input is LOW and \overline{OE} is LOW, the Q_i outputs are LOW. When the clear input is HIGH, data can be entered into the register.
13	CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
	Y_i, \overline{Y}_i	O	The register three-state outputs.
14	EN	I	Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions. (Note 5.)
	\overline{OE}	I	Output Control. When the \overline{OE} input is HIGH, the Y_i outputs are in the high impedance state. When the \overline{OE} input is LOW, the TRUE register data is present at the Y_i outputs.

Note 5: The Am29823 thru Am29826 registers achieve short throughput delay and setup time and reduced power consumption by means of a clock gating and latching circuit. This circuit is sensitive to very short (< 3ns) HIGH-to-LOW-to-HIGH going spikes on EN while CP is HIGH. The designer should be aware of this and avoid the use of decoders or other potentially glitching devices in the EN logic.

FUNCTION TABLES

Am29821/29823/29825

Inputs					Internal Outputs		Function
\overline{OE}	CLR	EN	D_i	CP	Q_i	Y_i	
H	X	L	L	↑	L	Z	Hi-Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

Am29822/29824/29826

Inputs					Internal Outputs		Function
\overline{OE}	CLR	EN	D_i	CP	Q_i	\overline{Y}_i	
H	X	L	L	↑	H	Z	Hi-Z
H	X	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	-0.5V to V_{CCmax}
DC Input Voltage	-0.5V to +5.5V
DC Output Current, into Outputs	100mA
DC Input Current	-30mA to +5.0mA

Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	Temperature	0°C to +70°C
	Supply Voltage	+4.75V to +5.25V
Military (M) Devices	Temperature	-55°C to +125°C
	Supply Voltage	+4.5V to +5.5V

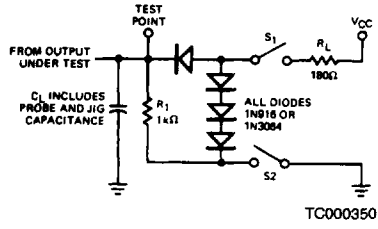
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)		Max	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15mA	2.4	3.3			Volts
				2.0	3.1			
V _{OL}	Output LOW Voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	MIL, I _{OL} = 32mA COM'L, I _{OL} = 48mA		0.31	0.5		Volts
					0.38	0.5		
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0				Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8		Volts
V _I	Input Clamp Voltage	V _{CC} = MIN, I _{IN} = -18mA			-0.7	-1.2		Volts
I _{IL}	Input LOW Current	V _{CC} = MAX, V _{IN} = 0.4V	Data, CLR		-0.3	-1.0		mA
			OE, EN, CP		-1.2	-2.0		
I _{IH}	Input HIGH Current	V _{CC} = MAX, V _{IN} = 2.7V				50		μA
I _I	Input HIGH Current	V _{CC} = MAX, V _{IN} = 5.5V				1.0		mA
I _{OZ}	Output Off-State (High Impedance) Output Current	V _{CC} = MAX	V _O = 0.4V			-50		μA
			V _O = 2.4V			50		
I _{SC}	Output Short Circuit Current (Note 3)	V _{CC} = MAX		-75	-180	-250		mA
I _{CC}	Supply Current (Note 4)	V _{CC} = MAX Outputs Open EN = LOW	Over Temperature Range			140		mA
			+70°C			130		
			+125°C			120		

- Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended Operating Range.
 2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
 3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
 4. Clock input, CP, is HIGH after clocking in data to produce outputs = LOW.

SWITCHING TEST CIRCUIT



SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

Parameters	Description	Test Conditions (Note 4)	Min	Typ	Max	Units	
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE} = \text{LOW}$)	$C_L = 50\text{pF}$	3.5		8.5	ns	
t_{PHL}			3.5		10.5	ns	
t_{PLH}		$C_L = 300\text{pF}$			14	ns	
t_{PHL}					18	ns	
t_S	Data to \overline{CP} Setup Time	$C_L = 50\text{pF}$	2.0	0		ns	
t_H	Data to \overline{CP} Hold Time		2.0	0.5		ns	
t_S	Enable ($\overline{EN} \downarrow$) to CP Setup Time		3.0	1.5		ns	
t_S	Enable ($\overline{EN} \uparrow$) to CP Setup Time		3.0	1.5		ns	
t_H	Enable (\overline{EN}) Hold Time		0	-1.5		ns	
t_{PHL}	Propagation Delay, Clear to Y_i				12.9	15.0	ns
t_S	Clear Recovery ($\overline{CLR} \downarrow$) Time			5.0	1.1		ns
t_{PWH}	Clock Pulse Width		HIGH	5.0	3.5		ns
t_{PWL}			LOW	5.0	3.0		ns
t_{PWL}	Clear ($\overline{CLR} = \text{LOW}$) Pulse Width			5.0	4.0		ns
t_{ZH}	Output Enable Time $\overline{OE} \downarrow$ to Y_i	$C_L = 300\text{pF}$			17	ns	
t_{ZL}					21	ns	
t_{ZH}		$C_L = 50\text{pF}$			11.5	12	ns
t_{ZL}					11.0	12	ns
t_{HZ}	Output Disable Time $\overline{OE} \uparrow$ to Y_i	$C_L = 50\text{pF}$			9	ns	
t_{LZ}					9	ns	
t_{HZ}		$C_L = 5\text{pF}$			5.2	8	ns
t_{LZ}					5.5	8	ns

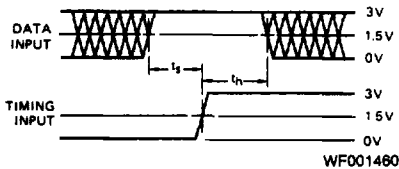
Note: 4. See test circuit and waveforms.



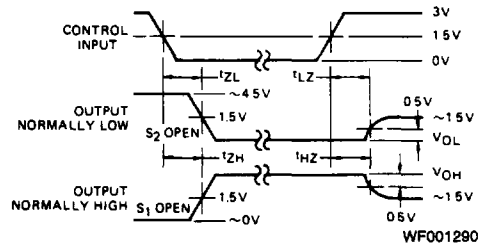
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 4)	COMMERCIAL		MILITARY		Units	
			Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE} = \text{LOW}$)	$C_L = 50\text{pF}$	3.5	10	3.5	10	ns	
t_{PHL}			3.5	12	3.5	12	ns	
t_{PLH}		$C_L = 300\text{pF}$		16		16	ns	
t_{PHL}				20		20	ns	
t_S	Data to \overline{CP} Setup Time	$C_L = 50\text{pF}$	4		4		ns	
t_H	Data to \overline{CP} Hold Time		2		2		ns	
t_S	Enable ($\overline{EN} \downarrow$) to CP Setup Time		4		4		ns	
t_S	Enable ($\overline{EN} \uparrow$) to CP Setup Time		4		4		ns	
t_H	Enable (\overline{EN}) Hold Time		2		2		ns	
t_{PHL}	Propagation Delay, Clear to Y_i			20		20	ns	
t_S	Clear Recovery ($\overline{CLR} \downarrow$) Time		7		7		ns	
t_{PWH}	Clock Pulse Width		HIGH	7		7		ns
t_{PWL}			LOW	7		7		ns
t_{PWL}	Clear ($\overline{CLR} = \text{LOW}$) Pulse Width		7		7		ns	
t_{ZH}	Output Enable Time $\overline{OE} \downarrow$ to Y_i		$C_L = 300\text{pF}$		20		22	ns
t_{ZL}						23		25
t_{ZH}			$C_L = 50\text{pF}$		14		15	ns
t_{ZL}					14		15	ns
t_{HZ}	Output Disable Time $\overline{OE} \uparrow$ to Y_i	$C_L = 50\text{pF}$		16		18	ns	
t_{LZ}					12		12	ns
t_{HZ}		$C_L = 5\text{pF}$		9		10	ns	
t_{LZ}					9		10	ns

Note: 4. See test circuit and waveforms.

SWITCHING WAVEFORMS**SET UP, HOLD, AND RELEASE TIMES**

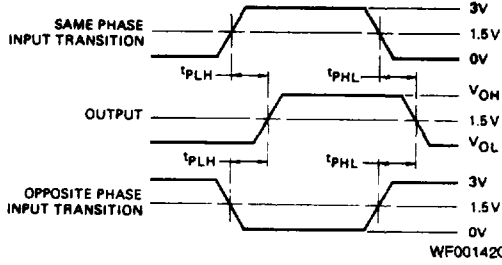
- Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

ENABLE AND DISABLE TIMES

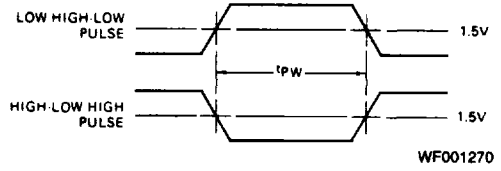
- Notes: 1. Diagram shown for input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $Z_0 = 50\Omega$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

PROPAGATION DELAY



PULSE WIDTH



Note: Pulse Generator for All Pulses: Rate \leq 10MHz; $Z_o = 50\Omega$; $t_r \leq 2.5ns$; $t_f \leq 2.5ns$.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

