

M5M5V416BTP

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V416B is a family of low voltage 4-Mbit static RAMs organized as 262,144-words by 16-bit, fabricated by Mitsubishi's high-performance 0.25µm CMOS technology.

The M5M5V416B is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5V416BTP,RT are packaged in a 44-pin 400mil thin small outline package. M5M5V416BTP (normal lead bend type package), M5M5V416BRT (reverse lead bend type package), both types are very easy to design a printed circuit board.

From the point of operating temperature, the family is divided into three versions; "Standard", "W-version", and "I-version". Those are summarized in the part name table below.

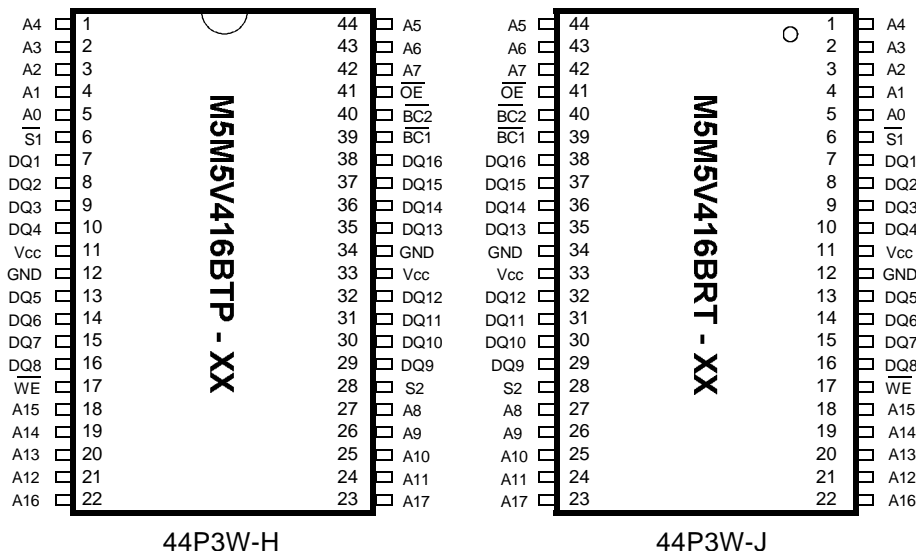
FEATURES

- Single +2.7~+3.6V power supply
- Small stand-by current: 0.3µA(3V,typ.)
- No clocks, No refresh
- Data retention supply voltage=2.0V to 3.6V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by $\overline{S1}$, $\overline{S2}$, $\overline{BC1}$ and $\overline{BC2}$
- Common Data I/O
- Three-state outputs: OR-tie capability
- \overline{OE} prevents data contention in the I/O bus
- Process technology: 0.25µm CMOS
- Package: 44 pin 400mil TSOP (II)

Version, Operating temperature	Part name	Power Supply	Access time max.	Stand-by current Icc(PD), Vcc=3.0V						Active current Icc1 (3.0V, typ.)
				typical *		Ratings (max.)				
				25°C	40°C	25°C	40°C	70°C	85°C	
Standard 0 ~ +70°C	M5M5V416BTP,RT -70L	2.7 ~ 3.6V	70ns	0.3µA	1µA	1µA	3µA	15µA	---	50mA (10MHz) 7mA (1MHz)
	M5M5V416BTP,RT -85L		85ns							
	M5M5V416BTP,RT -70H	2.7 ~ 3.6V	70ns							
	M5M5V416BTP,RT -85H		85ns							
W-version -20 ~ +85°C	M5M5V416BTP,RT -70LW	2.7 ~ 3.6V	70ns	0.3µA	1µA	1µA	3µA	15µA	30µA	
	M5M5V416BTP,RT -85LW		85ns							
	M5M5V416BTP,RT -70HW	2.7 ~ 3.6V	70ns							
	M5M5V416BTP,RT -85HW		85ns							
I-version -40 ~ +85°C	M5M5V416BTP,RT -70LI	2.7 ~ 3.6V	70ns	0.3µA	1µA	1µA	3µA	15µA	30µA	
	M5M5V416BTP,RT -85LI		85ns							
	M5M5V416BTP,RT -70HI	2.7 ~ 3.6V	70ns							
	M5M5V416BTP,RT -85HI		85ns							

* "typical" parameter is sampled, not 100% tested.

PIN CONFIGURATION



Pin	Function
A0 ~ A17	Address input
DQ1 ~ DQ16	Data input / output
$\overline{S1}$	Chip select input 1
$\overline{S2}$	Chip select input 2
\overline{W}	Write control input
\overline{OE}	Output enable input
$\overline{BC1}$	Lower Byte (DQ1 ~ 8)
$\overline{BC2}$	Upper Byte (DQ9 ~ 16)
Vcc	Power supply
GND	Ground supply

Outline: 44P3W-H/J

NC: No Connection

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FUNCTION

The M5M5V416BTP,RT are organized as 262,144-words by 16-bit. These devices operate on a single +2.7~3.6V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs $\overline{BC1}$, $\overline{BC2}$, $\overline{S1}$, $S2$, \overline{W} and \overline{OE} . Each mode is summarized in the function table.

A write operation is executed whenever the low level \overline{W} overlaps with the low level $\overline{BC1}$ and/or $\overline{BC2}$ and the low level $\overline{S1}$ and the high level $S2$. The address(A0~A17) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{BC1}$ and/or $\overline{BC2}$ and $\overline{S1}$ and $S2$ are in an active state($\overline{S1}=L, S2=H$).

When setting $\overline{BC1}$ at the high level and other pins are in an active stage, upper-byte are in a selectable mode in which both reading and writing are enabled, and lower-byte are in a non-selectable mode. And when setting $\overline{BC2}$ at a high level and other pins are in an active stage, lower-byte are in a selectable mode and upper-byte are in a non-selectable mode.

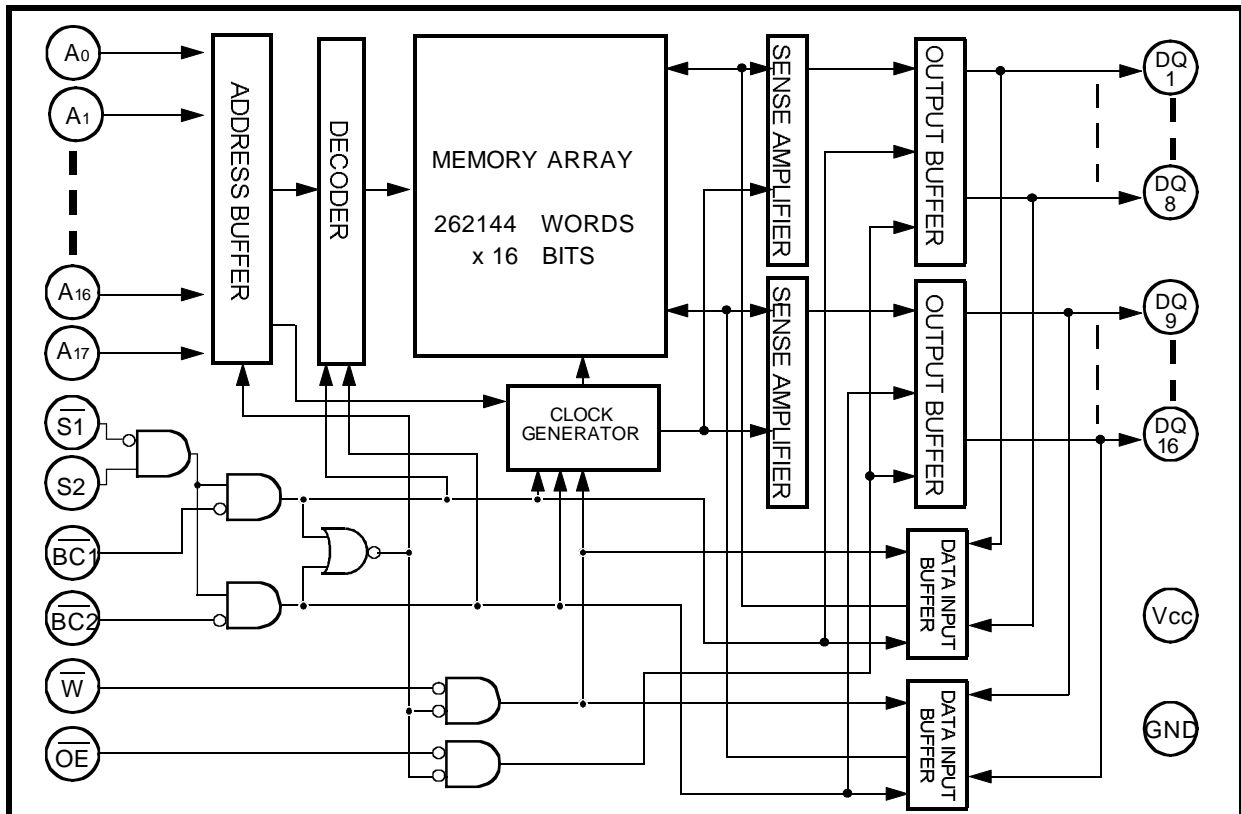
When setting $\overline{BC1}$ and $\overline{BC2}$ at a high level or $\overline{S1}$ at a high level or $S2$ at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{BC1}$, $\overline{BC2}$ and $\overline{S1}$, $S2$.

The power supply current is reduced as low as 0.3 μ A(25°C, typical), and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S1}$	$S2$	$\overline{BC1}$	$\overline{BC2}$	\overline{W}	\overline{OE}	Mode	DQ1-8	DQ9-16	I _{cc}
H	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
L	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
H	H	X	X	X	X	Non selection	High-Z	High-Z	Standby
X	X	H	H	X	X	Non selection	High-Z	High-Z	Standby
L	H	L	H	L	X	Write	Din	High-Z	Active
L	H	L	H	H	L	Read	Dout	High-Z	Active
L	H	L	H	H	H	————	High-Z	High-Z	Active
L	H	H	L	L	X	Write	High-Z	Din	Active
L	H	H	L	H	L	Read	High-Z	Dout	Active
L	H	H	L	H	H	————	High-Z	High-Z	Active
L	H	L	L	L	X	Write	Din	Din	Active
L	H	L	L	H	L	Read	Dout	Dout	Active
L	H	L	L	H	H	————	High-Z	High-Z	Active

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V _{CC}	Supply voltage	With respect to GND	-0.5* ~ +4.6	V
V _I	Input voltage	With respect to GND	-0.5* ~ V _{CC} + 0.5	
V _O	Output voltage	With respect to GND	0 ~ V _{CC}	
P _d	Power dissipation	T _a =25°C	700	mW
T _a	Operating temperature	Standard (-L, -H)	0 ~ +70	°C
		W-version (-LW, -HW)	-20 ~ +85	
		I-version (-LI, -HI)	-40 ~ +85	
T _{stg}	Storage temperature		-65 ~ +150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units	
			Min	Typ	Max		
V _{IH}	High-level input voltage		2.2		V _{CC} +0.3V	V	
V _{IL}	Low-level input voltage		-0.3*		0.6		
V _{OH1}	High-level output voltage 1	I _{OH} = -0.5mA	2.4				
V _{OH2}	High-level output voltage 2	I _{OH} = -0.05mA	V _{CC} -0.5V				
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4	μA	
I _I	Input leakage current	V _I =0 ~ V _{CC}			±1		
I _O	Output leakage current	$\overline{BC1}$ and $\overline{BC2}$ =V _{IH} or $\overline{S1}$ =V _{IH} or S ₂ =V _{IH} or \overline{OE} =V _{IH} , V _{I/O} =0 ~ V _{CC}			±1	mA	
I _{CC1}	Active supply current (AC, MOS level)	$\overline{BC1}$ and $\overline{BC2}$ ≤ 0.2V, $\overline{S1}$ ≤ 0.2V, S ₂ ≥ V _{CC} -0.2V other inputs ≤ 0.2V or ≥ V _{CC} -0.2V Output - open (duty 100%)	f = 10MHz	-	50		70
			f = 1MHz	-	7		15
I _{CC2}	Active supply current (AC, TTL level)	$\overline{BC1}$ and $\overline{BC2}$ =V _{IL} , \overline{S} =V _{IL} , S ₂ =V _{IH} other pins =V _{IH} or V _{IL} Output - open (duty 100%)	f = 10MHz	-	50		70
			f = 1MHz	-	7	15	
I _{CC3}	Stand by supply current (AC, MOS level)	< 1 > $\overline{S1}$ ≥ V _{CC} - 0.2V, other inputs = 0 ~ V _{CC} < 2 > S ₂ ≤ 0.2V, other inputs = 0 ~ V _{CC} < 3 > $\overline{BC1}$ and $\overline{BC2}$ ≥ V _{CC} - 0.2V $\overline{S1}$ ≤ 0.2V, S ₂ ≥ V _{CC} - 0.2V Other inputs=0~V _{CC}	-LW, -LI	+85°C	-	-	80
			-L, -LW, -LI	+70°C	-	-	40
			-HW, -HI	+85°C	-	-	40
			-H, -HW, -HI	+70°C	-	-	20
				+40°C	-	1	5.0
			-H	0 ~ +25°C	-	0.3	2.0
			-HW	-20 ~ +25°C	-	0.3	2.0
	-HI	-40 ~ +25°C	-	0.3	2.0		
I _{CC4}	Stand by supply current (AC, TTL level)	$\overline{BC1}$ and $\overline{BC2}$ =V _{IH} or $\overline{S1}$ =V _{IH} or S ₂ =V _{IL} Other inputs=0 ~ V _{CC}	-	-	0.5	mA	

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

* -3.0V in case of AC (Pulse width ≤ 30ns)

Note 2: Typical value is for V_{CC}=3.0V and T_a=25°C

CAPACITANCE

(V_{CC}=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			10	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	

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AC ELECTRICAL CHARACTERISTICS

(V_{CC}=2.7 ~ 3.6V, unless otherwise noted)

(1) TEST CONDITIONS

Supply voltage	2.7V~3.6V
Input pulse	V _{IH} =2.4V, V _{IL} =0.4V
Input rise time and fall time	5ns
Reference level	V _{OH} =V _{OL} =1.5V Transition is measured ±500mV from steady state voltage. (for t _{en} , t _{dis})
Output loads	Fig.1, CL=30pF CL=5pF (for t _{en} , t _{dis})

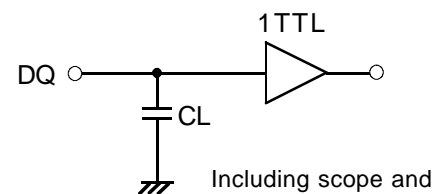


Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits				Units
		70L,70H,70LW 70HW,70LI,70HI		85L,85H,85LW 85HW,85LI,85HI		
		Min	Max	Min	Max	
t _{CR}	Read cycle time	70		85		ns
t _{a(A)}	Address access time		70		85	ns
t _{a(S1)}	Chip select 1 access time		70		85	ns
t _{a(S2)}	Chip select 2 access time		70		85	ns
t _{a(BC1)}	Byte control 1 access time		70		85	ns
t _{a(BC2)}	Byte control 2 access time		70		85	ns
t _{a(OE)}	Output enable access time		35		45	ns
t _{dis(S1)}	Output disable time after $\overline{S1}$ high		25		30	ns
t _{dis(S2)}	Output disable time after S2 low		25		30	ns
t _{dis(BC1)}	Output disable time after $\overline{BC1}$ high		25		30	ns
t _{dis(BC2)}	Output disable time after $\overline{BC2}$ high		25		30	ns
t _{dis(OE)}	Output disable time after \overline{OE} high		25		30	ns
t _{en(S1)}	Output enable time after S1 low	10		10		ns
t _{en(S2)}	Output enable time after S2 high	10		10		ns
t _{en(BC1)}	Output enable time after $\overline{BC1}$ low	10		10		ns
t _{en(BC2)}	Output enable time after $\overline{BC2}$ low	10		10		ns
t _{en(OE)}	Output enable time after \overline{OE} low	5		5		ns
t _{v(A)}	Data valid time after address	10		10		ns

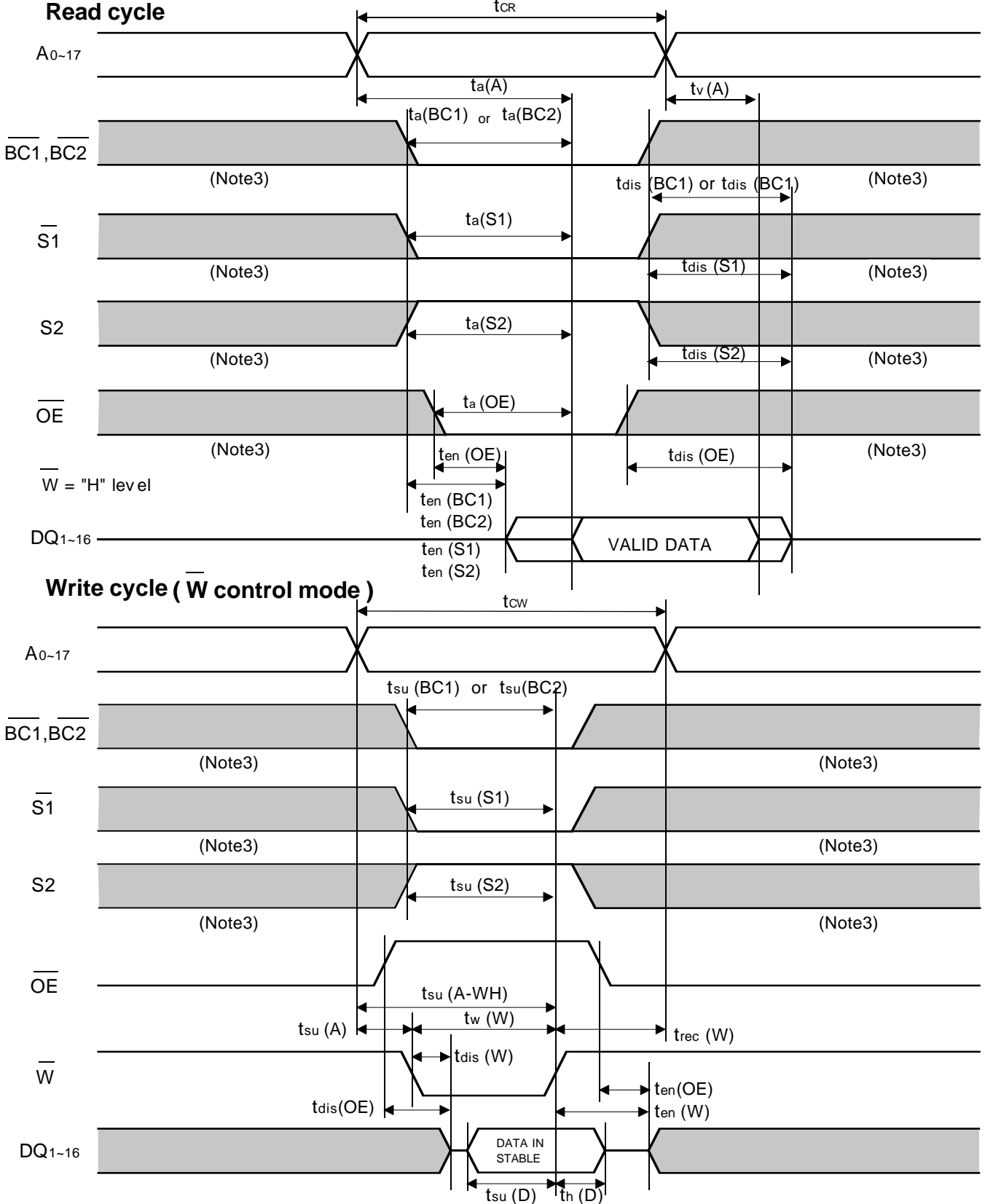
(3) WRITE CYCLE

Symbol	Parameter	Limits				Units
		70L,70H,70LW 70HW,70LI,70HI		85L,85H,85LW 85HW,85LI,85HI		
		Min	Max	Min	Max	
t _{cw}	Write cycle time	70		85		ns
t _{w(W)}	Write pulse width	55		60		ns
t _{su(A)}	Address setup time	0		0		ns
t _{su(A-WH)}	Address setup time with respect to \overline{W}	60		70		ns
t _{su(BC1)}	Byte control 1 setup time	60		70		ns
t _{su(BC2)}	Byte control 2 setup time	60		70		ns
t _{su(S1)}	Chip select 1 setup time	60		70		ns
t _{su(S2)}	Chip select 2 setup time	60		70		ns
t _{su(D)}	Data setup time	35		35		ns
t _{h(D)}	Data hold time	0		0		ns
t _{rec(W)}	Write recovery time	0		0		ns
t _{dis(W)}	Output disable time from \overline{W} low		25		30	ns
t _{dis(OE)}	Output disable time from \overline{OE} high		25		30	ns
t _{en(W)}	Output enable time from \overline{W} high	5		5		ns
t _{en(OE)}	Output enable time from \overline{OE} low	5		5		ns

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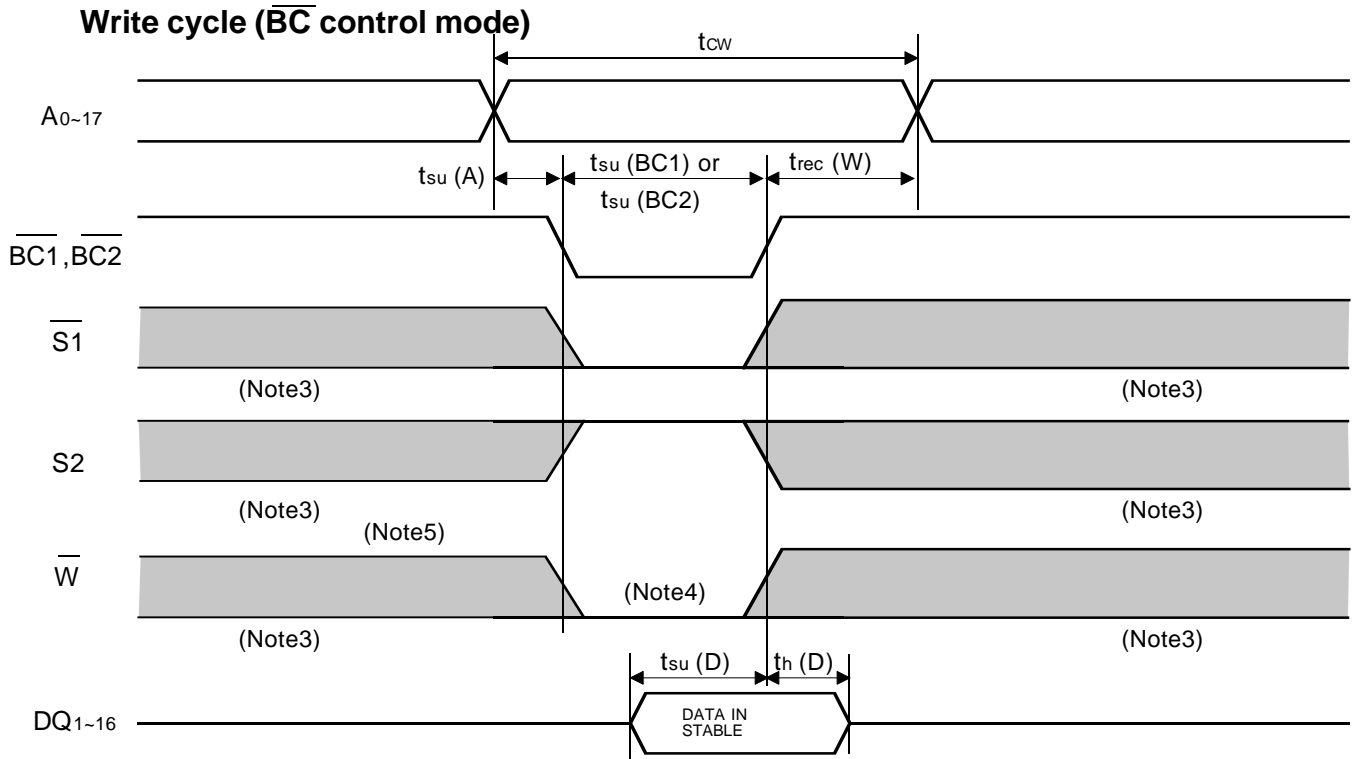
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(4)TIMING DIAGRAMS



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Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during $\overline{S1}$ low, $S2$ high overlaps $\overline{BC1}$ and/or $\overline{BC2}$ low and \overline{W} low.

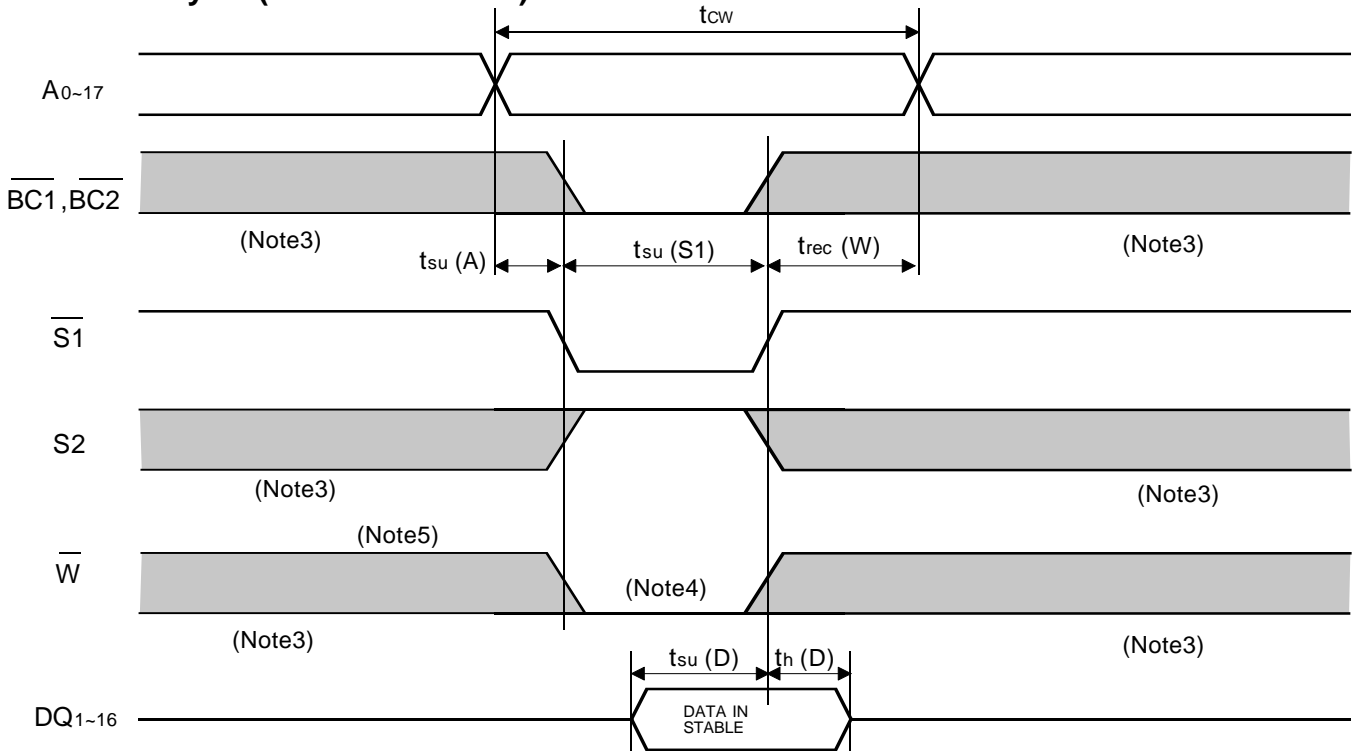
Note 5: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of $\overline{BC1}$ and/or $\overline{BC2}$ or the falling edge of $\overline{S1}$ or rising edge of $S2$, the outputs are maintained in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

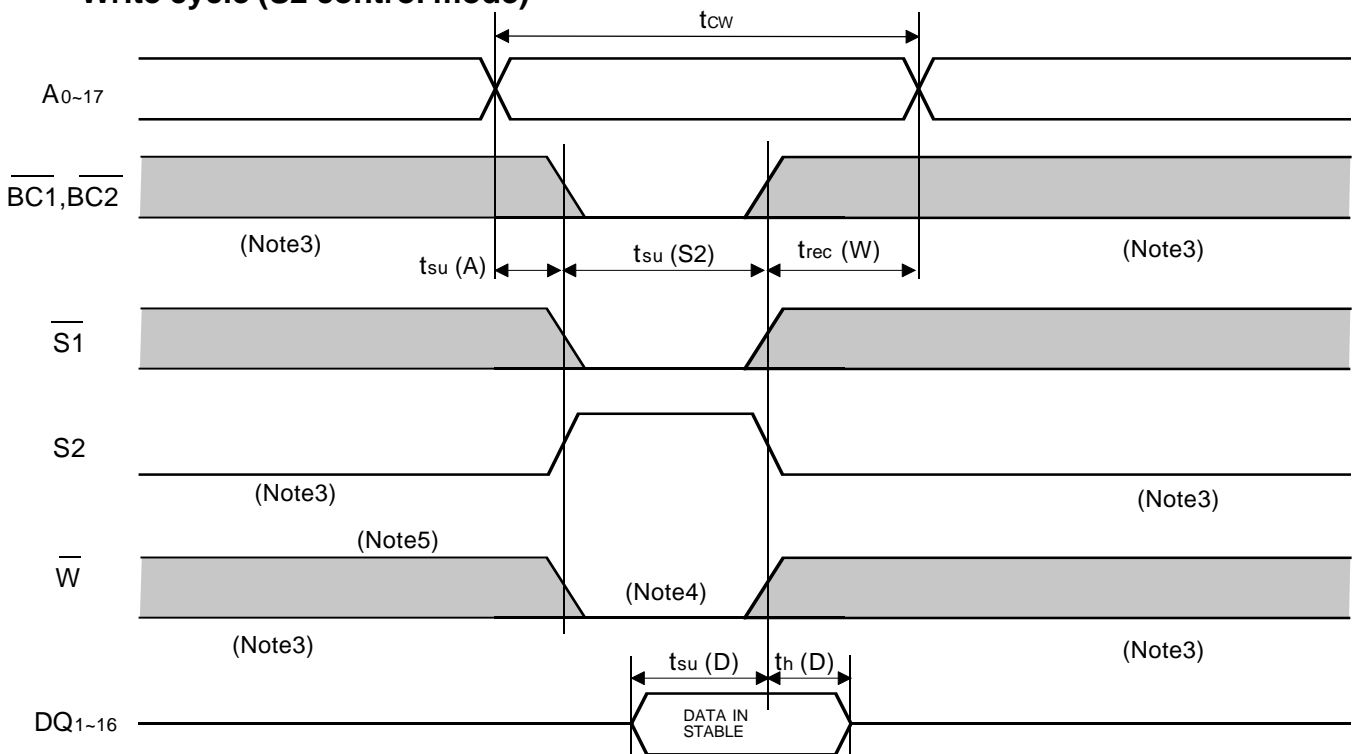
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Write cycle ($\overline{S1}$ control mode)



Write cycle ($S2$ control mode)



M5M5V416BTP

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Units		
			Min	Typ	Max			
V _{CC} (PD)	Power down supply voltage		2.0			V		
V _I (BC)	Byte control input $\overline{BC1}$ & $\overline{BC2}$		2.0			V		
V _I ($\overline{S1}$)	Chip select input $\overline{S1}$		2.0			V		
V _I (S2)	Chip select input S2				0.2	V		
I _{CC} (PD)	Power down supply current	V _{CC} =3.0V	-LW, -LI	+85°C	-	-	60	μA
		< 1 > S1 ≥ V _{CC} - 0.2V	-L, -LW, -LI	+70°C	-	-	30	μA
		S2 ≥ V _{CC} - 0.2V or ≤ 0.2V other inputs=0-3V	-HW, -HI	+85°C	-	-	30	μA
		< 2 > S2 ≤ 0.2V other inputs=0-3V	-H, -HW, -HI	+70°C	-	-	15	μA
				+40°C	-	1	3	μA
		< 3 > BC1 and BC2 ≥ V _{CC} -0.2V S1 ≤ 0.2V or S2 ≥ V _{CC} -0.2V other inputs=0-3V	-H	0 ~ +25°C	-	0.3	1	μA
			-HW	-20 ~ +25°C	-	0.3	1	μA
	-HI	-40 ~ +25°C	-	0.3	1	μA		

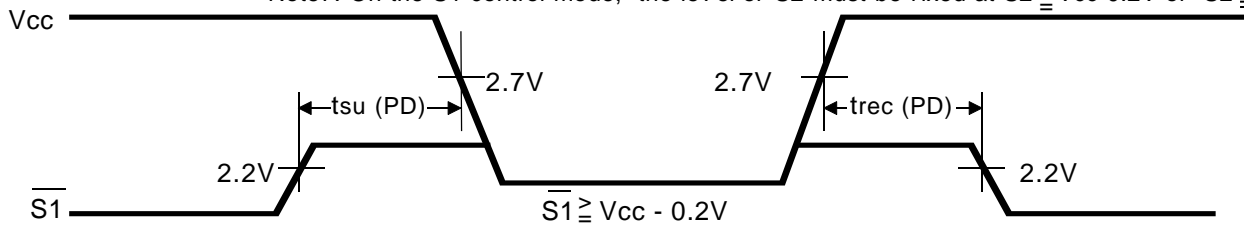
Typical value is for Ta=25°C

(2) TIMING REQUIREMENTS

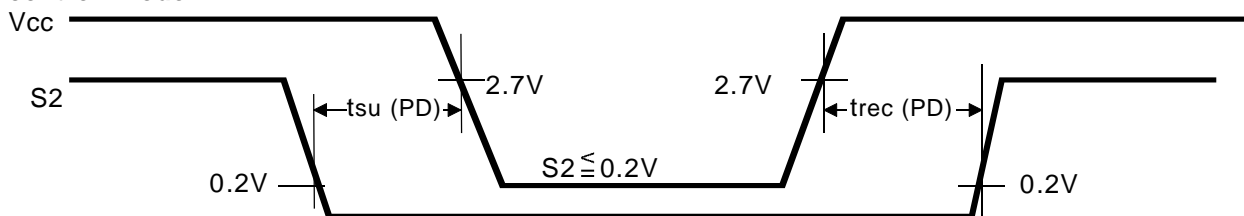
Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

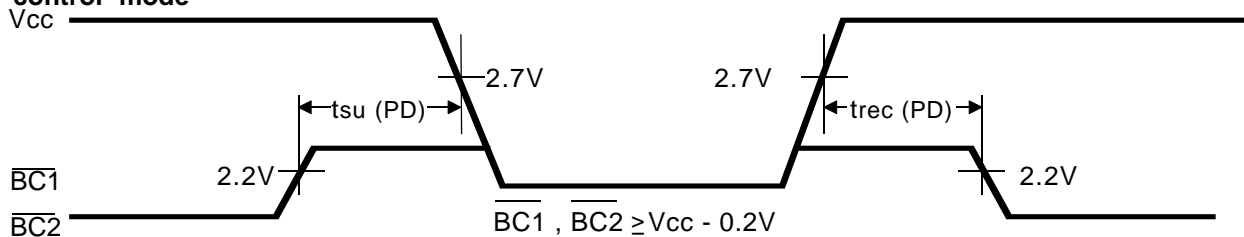
S1 control mode Note7: On the $\overline{S1}$ control mode, the level of S2 must be fixed at S2 ≥ V_{CC}-0.2V or S2 ≤ 0.2V.



S2 control mode



BC control mode



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Revision History

<u>Revision No.</u>	<u>History</u>	<u>Date</u>	<u>Remark</u>
P01	The first edition	'98 . 07 . 07	Preliminary
P02	Pin#28: NC --> S2	'98 . 07 . 14	Preliminary
P03	Font problem fixed	'98 . 08 . 27	Preliminary
P04	70ns version added	'98 . 12 . 16	Preliminary
P05	Icc1/Icc2 revised	'99 . 02 . 10	Preliminary
P06	1) Speed items revised: 100ns deleted 2) Icc3 and Icc(PD) limits revised	'99 . 03 . 10	Preliminary
P07	1) Errata corrected (page 8) 2) tsu(A-WH), tsu(BC1), tsu(BC2), tsu(S1) and tsu(S2) revised from 65ns to 60ns	'99 . 11 . 26	Preliminary
P10	The first product version	'00 . 06 . 01	-----

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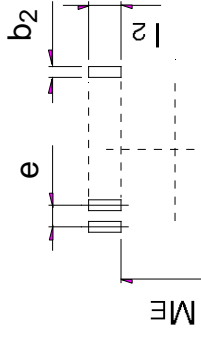
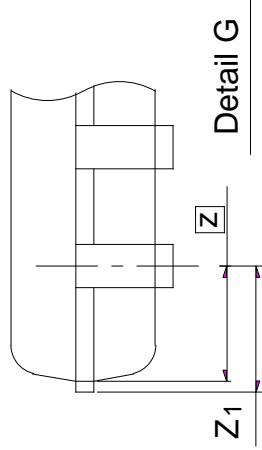
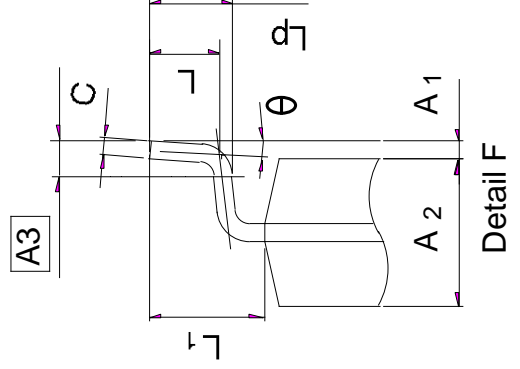
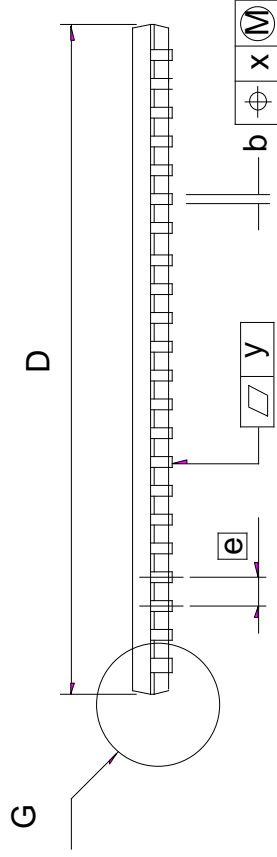
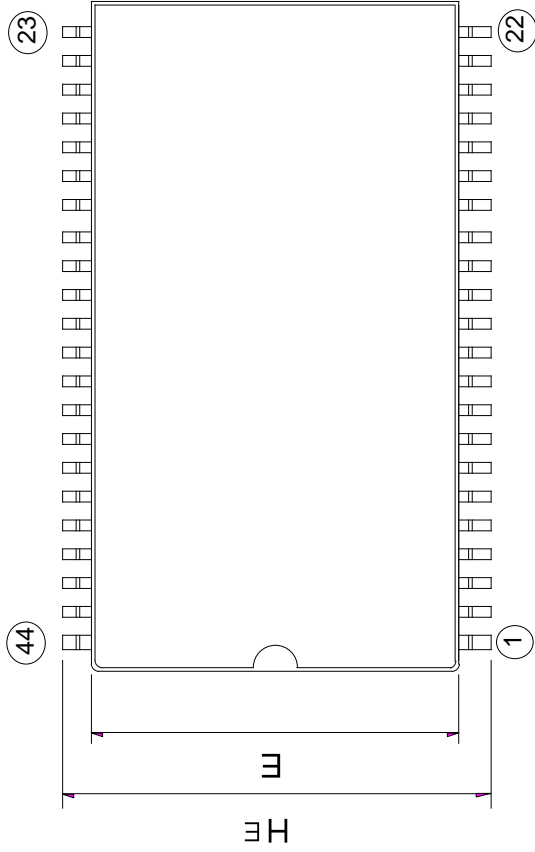
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44P3W-H

Plastic 44pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOPII44-P-400-0.80	—	0.47	Alloy 42

Scale: 3/1



Recommended Mount Pad

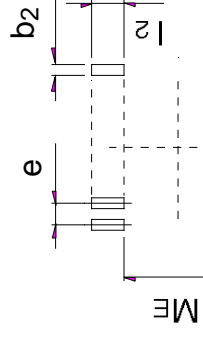
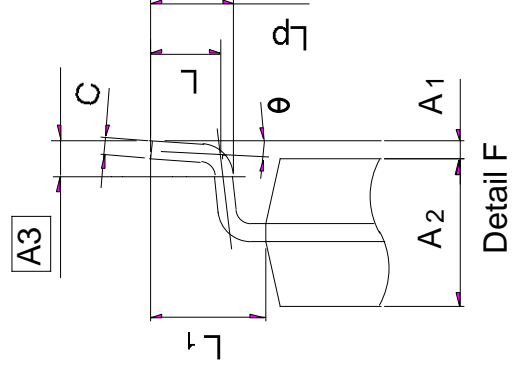
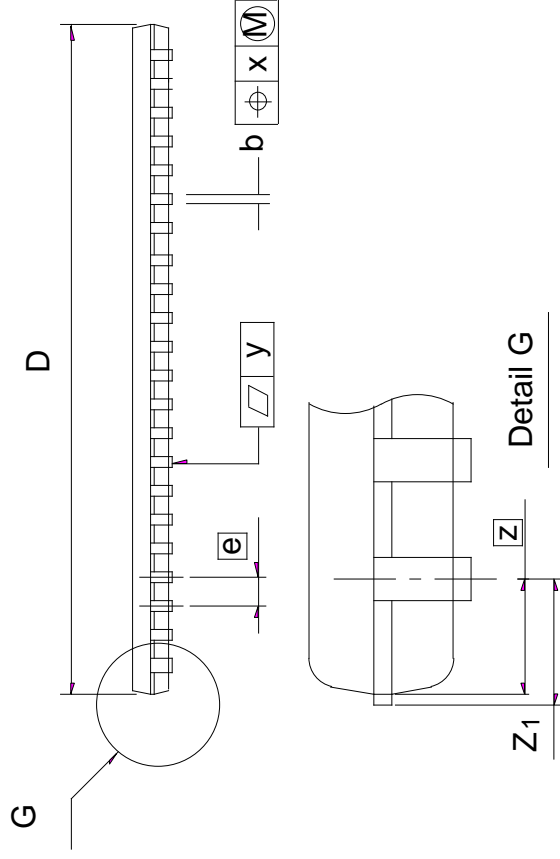
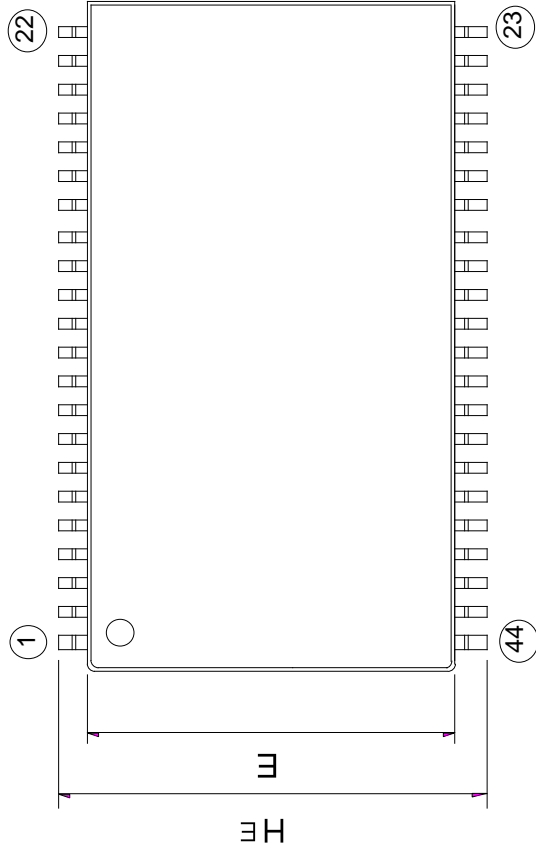
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A1	0.05	0.125	0.2
A2	—	1.0	—
b	0.3	0.35	0.45
c	0.105	0.125	0.175
D	18.31	18.41	18.51
E	10.06	10.16	10.26
e	—	0.8	—
HE	11.56	11.76	11.96
L	0.4	0.5	0.6
L1	—	0.8	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
Z	—	0.805	—
Z1	—	—	0.955
x	—	—	0.16
y	—	—	0.1
theta	0°	—	10°
ME	—	10.36	—
l2	0.9	—	—
b2	—	0.5	—

44P3W-J

Plastic 44pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOPII44-P-400-0.80	—	0.47	Alloy 42

Scale: 3/1



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A1	0.05	0.125	0.2
A2	—	1.0	—
b	0.3	0.35	0.45
c	0.105	0.125	0.175
D	18.31	18.41	18.51
E	10.06	10.16	10.26
e	—	0.8	—
HE	11.56	11.76	11.96
L	0.4	0.5	0.6
L1	—	0.8	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
Z	—	0.805	—
Z1	—	—	0.955
x	—	—	0.16
y	—	—	0.1
theta	0°	—	10°
ME	—	10.36	—
l2	0.9	—	—
b2	—	0.5	—