54/7474 01153O
54H/74H74 01153H
54S/74S74 01153S
54LS/74LS74 01153J

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '74 devices are dual D-type flip-flops with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

TRUTH TABLE
(Each Half)

INPUT	OUTPUTS	
@ t_n	@ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

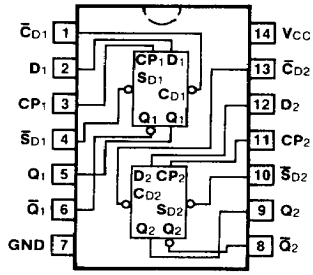
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

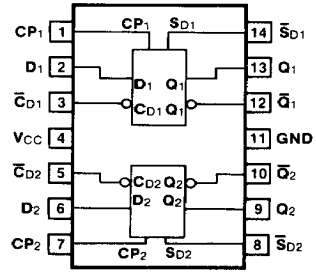
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7474PC, 74H74PC 74S74PC, 74LS74PC		9A
Ceramic DIP (D)	A	7474DC, 74H74DC 74S74DC, 74LS74DC	5474DM, 54H74DM 54S74DM, 54LS74DM	6A
Flatpak (F)	A	74S74FC, 74LS74FC	54S74FM, 54LS74FM	3I
	B	7474FC, 74H74FC	5474FM, 54H74FM	

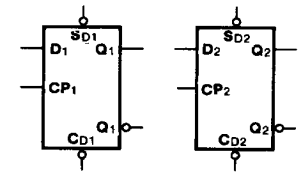
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



LOGIC SYMBOL

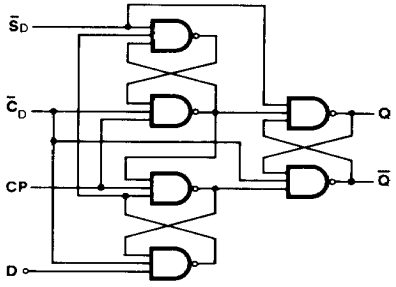


V_{CC} = Pin 14 (4)
GND = Pin 7 (11)

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
D_1, D_2	Data Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	2.0/2.0	2.5/2.5	2.5/2.5	1.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	3.0/2.0	3.75/2.5	3.75/3.75	1.5/0.75
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.0/1.0	2.5/1.25	2.5/2.5	1.0/0.5
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		30		42		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V
		XC		30		50		50		8.0		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74H C_L = 25 pF, R_L = 280 Ω Min	54/74H Max	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	15		35		75		30		MHz	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$		25		15		9.0		25	ns	Figs. 3-1, 3-8
t_{PHL}			40		20		11		35		
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		25		20		6.0		15	ns	$V_{CP} \geq 2.0$ V Figs. 3-1, 3-10
t_{PHL}			40		30		13.5		35		
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		25		20		6.0		15	ns	$V_{CP} \leq 0.8$ V Figs. 3-1, 3-10
t_{PHL}			40		30		8.0		24		

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74H		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max	Min	Max		
t_s (H)	Setup Time HIGH D_n to CP_n	20		10		3.0		10		ns	Fig. 3-6
t_h (H)	Hold Time HIGH D_n to CP_n	5.0		0		0		5.0		ns	
t_s (L)	Setup Time LOW D_n to CP_n	20		15		3.0		20		ns	Fig. 3-6
t_h (L)	Hold Time LOW D_n to CP_n	5.0		0		0		5.0		ns	
t_w (H) t_w (L)	CP_n Pulse Width	30 37		15 13.5		6.0 7.3		18 15.5		ns	Fig. 3-8
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	30		25		7.0		15		ns	Fig. 3-10