W83C17

Winbond

MOTHERBOARD CLOCK CHIP

GENERAL DESCRIPTION

The W83C17 Motherboard Clock Chip is a solid state dual phase-locked loop frequency synthesizer designed to offer jitter-free and low skew clocking for green PC motherboard applications. This frequency synthesizer generates three simultaneous clocks. One clock, REFCLK, is a fixed output frequency (14.318 MHz) which is the same as the input reference crystal (or clock). The second clock, PCLK, is a fixed output frequency which is 24 MHz when the input reference clock frequency is 14.318 MHz. The third clock, CPUCLK, is a programmable CPU clock, with up to eight selectable preprogrammed frequencies stored in an internal ROM. In addition to the industry standard frequency sets, Winbond also offers customized frequency sets (within the frequency range up to 135 MHz) to accommodate unique requirements. Contact Winbond's local sales representatives for further details.

The W83C17 has integrated advanced power management capabilities to support green PC applications. System power management can be achieved by switching the CPUCLK to slower speed (low power mode, 2/4/8 MHz optional), or by disabling the output buffers of CPUCLK and PCLK (stop mode). This clock generator also permits smooth and glitch-free transitions when frequency is changed or low power mode (or stop mode) is enabled.

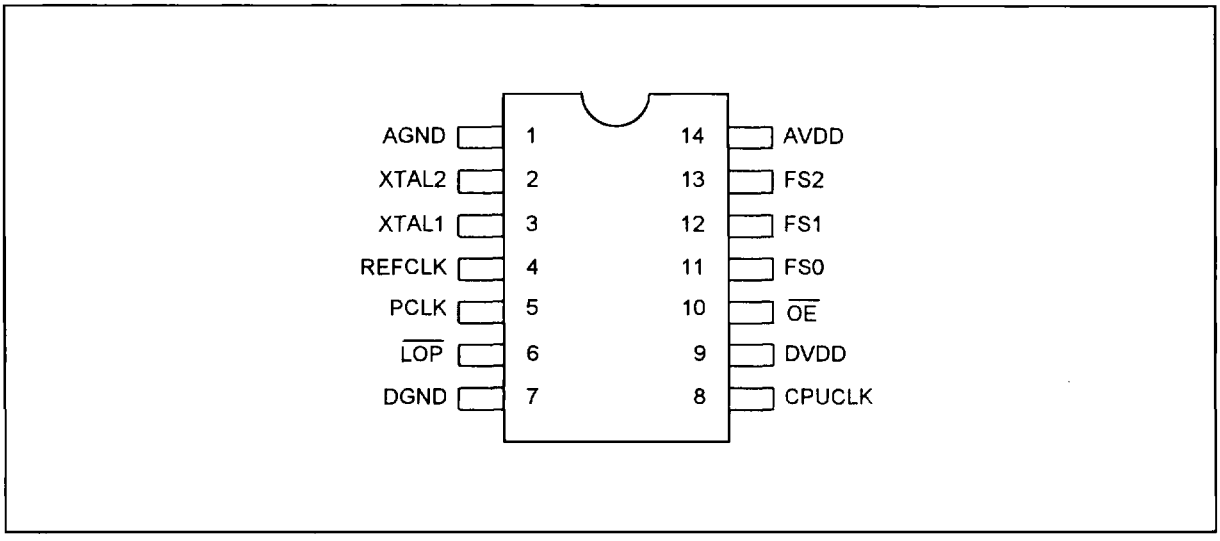
The reference clock source is typically a series-resonant crystal connected across the XTAL1 and XTAL2 pins or an externally generated reference clock connected to the XTAL1 pin. In the latter case, the XTAL2 pin should be left open. For IBM® PC or compatible systems, the crystal frequency typically is 14.318 MHz.

FEATURES

- Clock generator for IBM PC/AT® system
- Mask programmable for CPU clock frequencies up to 135 MHz
- Generates three buffered clock outputs simultaneously (14.318 MHz, 24 MHz, and a CPU clock)
- On-chip loop filters to provide glitch-free frequency transition
- Advanced PLL for low phase jitter
- Provides advanced power management capabilities, including low power mode (2/4/8 MHz optional) and stop mode (0 Hz) for green PC applications
- Subsequent clock period changed under 0.1% while switching frequencies
- Advanced low power CMOS technology
- 14-pin plastic DIP or SOP package

Publication Release Date: June 1994
Revision A1

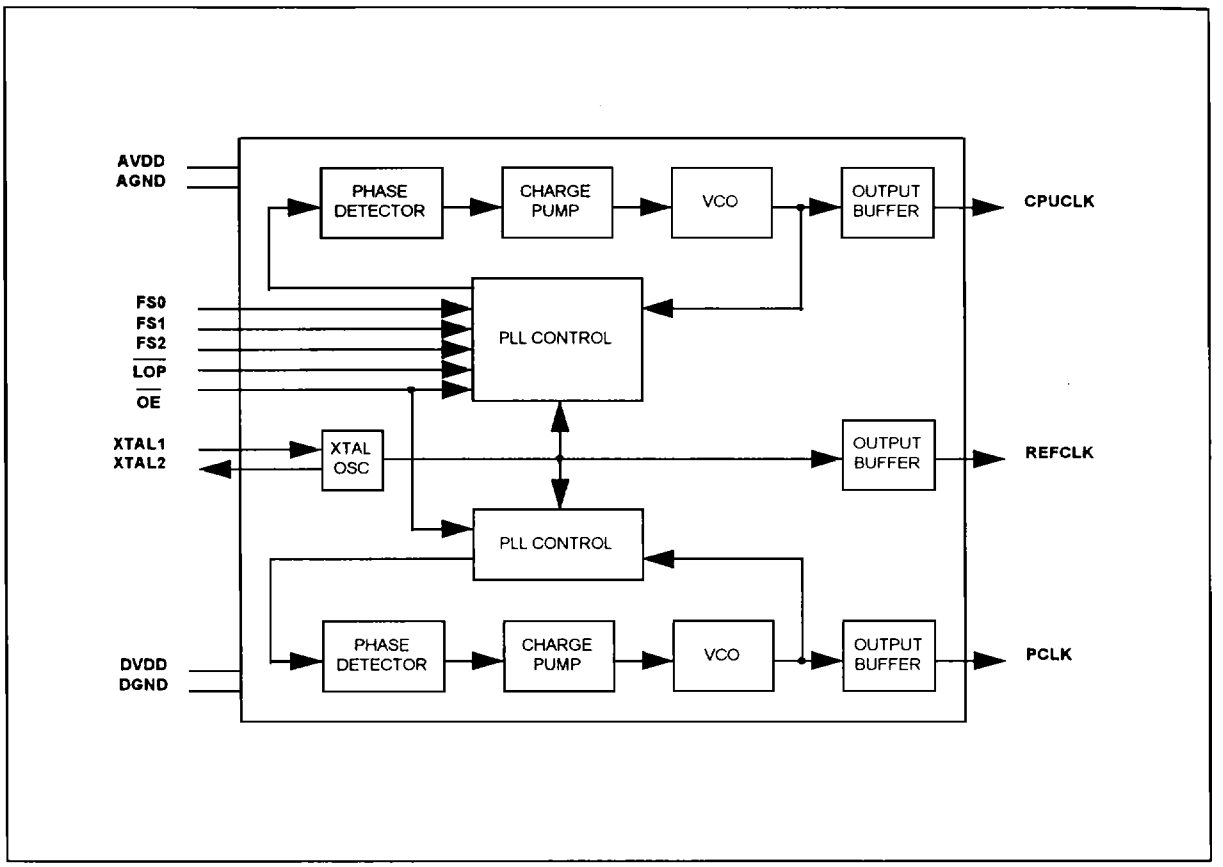
PIN CONFIGURATION



PIN DESCRIPTION

NAME	NUMBER	TYPE	DESCRIPTION
AGND	1		Analog ground.
XTAL2	2	O	Crystal output (no connection when clock used).
XTAL1	3	I	Crystal input or input clock frequency. Typically 14.318 MHz system clock.
REFCLK	4	O	Crystal output which rebuffers the reference input clock or crystal frequency (typically 14.318 MHz).
PCLK	5	O	Peripheral clock output. Typically 24 MHz.
$\overline{LOP}$	6	I	Low power. When asserted low, the CPUCLK gradually transits to 2/4/8 MHz. Internal pull-up.
DGND	7		Digital ground.
CPUCLK	8	O	CPU clock output (see decoding table).
DV_{DD}	9		Digital power supply.
$\overline{OE}$	10	I	Output enable. When asserted high, PCLK and CPUCLK stop to low. Internal pull-down.
FS0	11	I	Frequency select 0 (see decoding table). Internal pull-up.
FS1	12	I	Frequency select 1 (see decoding table). Internal pull-up.
FS2	13	I	Frequency select 2 (see decoding table). Internal pull-up.
AV_{DD}	14		Analog power supply.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The W83C17 Motherboard Clock Chip is a dual phase-locked loop frequency synthesizer capable of generating three clock outputs for a PC system. REFCLK (pin 4) provides the crystal oscillation frequency (14.318 MHz). PCLK (pin 5) provides the peripheral clock frequency (24 MHz). CPUCLK (pin 8) provides the CPU clock frequency, which is programmable through three selectable pins (FS0, FS1, and FS2) based on the decoding table. This device also has advanced power management features, including low power mode and stop mode.

Low Power Mode

The low power mode gradually transits the CPUCLK to 2/4/8 MHz to allow for system power saving.

Stop Mode

The stop mode feature stops the PCLK and CPUCLK to allow for CPU stop mode operation.

Frequency Decoding Table

(Assumes a 14.318 MHz input. Unit: MHz)

$\overline{OE}$	$\overline{LOP}$	FS2	FS1	FS0	CPUCLK	PCLK	REFCLK
1	X	X	X	X	0	0	14.318
0	0	X	X	X	8	24	14.318
0	1	0	0	0	33.3	24	14.318
0	1	0	0	1	80	24	14.318
0	1	0	1	0	66.6	24	14.318
0	1	0	1	1	50	24	14.318
0	1	1	0	0	40	24	14.318
0	1	1	0	1	60	24	14.318
0	1	1	1	0	25	24	14.318
0	1	1	1	1	20	24	14.318

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
V_{DD}	Supply voltage	-0.5	7	V
V_{IN}	Input voltage	-0.5	V_{DD} +0.5	V
V_{OUT}	Output voltage	-0.5	V_{DD} +0.5	V
T_O	Operating temperature	0	70	°C
T_{STG}	Storage temperature	-65	150	°C
P_D	Power dissipation		0.5	W

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to ≥ GND and ≤ V_{DD}.

DC CHARACTERISTICS

(V_{DD}= 4.5 V to 5.5 V, V_{SS}= 0 V, T_A= 0° C to 70° C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
V_{DD}	Operating voltage range	4.5	5.5	V
V_{IL}	Input low voltage	V_{SS}	0.8	V
V_{IH}	Input high voltage	2.0	V_{DD}	V
V_{OL}	Output low voltage	-	0.4	V

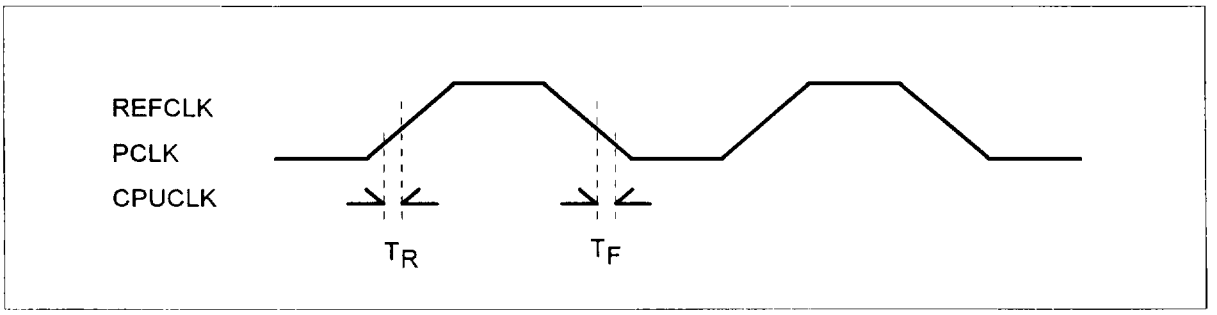
DC characteristics, continued

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
VOH	Output high voltage	2.4	-	V
IDD	Supply current (Note 1)	-	35	mA
IIL	Input low leakage current	-	10	μA
IIH	Input high leakage current	-	-5	μA
RUP	Internal pull-up resistance	50	200	KΩ
RDOWN	Internal pull-down resistance	50	200	KΩ
CIN	Input pin capacitance	-	8	pF
COUT	Output pin capacitance	-	8	pF

Note: No load, 14.318 MHz crystal input, and CPUCLK running at 80 MHz.

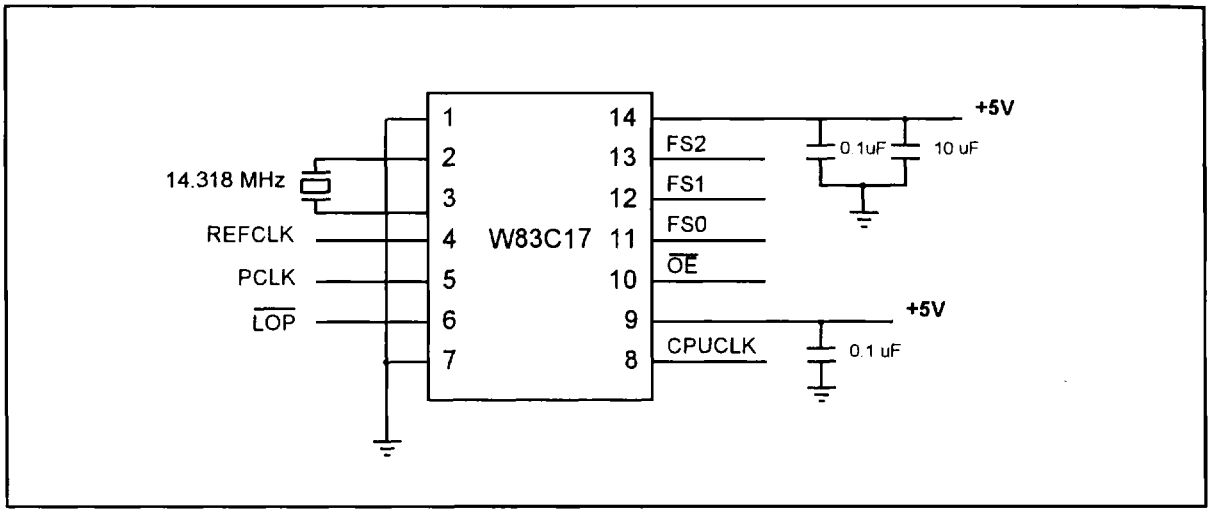
AC CHARACTERISTICS

Output Clock Timing



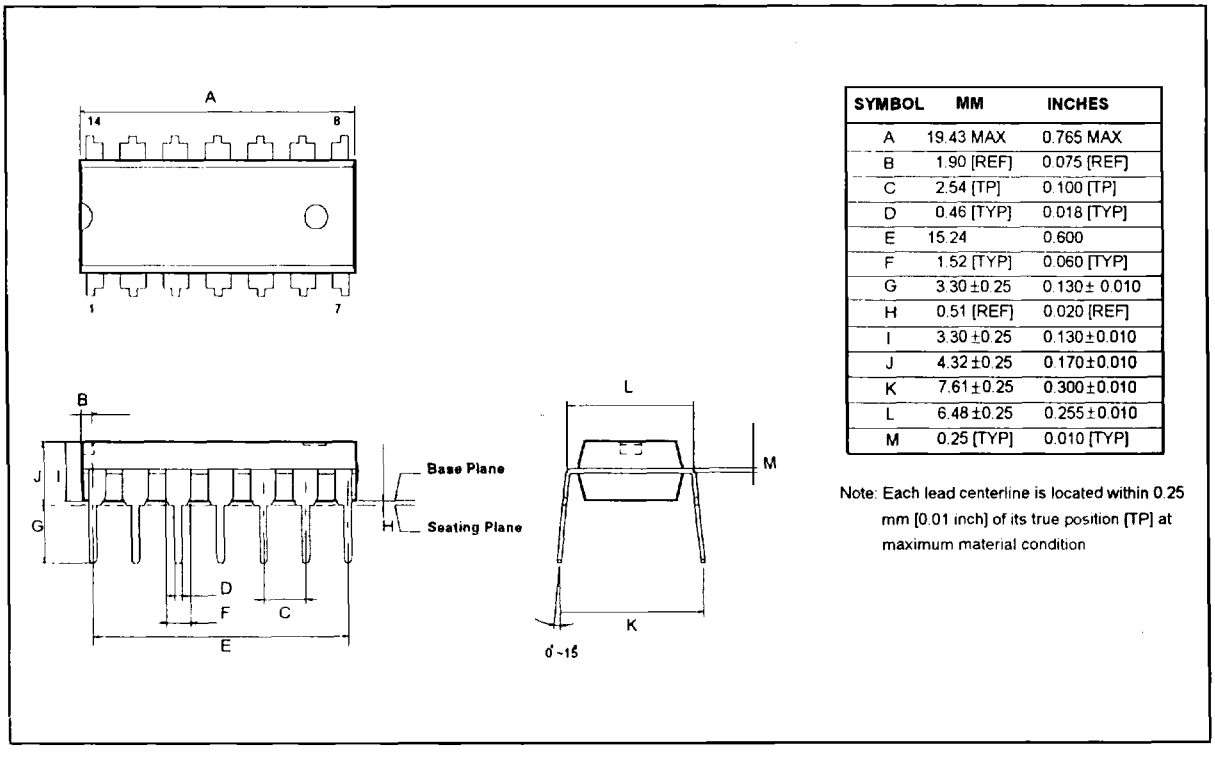
SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTES
TR	Output clock rise time	-	2.0	-	nS	25 pF load
TF	Output clock fall time	-	2.0	-	nS	25 pF load
DT	Output clock duty cycle	-	50	-	%	25 pF load
FE	Frequency error	-	-	0.5	%	All frequencies
FMAX	Maximum frequency	-	-	135	MHz	Per customer request

APPLICATION CIRCUIT



PACKAGE DIMENSIONS

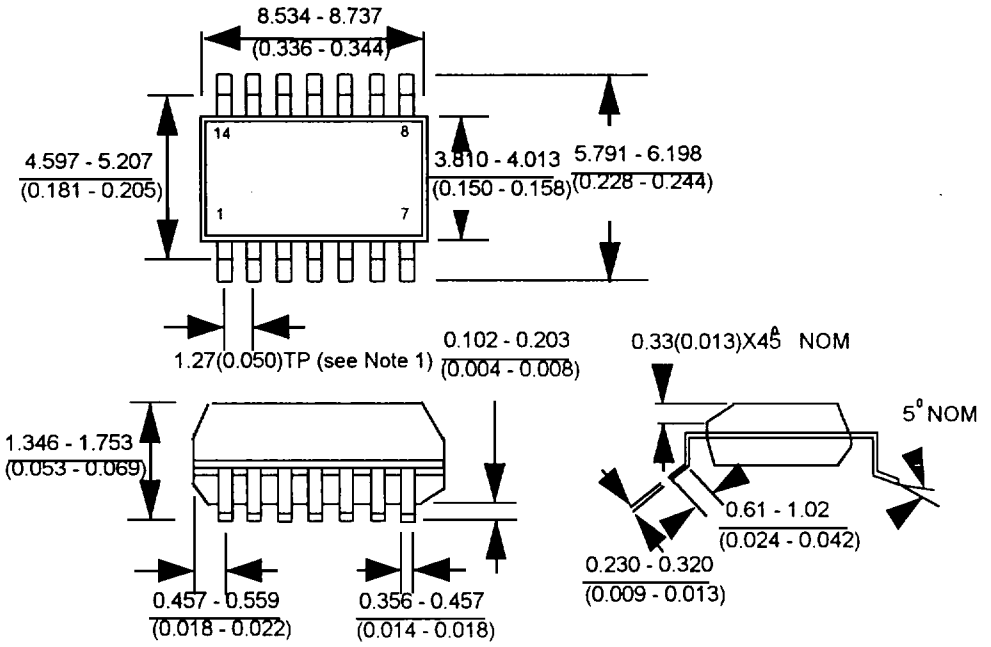
14-Pin Plastic DIP (300 mil)



SYMBOL	MM	INCHES
A	19.43 MAX	0.765 MAX
B	1.90 [REF]	0.075 [REF]
C	2.54 [TP]	0.100 [TP]
D	0.46 [TYP]	0.018 [TYP]
E	15.24	0.600
F	1.52 [TYP]	0.060 [TYP]
G	3.30±0.25	0.130± 0.010
H	0.51 [REF]	0.020 [REF]
I	3.30±0.25	0.130±0.010
J	4.32±0.25	0.170±0.010
K	7.61±0.25	0.300±0.010
L	6.48±0.25	0.255±0.010
M	0.25 [TYP]	0.010 [TYP]

Note: Each lead centerline is located within 0.25 mm [0.01 inch] of its true position [TP] at maximum material condition

14-Pin Plastic SOP (150 mil)



Note 1: Leads are within 0.25 (0.010) radius of true position at maximum material condition.

2: All linear dimensions are in millimeters and parenthetically in inches.

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