

Philips Components

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ECL Products	

100151

Hex D-Type Master-Slave Flip-Flop

FEATURES

- Typical propagation delay: 1.7ns
- Typical supply current ($-I_{EE}$): 137mA

DESCRIPTION

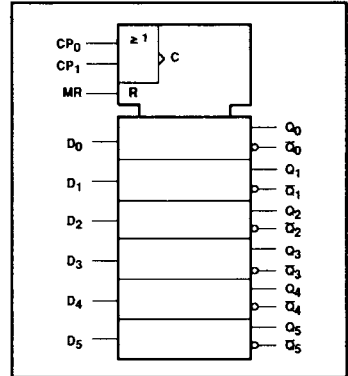
The 100151 contains six flip-flops with Complement and True data outputs, a master reset (MR) and a pair of common clock inputs. Data enters the flip-flop on the Low-to-High transition of one of two clock inputs.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE} .

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
CP_0, CP_1	Common Clock Inputs
MR	Master Reset Input
$Q_0 - Q_5$	True Data Outputs
$\bar{Q}_0 - \bar{Q}_5$	Complementary Data Outputs

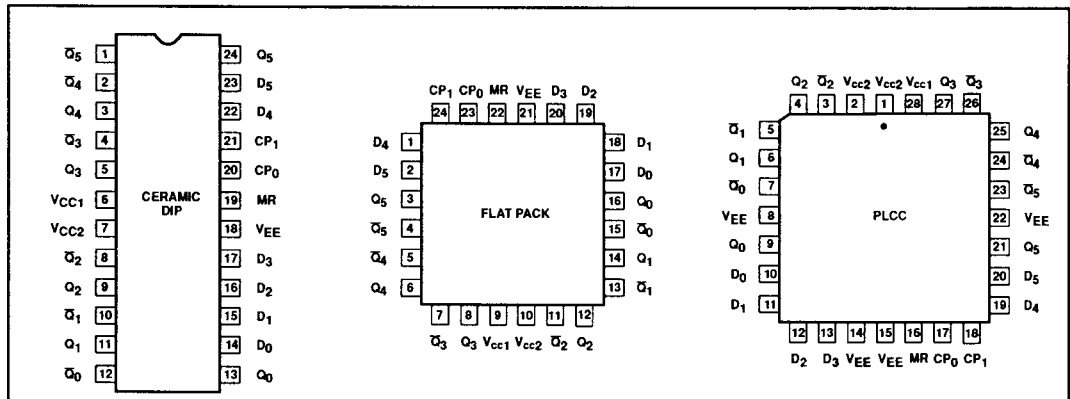
IEC/IEEE SYMBOL



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP (400 mils wide)	100151F
24-Pin Ceramic Flat Pack	100151Y
28-Pin PLCC	100151A

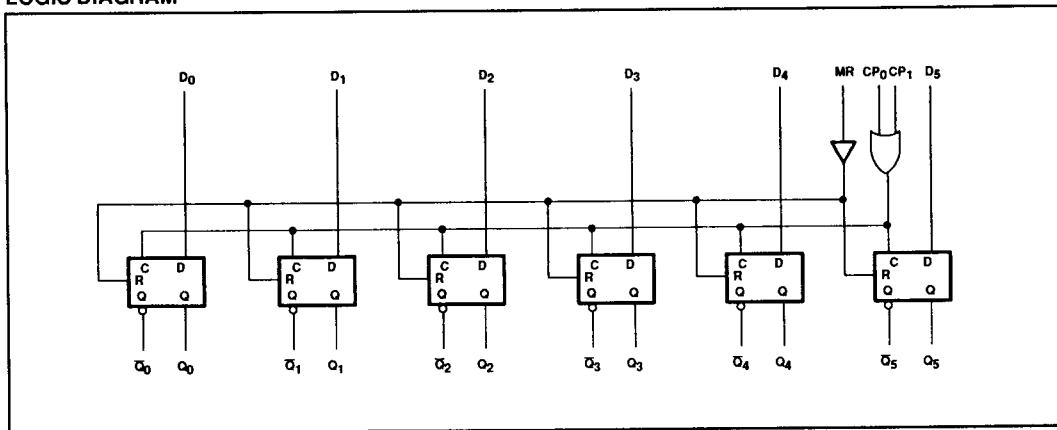
PIN CONFIGURATIONS



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
D _n	CP ₀	CP ₁	MR	Q _n	Q _n
H	L	↑	L	L	H
L	L	↑	L	H	L
H	↑	L	L	L	H
L	↑	L	L	H	L
X	X	H	L	NC	NC
X	H	X	L	NC	NC
X	X	X	H	H	L
X	L	L	L	NC	NC

NOTES:

- H = High voltage level
- L = Low voltage level
- X = Don't care
- NC = No change
- ↑ = Low-to-High transition

ABSOLUTE MAXIMUM RATINGS V_{CC1} = V_{CC2} = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V _{EE}	Supply voltage range	-7.0 to +0.5	V
V _{IN}	Input voltage (V _{IN} should never be more negative than V _{EE})	V _{EE} to +0.5	V
I _O	Output source current (continuous)	-55	mA
T _S	Storage temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+150	°C

NOTE:

Operation beyond the limits set forth in this table may impair the useful life of the device.

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DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V _{CC1} , V _{CC2}	Circuit ground		0	0	0	V
V _{EE}	Supply voltage		-4.8	-4.5	-4.2	V
V _{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		-5.7			V
V _{IH}	High level input voltage	V _{EE} = -4.2V	-1150		-880	mV
		V _{EE} = -4.5V	-1165			
		V _{EE} = -4.8V	-1165			
V _{IL}	Low level input voltage	V _{EE} = -4.2V	-1810		-1475	mV
		V _{EE} = -4.5V			-1475	mV
		V _{EE} = -4.8V			-1490	mV
T _A	Operating ambient temperature range		0	+25	+85	°C

NOTE:

When operating at other than the specified V_{EE} voltages (-4.2V, -4.5V, -4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS V_{CC1} = V_{CC2} = ground, V_{EE} = -4.8V to -4.2V, T_A = 0°C to +85°C unless otherwise specified^{1,3,4}

SYMBOL	PARAMETER	TEST CONDITIONS ²	LIMITS			UNIT		
			MIN.	TYP.	MAX.			
V _{OH}	High level output voltage	Inputs at V _{IHMAX} or V _{ILMIN}	V _{EE} = -4.2V	-1020		-870	mV	
			V _{EE} = -4.5V	-1025	-955	-880	mV	
			V _{EE} = -4.8V	-1035		-880	mV	
V _{OHT}	High level output threshold voltage	Outputs loaded with 50Ω to -2.0V ±0.010V	Apply V _{IHMIN} or V _{ILMAX} to one input at a time. Other inputs at V _{IHMAX} or V _{ILMIN} .	V _{EE} = -4.2V	-1030			mV
				V _{EE} = -4.5V	-1035			mV
				V _{EE} = -4.8V	-1045			mV
V _{OLT}	Low level output threshold voltage	with 50Ω to -2.0V ±0.010V	Apply V _{IHMIN} or V _{ILMAX} to input at a time. Other inputs at V _{IHMAX} or V _{ILMIN} .	V _{EE} = -4.2V			-1595	mV
				V _{EE} = -4.5V			-1610	mV
				V _{EE} = -4.8V			-1610	mV
V _{OL}	Low level output voltage	Inputs at V _{IHMAX} or V _{ILMIN} .	V _{EE} = -4.2V	-1810		-1605	mV	
			V _{EE} = -4.5V	-1810	-1705	-1620	mV	
			V _{EE} = -4.8V	-1830		-1620	mV	
I _{IH}	High level input current	MR D _n E _n	One input under test at V _{IHMAX} . Other inputs at V _{ILMIN} .				450	μA
							340	μA
							520	μA
I _{IL}	Low level input current	One input under test at V _{ILMIN} . Other inputs at V _{IHMAX} .	0.5			μA		
-I _{EE}	V _{EE} supply current	All inputs at V _{IHMAX}	98	137	210	mA		

NOTES:

- The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
- Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.

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NOTES (CONTINUED):

3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to $V_{EE} = -5.7V$, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1	375		375		375		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or \bar{Q}_n	Waveforms 1,2	0.80 0.80	2.20 2.20	0.80 0.80	2.20 2.20	0.90 0.90	2.40 2.40	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or \bar{Q}_n	Waveform 2	0.80 0.80	2.90 2.90	0.80 0.80	3.00 3.00	0.90 0.90	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time Q_n or \bar{Q}_n	Waveform 1	0.45 0.45	1.70 1.70	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time, D_n to CP_n	Waveform 2	0.70		0.70		0.70		ns
t_h	Hold time, CP_n to D_n		0.70		0.70		0.70		ns
t_R	Release time, MR to CP_n		2.30		2.30		2.30		ns
$t_w(H)$	Pulse width CP_n , MR	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1	375		375		375		
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or \bar{Q}_n	Waveforms 1,2	0.80 0.80	2.20 2.20	0.80 0.80	2.20 2.20	0.90 0.90	2.40 2.40	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or \bar{Q}_n	Waveform 2	0.80 0.80	2.90 2.90	0.80 0.80	3.00 3.00	0.90 0.90	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time Q_n or \bar{Q}_n	Waveform 1	0.45 0.45	1.70 1.70	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time, D_n to CP_n	Waveform 2	0.95		0.90		0.95		ns
t_h	Hold time, CP_n to D_n		0.70		0.70		0.70		ns
t_R	Release time, MR to CP_n		2.30		2.30		2.30		ns
$t_w(H)$	Pulse width CP_n , MR	Waveforms 1,2	2.50		2.50		2.50		ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

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AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8\text{V to } -4.2\text{V}$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1	375		375		375		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or \bar{Q}_n	Waveforms 1,2	0.80 0.80	2.00 2.00	0.80 0.80	2.00 2.00	0.90 0.90	2.20 2.20	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or \bar{Q}_n	Waveform 2	0.80 0.80	2.70 2.70	0.80 0.80	2.80 2.80	0.90 0.90	2.90 2.90	ns ns
t_{TLH} t_{THL}	Transition time Q_n or \bar{Q}_n	Waveform 1	0.45 0.45	1.70 1.70	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time, D_n to CP_n	Waveform 2	0.60		0.60		0.60		ns
t_h	Hold time, CP_n to D_n		0.60		0.60		0.60		ns
t_R	Release time, MR to CP_n		2.20		2.20		2.50		ns
$t_w(\text{H})$	Pulse width CP_n , MR	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2\text{V} \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1	375		375		375		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or \bar{Q}_n	Waveforms 1,2	0.80 0.80	2.00 2.00	0.80 0.80	2.00 2.00	0.90 0.90	2.20 2.20	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or \bar{Q}_n	Waveform 2	0.80 0.80	2.70 2.70	0.80 0.80	2.80 2.80	0.90 0.90	2.90 2.90	ns ns
t_{TLH} t_{THL}	Transition time Q_n or \bar{Q}_n	Waveform 1	0.45 0.45	1.70 1.70	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time, D_n to CP_n	Waveform 2	0.75		0.70		0.75		ns
t_h	Hold time, CP_n to D_n		0.60		0.60		0.60		ns
t_R	Release time, MR to CP_n		2.20		2.20		2.50		ns
$t_w(\text{H})$	Pulse width CP_n , MR	Waveforms 1,2	2.50		2.50		2.50		ns

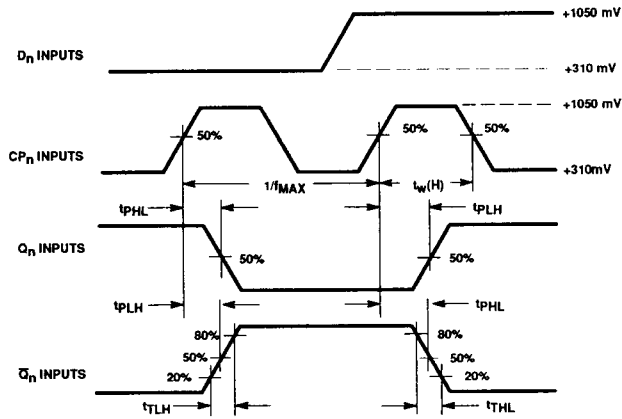
NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

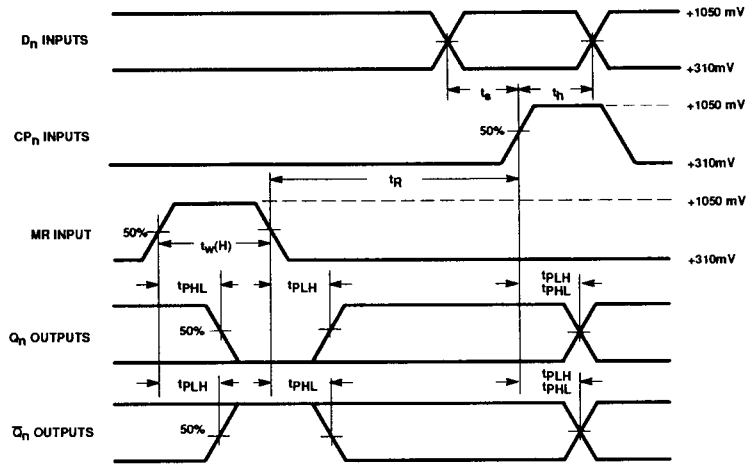
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AC WAVEFORMS



Waveform 1. Propagation Delays and Transition Times



Waveform 2. Reset, Setup and Hold Times

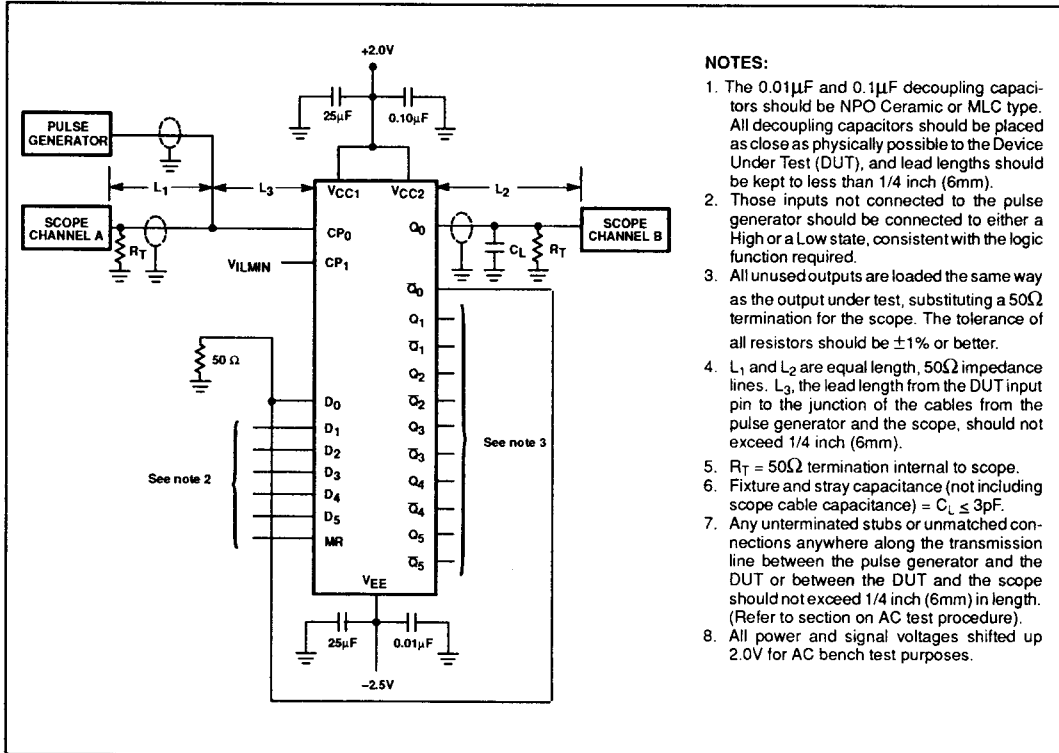
NOTE:

All power and signal voltages shifted up 2.0V for AC bench test purposes.

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SHIFT FREQUENCY TEST CIRCUIT



NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L₁ and L₂ are equal length, 50Ω impedance lines. L₃, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = C_L ≤ 3pF.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.