FEATURES

- **Excellent Speed** ..... **8V/μs Typ**
- **Low Noise** ..... **11nV/√Hz @ 1kHz Max**
- **Unity-Gain Stable**
- **High Gain-Bandwidth** ..... **6.5MHz Typ**
- **Low Input Offset Voltage** ..... **0.8mV Max**
- **Low Offset Voltage Drift** ..... **4μV/° C Max**
- **High Gain** ..... **500V/mV Min**
- **Outstanding CMR** ..... **105 dB Min**
- **Industry Standard Quad Pinouts**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP	PLASTIC	LCC*	OPERATING TEMPERATURE RANGE
800	OP471AY*	–	OP471ATC/883	MIL
800	–	–	OP471ARC/883	MIL
800	OP471EY	–	–	IND
1500	OP471FY	–	–	IND
1800	–	OP471GP	–	XIND
1800	–	OP471GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

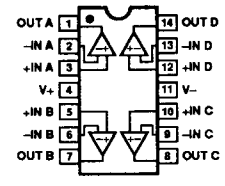
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

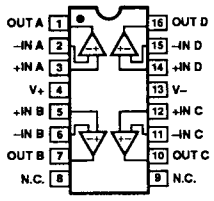
The OP-471 is a monolithic quad op amp featuring low noise, 11nV/√Hz Max @ 1kHz, excellent speed, 8V/μs typical, a gain-bandwidth of 6.5MHz, and unity-gain stability.

The OP-471 has an input offset voltage under 0.8mV and an input offset voltage drift below 4μV/°C, guaranteed over the full military temperature range. Open loop gain of the OP-471 is over 500,000 into a 10kΩ load insuring outstanding gain accuracy and linearity. The input bias current is under 25nA

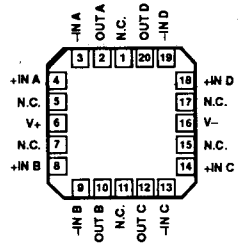
PIN CONNECTIONS



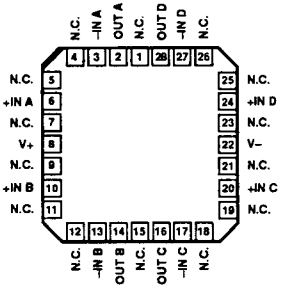
14-PIN HERMETIC DIP (Y-Suffix)
14-PIN PLASTIC DIP (P-Suffix)



16-PIN SOL (S-Suffix)

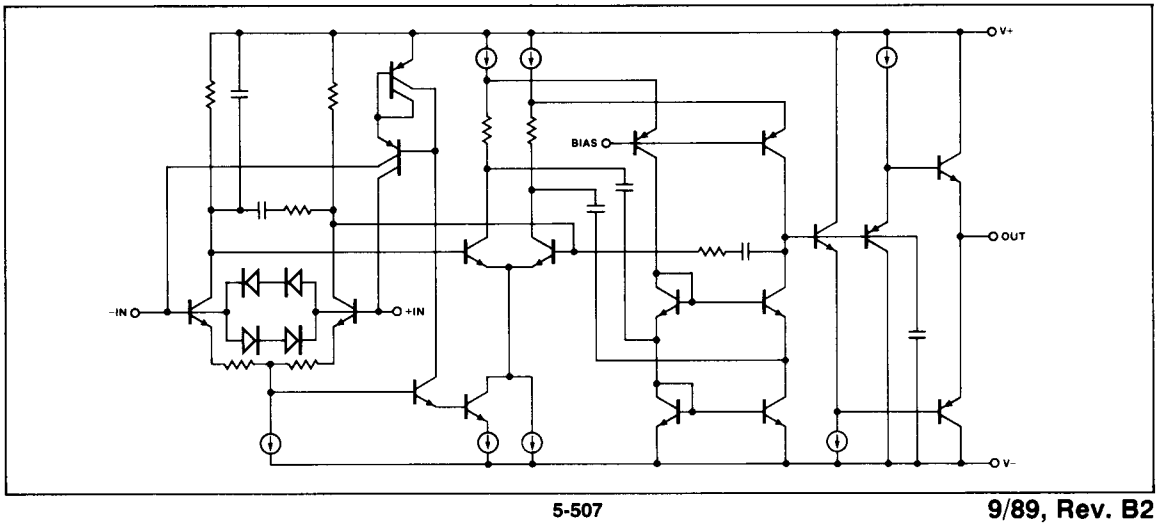


20-LEAD LCC (RC-Suffix)



28-LEAD LCC (TC-Suffix)

SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)



limiting errors due to signal source resistance. The OP-471's CMR of over 105dB and PSRR of under 5.6μV/V significantly reduce errors caused by ground noise and power supply fluctuations.

The OP-471 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers and low-noise active filters.

The OP-471 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, RM4156, MC33074, TL084 and TL074 quad op amps and can be used to upgrade systems using these devices.

For applications requiring even lower voltage noise the OP-470, with a voltage density of $5nV/\sqrt{Hz}$ Max @ 1kHz, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 3) ..... ±1.0V
Differential Input Current (Note 3) ..... ±25mW
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, RC, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP-471A ..... –55°C to +125°C
OP-471E, OP-471F ..... –25°C to +85°C
OP-471G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.
3. The OP-471's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-471A/E MIN	OP-471A/E TYP	OP-471A/E MAX	OP-471F MIN	OP-471F TYP	OP-471F MAX	OP-471G MIN	OP-471G TYP	OP-471G MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.25	0.8	—	0.5	1.5	—	1.0	1.8	mV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	4	10	—	7	20	—	12	30	nA
Input Bias Current	I_B	V_{CM} = 0V	—	7	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	250	500	—	250	500	—	250	500	nV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	9	16	—	9	16	—	9	16	$nV/\sqrt{Hz}$
		f_O = 100Hz	—	7	12	—	7	12	—	7	12	
		f_O = 1kHz (Note 2)	—	6.5	11	—	6.5	11	—	6.5	11	
Input Noise Current Density	i_n	f_O = 10Hz	—	1.7	—	—	1.7	—	—	1.7	—	$pA/\sqrt{Hz}$
		f_O = 100Hz	—	0.7	—	—	0.7	—	—	0.7	—	
		f_O = 1kHz	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 10kΩ	500	700	—	300	500	—	300	500	—	V/mV
		V_O = ±10V, R_L = 2kΩ	350	550	—	175	275	—	175	275	—	
Input Voltage Range	IVR	(Note 3)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	105	120	—	95	115	—	95	115	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	1	5.6	—	5.6	17.8	—	5.6	17.8	μV/V
Slew Rate	SR		6.5	8	—	6.5	8	—	6.5	8	—	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-471A/E MIN	OP-471A/E TYP	OP-471A/E MAX	OP-471F MIN	OP-471F TYP	OP-471F MAX	OP-471G MIN	OP-471G TYP	OP-471G MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.2	11	mA
Gain-Bandwidth Product	GBW	$A_V = +10$	—	6.5	—	—	6.5	—	—	6.5	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	150	—	125	150	—	125	150	—	dB
Input Capacitance	C_{IN}		—	2.6	—	—	2.6	—	—	2.6	—	pF
Input Resistance Differential-Mode	R_{IN}		—	1.1	—	—	1.1	—	—	1.1	—	MΩ
Input Resistance Common-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	GΩ
Settling Time	t_s	$A_V = +1$ to 0.1% to 0.01%	— —	4.5 7.5	— —	— —	4.5 7.5	— —	— —	4.5 7.5	— —	μs

NOTES:
1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$ for OP-471A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-471A MIN	OP-471A TYP	OP-471A MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	1.2	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	4	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	6	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	16	50	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	375 250	500 350	— —	V/mV
Input Voltage Range	IVR	(Note 1)	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	5.6	10	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.3	11	mA

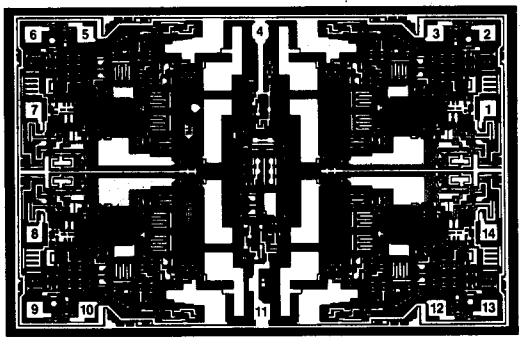
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-471E/F, $-40°C \le T_A \le +85°C$ for OP-471G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-471E			OP-471F			OP-471G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.3	1.1	—	0.6	2.0	—	1.2	2.5	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	4	—	2	7	—	4	—	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	5	20	—	8	40	—	20	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	13	50	—	25	70	—	40	75	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$										
		$R_L = 10k\Omega$	375	600	—	200	400	—	200	400	—	V/mV
		$R_L = 2k\Omega$	250	400	—	125	200	—	125	200	—	
Input Voltage Range	IVR	(Note 1)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	3.2	10	—	18	31.6	—	18	31.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.3	11	—	9.3	11	—	9.3	11	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.163 × 0.106 inch, 17,278 sq. mils
(4.14 × 2.69 mm, 11.14 sq. mm)

1. OUT A
2. −IN A
3. +IN A
4. V+
5. +IN B
6. −IN B
7. OUT B
8. OUT C
9. −IN C
10. +IN C
11. V−
12. +IN D
13. −IN D
14. OUT D

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

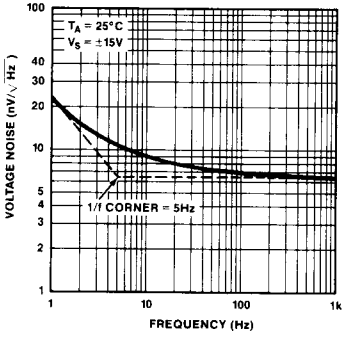
PARAMETER	SYMBOL	CONDITIONS	OP-471GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		1.5	mV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	20	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	50	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 175	 V/mV MIN
Input Voltage Range	IVR	Note 1	±11	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	17.8	μV/V MAX
Slew Rate	SR		6.5	V/μs MIN
Supply Current (All Amplifiers)	I_{SY}	No Load	11	mA MAX

NOTES:
1. Guaranteed by CMR test.

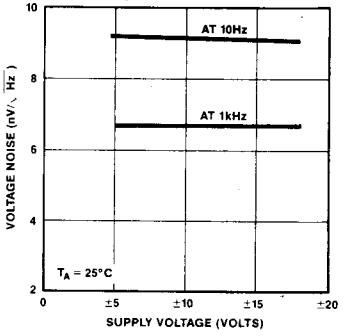
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

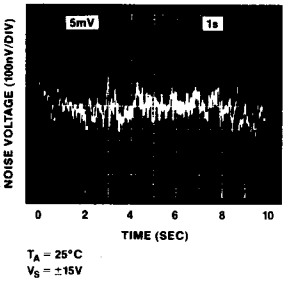
VOLTAGE NOISE DENSITY vs FREQUENCY



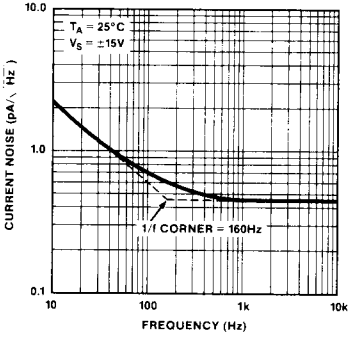
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



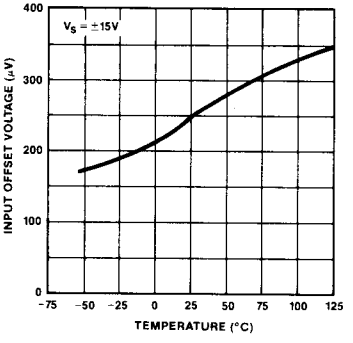
0.1Hz TO 10Hz NOISE



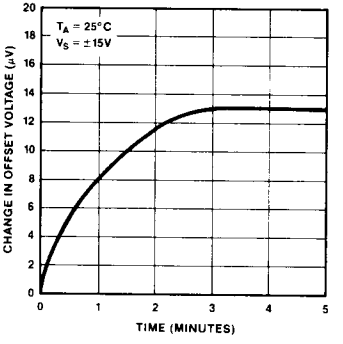
CURRENT NOISE DENSITY vs FREQUENCY



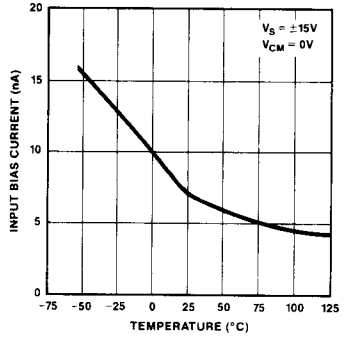
INPUT OFFSET VOLTAGE vs TEMPERATURE



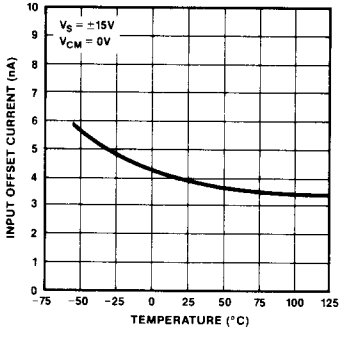
WARM-UP OFFSET VOLTAGE DRIFT



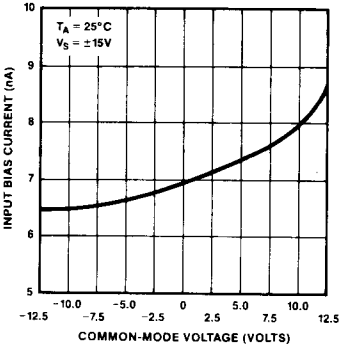
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

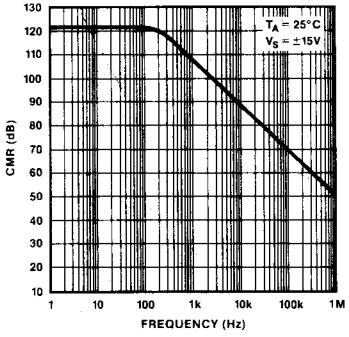


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

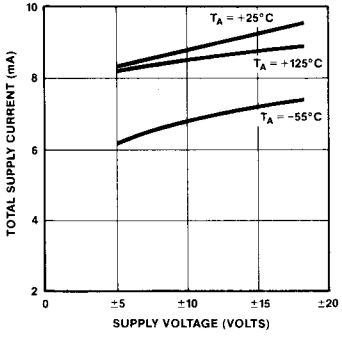


TYPICAL PERFORMANCE CHARACTERISTICS

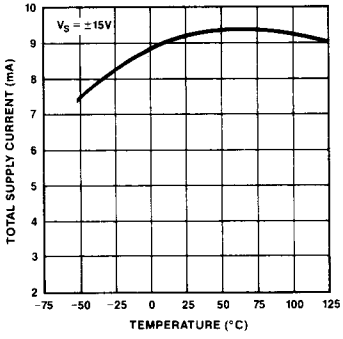
CMR vs FREQUENCY



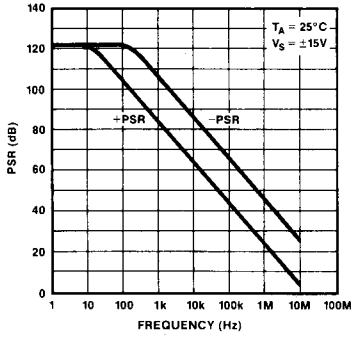
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



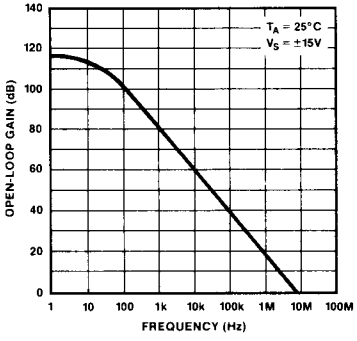
TOTAL SUPPLY CURRENT vs TEMPERATURE



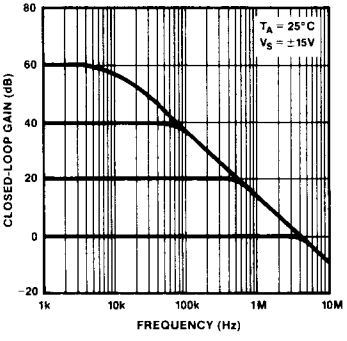
PSR vs FREQUENCY



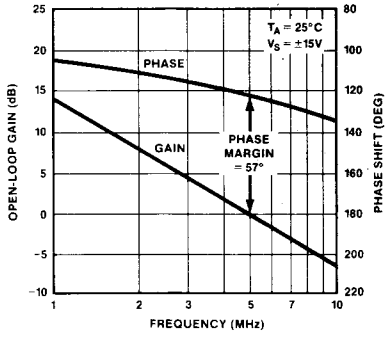
OPEN-LOOP GAIN vs FREQUENCY



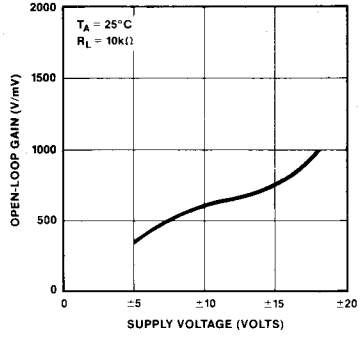
CLOSED-LOOP GAIN vs FREQUENCY



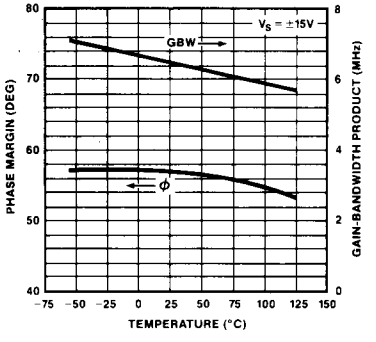
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE

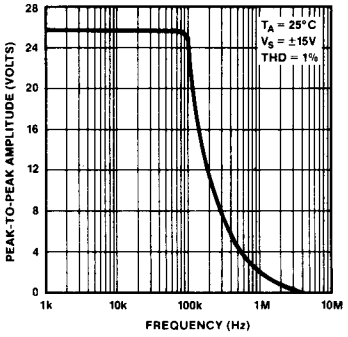


GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

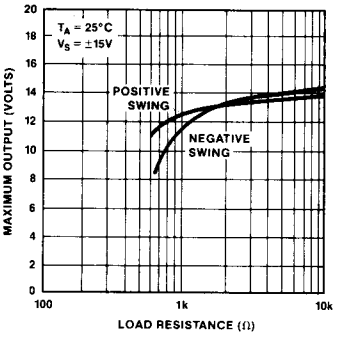


TYPICAL PERFORMANCE CHARACTERISTICS

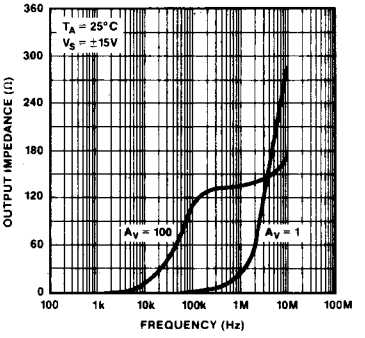
MAXIMUM OUTPUT SWING vs FREQUENCY



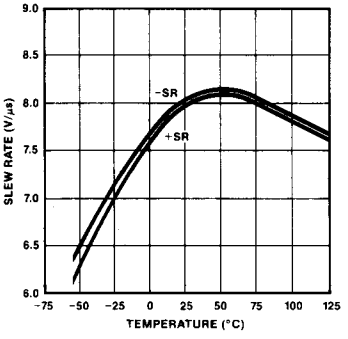
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



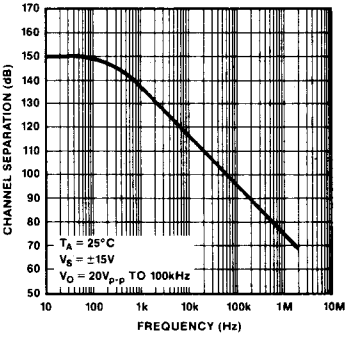
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



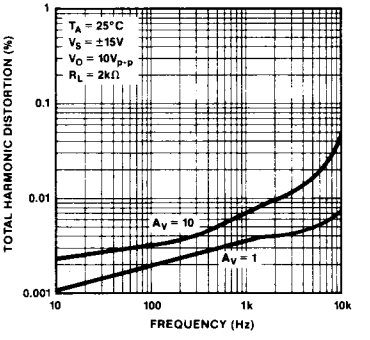
SLEW RATE vs TEMPERATURE



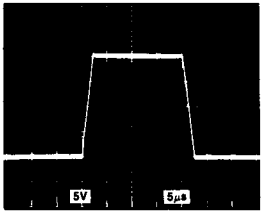
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

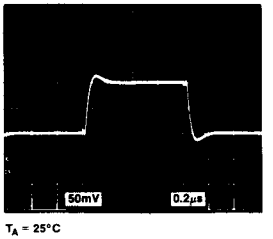


LARGE-SIGNAL TRANSIENT RESPONSE



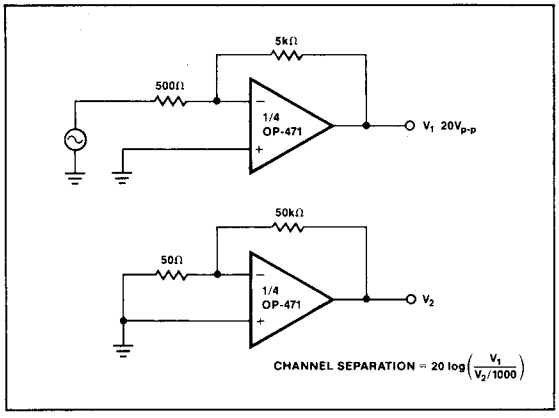
T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE

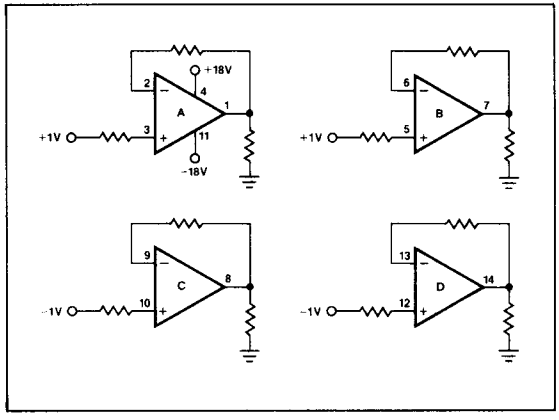


T_A = 25°C
V_S = ±15V
A_V = +1

CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP-471 is a very low-noise quad op amp, exhibiting a typical voltage noise of only 6.5nV/$\sqrt{Hz}$ @ 1kHz. The low noise characteristic of the OP-471 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-471 is gained at the expense of current noise performance which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calulated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1k\Omega$ the total noise is domi-

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

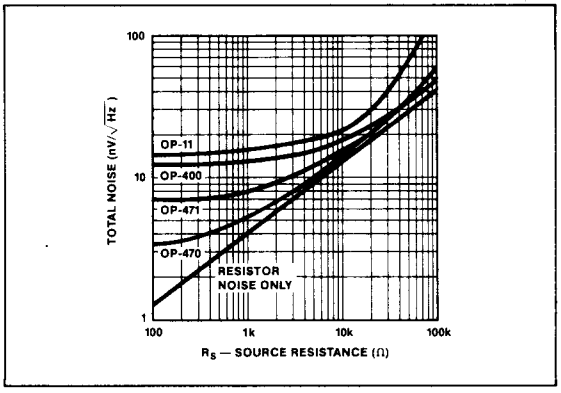
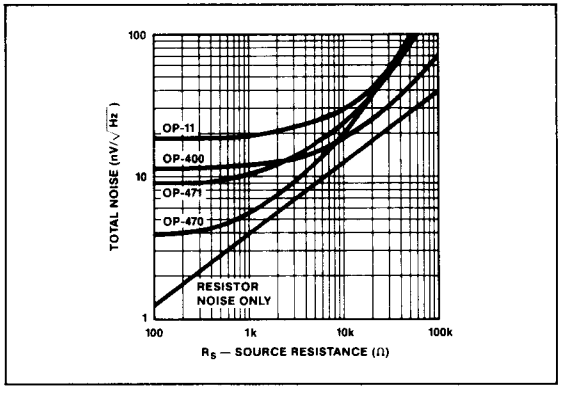


FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz



5

OPERATIONAL AMPLIFIERS/BUFFERS

nated by the voltage noise of the OP-471. As R_S rises above 1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-471. When R_S exceeds 20kΩ, current noise of the OP-471 becomes the major contributor to total noise.

Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-471 dominates the total noise when $R_S > 5k\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-400, with lower current noise than the OP-471, will provide lower total noise.

Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the OP-471 is the major contributor to peak-to-peak noise. Current noise becomes the major contributor as R_S increases. The crossover point between the OP-471 and the OP-400 for peak-to-peak noise is at $R_S = 17k\Omega$.

The OP-470 is a lower noise version of the OP-471, with a typical noise voltage density of $3.2nV/\sqrt{Hz}$ @ 1kHz. The OP-470 offers lower offset voltage and higher gain than the OP-471, but is a slower speed device, with a slew rate of 2V/μs compared to a slew rate of 8V/μs for the OP-471.

For reference, typical source resistances of some signal sources are listed in Table I.

FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)

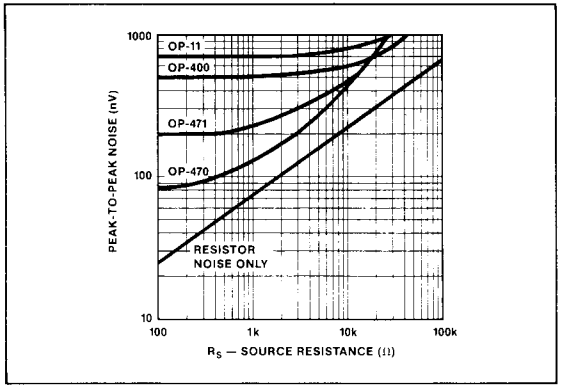


TABLE I

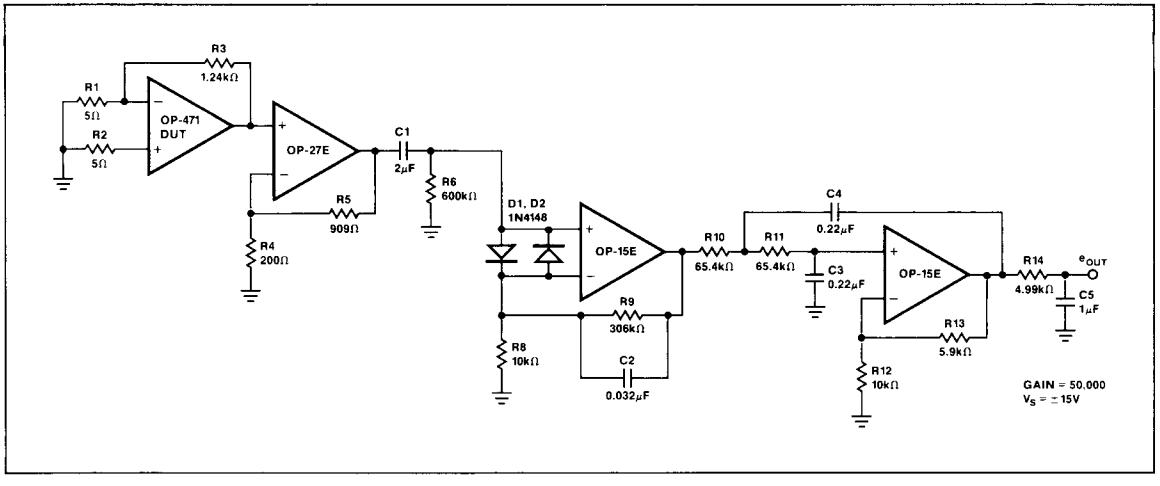
DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-471 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-471 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 500nV peak-to-peak

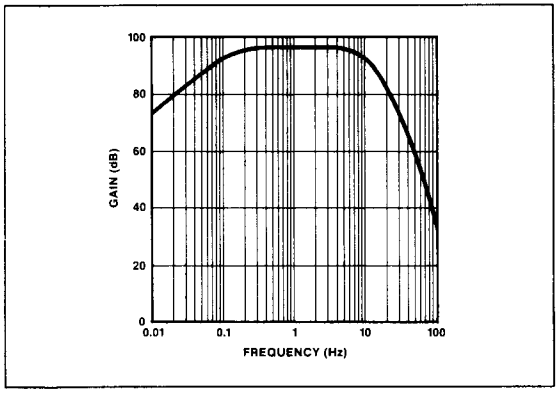
FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)



noise specification of the OP-471 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 13μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced through the amplifier supply pins.

FIGURE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101\ (\sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2})$$

The OP-471 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101\ (\sqrt{4e_n^2}) = 101\ (2e_n)$$

FIGURE 6: Noise Voltage Density Test Circuit

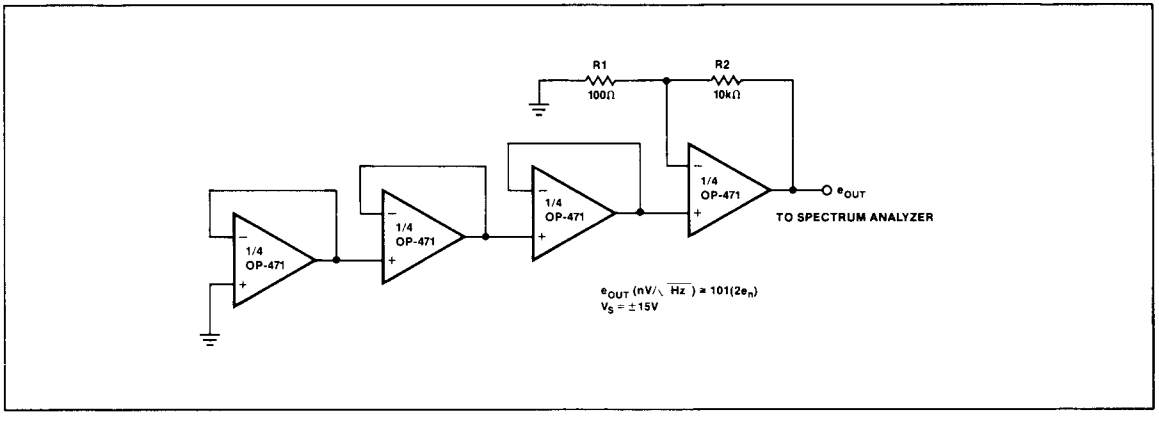
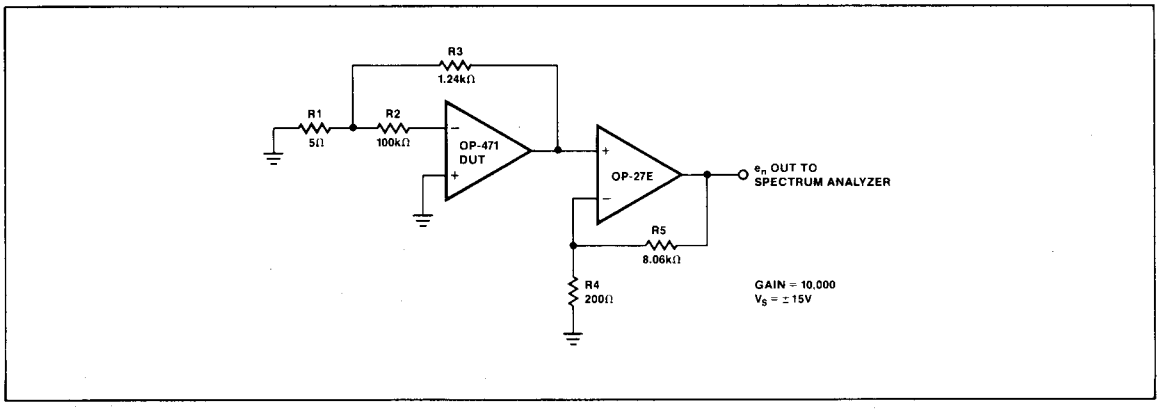


FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000
R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-471 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-471.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for load capacitances of up to 1000pF when used with the OP-471.

In applications where the OP-471's inverting or noninverting inputs are driven by a low source impedance (under 100Ω) or connected to ground, if V+ is applied before V−, or when V− is disconnected, excessive parasitic currents will flow. Most

FIGURE 8: Driving Large Capacitive Loads

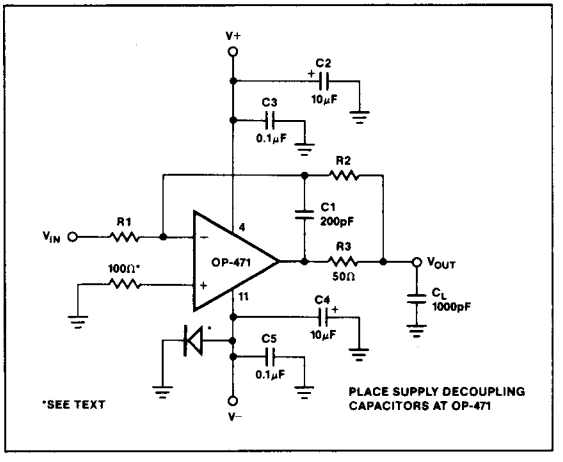
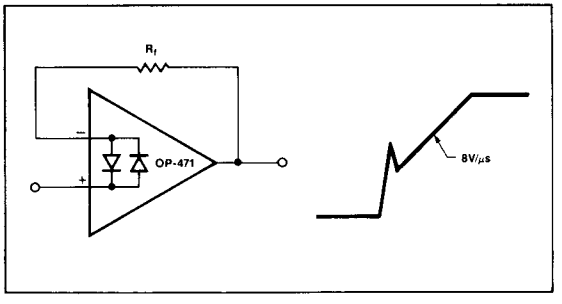


FIGURE 9: Pulsed Operation



applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100Ω in series with all inputs (Figure 8) will limit the parasitic currents to a safe level if V− is disconnected. It should be noted that any source resistance, even 100Ω, adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V− pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (2.6pF) creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f helps eliminate this problem.

APPLICATIONS

LOW NOISE AMPLIFIER

A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 10. Amplifier noise, depicted in Figure 11, is around $5nV/\sqrt{Hz}$ @ 1kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 100. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω. The amplifier is stable with a 10nF capacitive load and can supply up to 30mA of output drive.

HIGH-SPEED DIFFERENTIAL LINE DRIVER

The circuit of Figure 12 is a unique line driver widely used in professional audio applications. With ±18V supplies the line driver can deliver a differential signal of $30V_{p-p}$ into a 1.5kΩ load. The output of the differential line driver looks exactly like a transformer. Either output can be shorted to ground without changing the circuit gain of 5, so the amplifier can easily be set for inverting, noninverting, or differential operation. The line driver can drive unbalanced loads, like a true transformer.

HIGH OUTPUT AMPLIFIER

The amplifier shown in Figure 13 is capable of driving $20V_{p-p}$ into a floating 400Ω load. Design of the amplifier is based on a bridge configuration. A1 amplifies the input signal and drives the load with the help of A2. Amplifier A3 is a unity-gain inverter which drives the load with help from A4. Gain of the high output amplifier with the component values shown is 10, but can easily be changed by varying R1 or R2.

FIGURE 10: Low Noise Amplifier

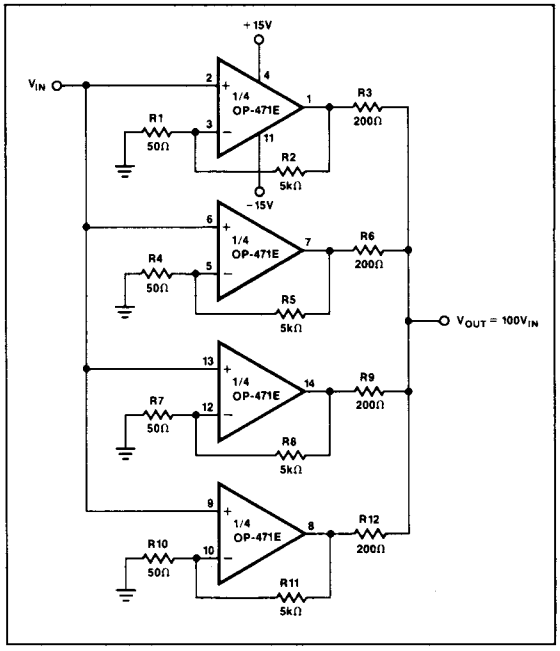


FIGURE 11: Noise Density of Low Noise Amplifier, G = 100

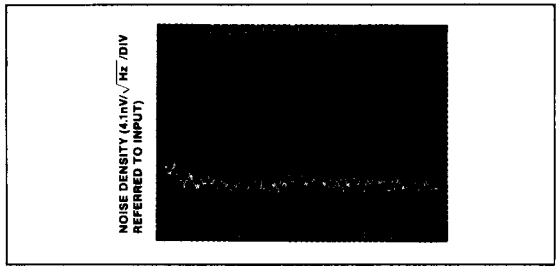


FIGURE 12: High-Speed Differential Line Driver

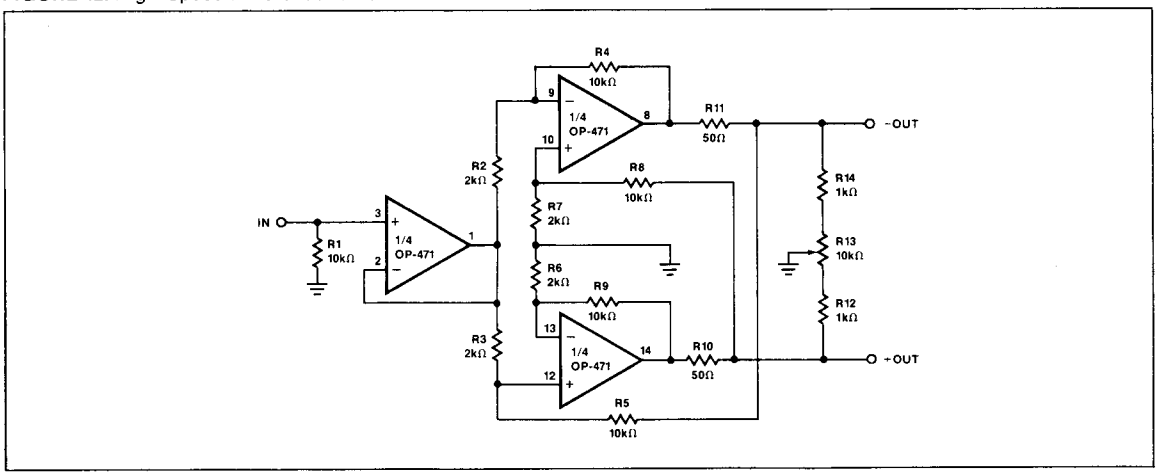
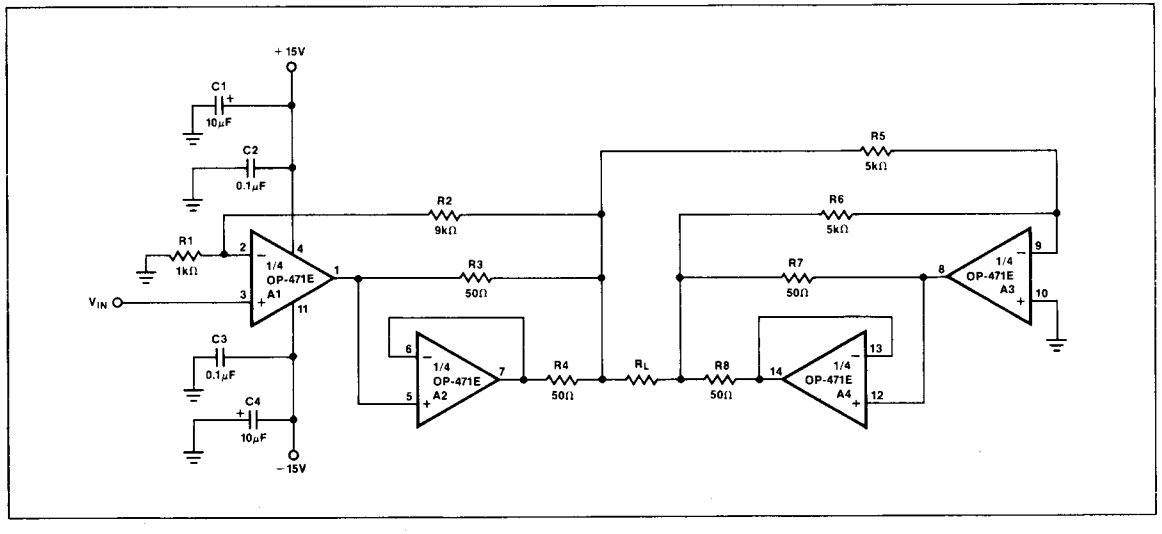


FIGURE 13: High Output Amplifier



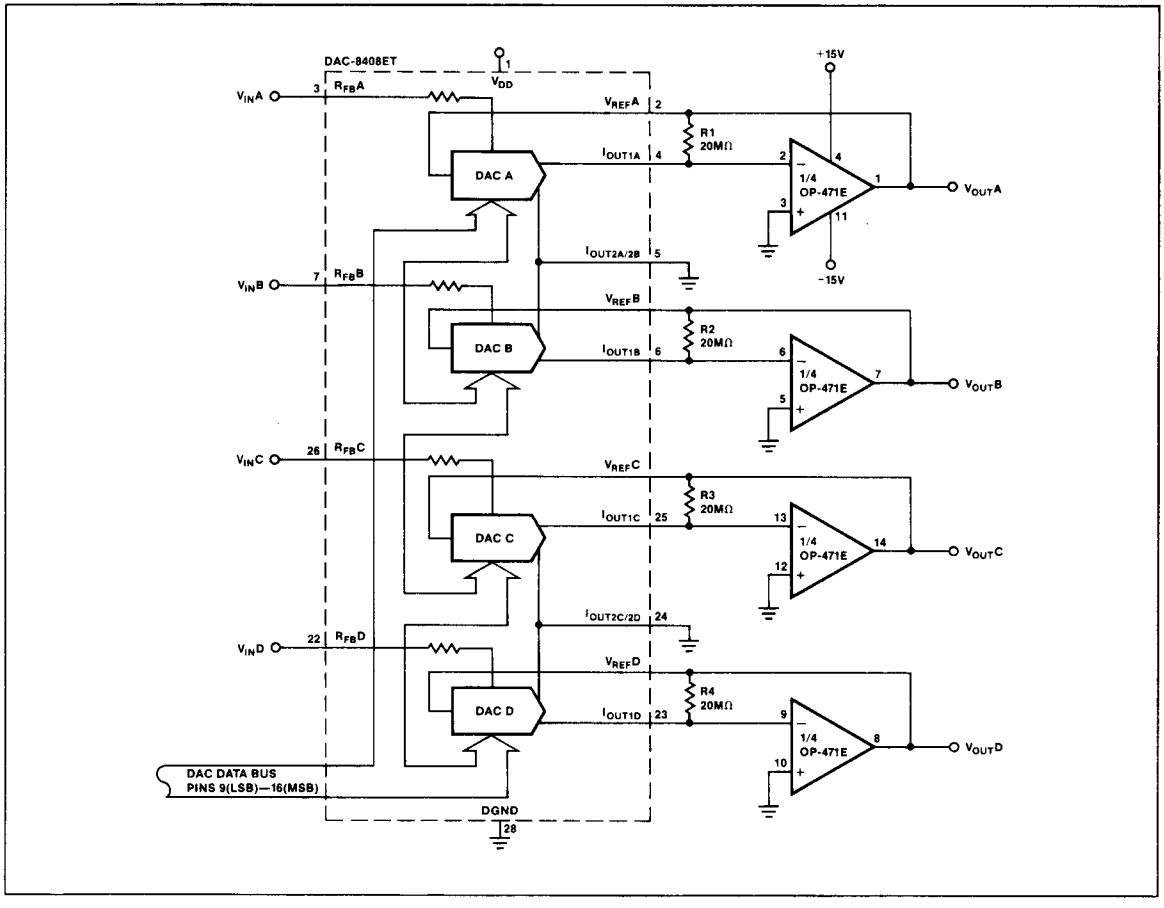
QUAD PROGRAMMABLE GAIN AMPLIFIER

The combination of the quad OP-471 and the DAC-8408, a quad 8-bit CMOS DAC, creates a space-saving quad programmable gain amplifier. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the fixed DAC feedback resistor and the impedance the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{256}{n},$$

where n equals the decimal equivalent of the 8-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will be open causing the op amp output to saturate. The 20MΩ resistors placed in parallel with the DAC feedback loop eliminates this problem with a very small reduction in gain accuracy.

FIGURE 14: Quad Programmable Gain Amplifier



LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 15 utilizes monolithic matched operational amplifiers and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $V_O/(K1 + 1) = V_2/(K1 + 1)$ yielding an overall transfer function of $V_O/V_{IN} = K1 + 1$. The DC gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note, that like a conventional single op amp amplifier, the DC gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

Figure 16 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of −0.1° occurs at $0.002\ \omega/\beta\omega_T$ for the single op amp amplifier, but at $0.11\ \omega/\beta\omega_T$ for the low phase error amplifier.

For more detailed information on the low phase error amplifier, see Application Note AN-107.

FIGURE 15: Low Phase Error Amplifier

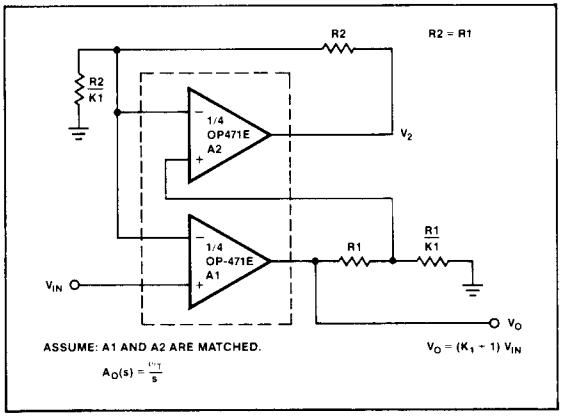


FIGURE 16: Phase Error Comparison