Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 2048 x 9-BIT and 4096 x 9-BIT

IDT7203S/L
IDT7204S/L

FEATURES:

- First-In/First-Out dual-port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- Ultra high-speed: 15ns access time
- Low power consumption
  - — Active: 880mW (max.)
  - — Power-down: 44mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with IDT720X family
- Status Flags: Empty, Half-Full, Full
- Auto retransmit capability
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88669, 5962-89567, and 5962-89568 are listed on this function.

DESCRIPTION:

The IDT7203/7204 are dual-port memories that load and empty data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

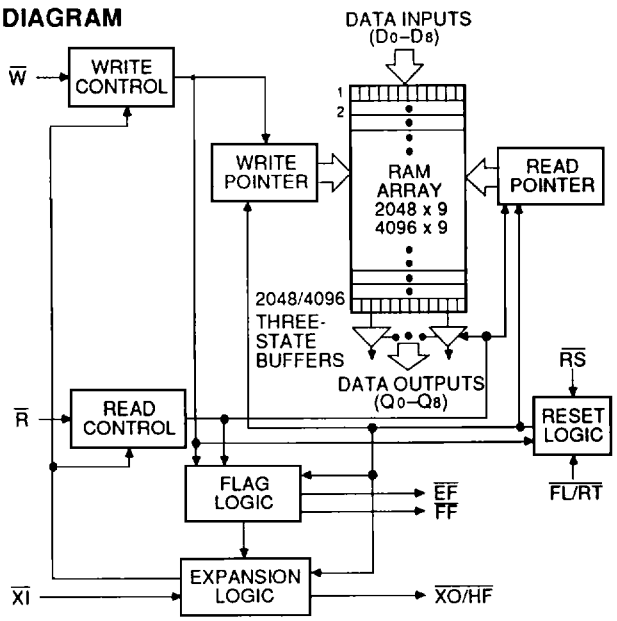
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 25ns (40MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low. A Half-Full Flag is available in the single device and width expansion modes.

The IDT7203/7204 is fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



2661 drw 01

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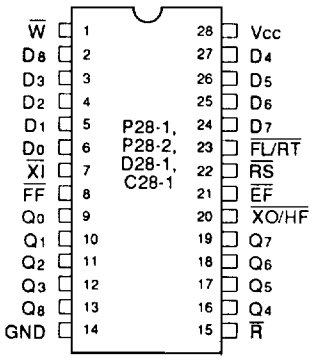
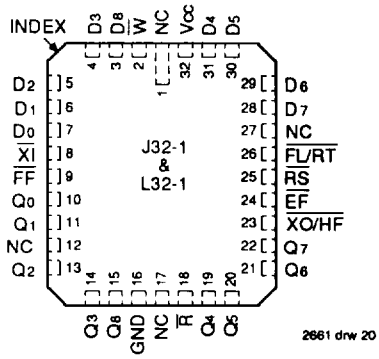
PIN CONFIGURATIONS



DIP
TOP VIEW

Consult Factory for CERPACK Pinout.



PLCC/LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to + 7.0	-0.5 to + 7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	° C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	° C
TSTG	Storage Temperature	-55 to + 125	-65 to + 155	° C
IOUT	DC Output Current	50	50	mA

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NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL (2,)	Input Low Voltage Commercial and Military	—	—	0.8	V

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NOTES:

1. VIH = 2.6V for $\overline{XI}$ input (commercial).
   VIH = 2.8V for $\overline{XI}$ input (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT7203, IDT7204 Commercial t_A = 15, 20ns			IDT7203, IDT7204 Military t_A = 20ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI} (1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{LO} (2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1} (3,4)	Active Power Supply Current	—	—	160	—	—	200	mA
I_{CC2} (3)	Average Standby Current, ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	—	14	—	—	19	mA
I_{CC3} (L) (3)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	8	—	—	12	mA

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20 MHz

2661 tbl 03

DC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT7203, IDT7204 Commercial t_A = 25, 35, 50, 65 80, 120ns			IDT7203, IDT7204 Military t_A = 30, 40, 50, 65 80, 120ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI} (1)	Input Leakage Current (Any Input)	-1	—	-1	-10	—	10	µA
I_{LO} (2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = 2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1} (3, 4)	Active Power Supply Current	—	75	120	—	100	150	mA
I_{CC2} (3)	Average Standby Current, ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	8	12	—	12	25	mA
I_{CC3} (L) (3)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	2	—	—	4	mA
I_{CC3} (S) (3)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	8	—	—	12	mA

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open.
4. Tested at f = 20MHz.

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AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Commercial 7203/04L15		Com'l. & Mil. 7203/04L20		Commercial 7203/04L25		Military 7203/04L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_s	Shift Frequency	—	40	—	33.3	—	28.5	—	25	MHz
tRC	Read Cycle Time	25	—	30	—	35	—	40	—	ns
tA	Access Time	—	15	—	20		25	—	30	ns
tRR	Read Recovery Time	10	—	10	—	10	—	10	—	ns
tRPW	Read Pulse Width[2]	15	—	20	—	25	—	30	—	ns
tRLZ	Read Low to Data Bus Low Z[3]	5	—	5	—	5	—	5	—	ns
tWLZ	Write High to Data Bus Low Z[3, 4]	5	—	5	—	5	—	5	—	ns
tDV	Data Valid from Read High	5	—	5	—	5	—	5	—	ns
tRHZ	Read High to Data Bus High Z[3]	—	15	—	15	—	18	—	20	ns
tWC	Write Cycle Time	25	—	30	—	35	—	40	—	ns
tWPW	Write Pulse Width[2]	15	—	20	—	25	—	30	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	11	—	12	—	15	—	18	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tRSC	Reset Cycle Time	25	—	30	—	35	—	40	—	ns
tRS	Reset Pulse Width[2]	15	—	20	—	25	—	30	—	ns
tRSS	Reset Set-up Time	15	—	20	—	25	—	30	—	ns
tRSR	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
tRTC	Retransmit Cycle Time	25	—	30	—	35	—	40	—	ns
tRT	Retransmit Pulse Width[2]	15	—	20	—	25	—	30	—	ns
tRTS	Retransmit Set-up Time	15	—	20	—	25	—	30	—	ns
tRTR	Retransmit Recovery Time	10	—	10	—	10	—	10	—	ns
tEFL	Reset to Empty Flag Low	—	25	—	30	—	35	—	40	ns
tHFH,tFFH	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	25	—	30	—	35	—	40	ns
tREF	Read Low to Empty Flag Low	—	15	—	20	—	25	—	30	ns
tRFF	Read High to Full Flag High	—	18	—	20	—	25	—	30	ns
tRPE	Read Pulse Width after $\overline{EF}$ High	15	—	20	—	25	—	30	—	ns
tWEF	Write High to Empty Flag High	—	18	—	20	—	25	—	30	ns
tWFF	Write Low to Full Flag Low	—	15	—	20	—	25	—	30	ns
tWHF	Write Low to Half-Full Flag Low	—	25	—	30	—	35	—	40	ns
tRHF	Read High to Half-Full Flag High	—	25	—	30	—	35	—	40	ns
tWPF	Write Pulse Width after $\overline{FF}$ High	15	—	20	—	25	—	30	—	ns
tXOL	Read/Write Low to $\overline{XO}$ Low	—	15	—	20	—	25	—	30	ns
tXOH	Read/Write High to $\overline{XO}$ High	—	15	—	20	—	25	—	30	ns
tXI	$\overline{XI}$ Pulse Width[2]	15	—	20	—	25	—	30	—	ns
tXIR	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	ns
tXIS	$\overline{XI}$ Set-up Time	10	—	10	—	10	—	10	—	ns

NOTES:

2661 tbl 05

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC ELECTRICAL CHARACTERISTICS[1] (Continued)

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

		Com'l.		Military		Commercial and Military								
		7203S/L35 7204S/L35		7203S/L40 7204S/L40		7203S/L50 7204S/L50		7203S/L65 7204S/L65		7203S/L80 7204S/L80		7203S/L120 7204S/L120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_s	Shift Frequency	—	22.2	—	20	—	15	—	12.5	—	10	—	7	MHz
tRC	Read Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
tA	Access Time	—	35	—	40	—	50	—	65	—	80	—	120	ns
tRR	Read Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
tRPW	Read Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
tRLZ	Read Low to Data Bus Low Z[3]	5	—	5	—	10	—	10	—	10	—	10	—	ns
tWLZ	Write High to Data Bus Low Z[3,4]	10	—	10	—	5	—	5	—	5	—	5	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
tRHZ	Read High to Data Bus High Z[3]	—	20	—	25	—	30	—	30	—	30	—	35	ns
tWC	Write Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
tWPW	Write Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
tWR	Write Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
tDS	Data Set-up Time	18	—	20	—	30	—	30	—	40	—	40	—	ns
tDH	Data Hold Time	0	—	0	—	5	—	10	—	10	—	10	—	ns
tRSC	Reset Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
tRS	Reset Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
tRSS	Reset Set-up Time	35	—	40	—	50	—	65	—	80	—	120	—	ns
tRSR	Reset Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
tRTC	Retransmit Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
tRT	Retransmit Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
tRTS	Retransmit Set-up Time [3]	35	—	40	—	50	—	65	—	80	—	120	—	ns
tRTR	Retransmit Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
tEFL	Reset to Empty Flag Low	—	45	—	50	—	65	—	80	—	100	—	140	ns
tHFH, tFFH	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	50	—	65	—	80	—	100	—	140	ns
tREF	Read Low to Empty Flag Low	—	30	—	35	—	45	—	60	—	60	—	60	ns
tRFF	Read High to Full Flag High	—	30	—	35	—	45	—	60	—	60	—	60	ns
tRPE	Read Pulse Width after $\overline{EF}$ High	35	—	40	—	50	—	65	—	80	—	120	—	ns
tWEF	Write High to Empty Flag High	—	30	—	35	—	45	—	60	—	60	—	60	ns
tWFF	Write Low to Full Flag Low	—	30	—	35	—	45	—	60	—	60	—	60	ns
tWHF	Write Low to Half-Full Flag Low	—	45	—	50	—	65	—	80	—	100	—	140	ns
tRHF	Read High to Half-Full Flag High	—	45	—	50	—	65	—	80	—	100	—	140	ns
tWPF	Write Pulse Width after $\overline{FF}$ High	35	—	40	—	50	—	65	—	80	—	120	—	ns
tXOL	Read/Write Low to $\overline{XO}$ Low	—	35	—	40	—	50	—	65	—	80	—	120	ns
tXOH	Read/Write High to $\overline{XO}$ High	—	35	—	40	—	50	—	65	—	80	—	120	ns
tXI	$\overline{XI}$ Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
tXIR	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	10	—	ns
tXIS	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	15	—	15	—	15	—	ns

2661 tbl 05

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

6

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

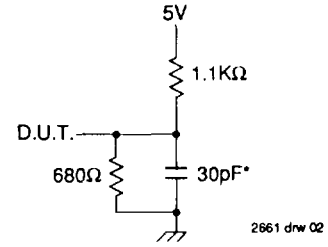
2661 tbl 08

CAPACITANCE[1] (T_A = + 25° C, f = 1.0MHZ)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}[2]	Output Capacitance	V_{OUT} = 0V	12	pF

2661 tbl 09

NOTES:
1. This parameter is sampled and not 100% tested.
2. With output deselected.



or equivalent circuit

Figure 1. Output Load

* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

Inputs:

DATA IN (D_0–D_8) — Data inputs for 9-bit wide data.

Controls:

RESET ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after master Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$) — A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$) — A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$) — This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7203/7204 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the status of the flags depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$) — This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the Single Device Mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

Outputs:

FULL FLAG ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go low, inhibiting further write operations, when the write pointer is equal to the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 2048 writes for the IDT7203 and 4096 writes for the IDT7204.

EMPTY FLAG ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

Expansion Out/Half Full Flag ($\overline{XO}/\overline{HF}$)

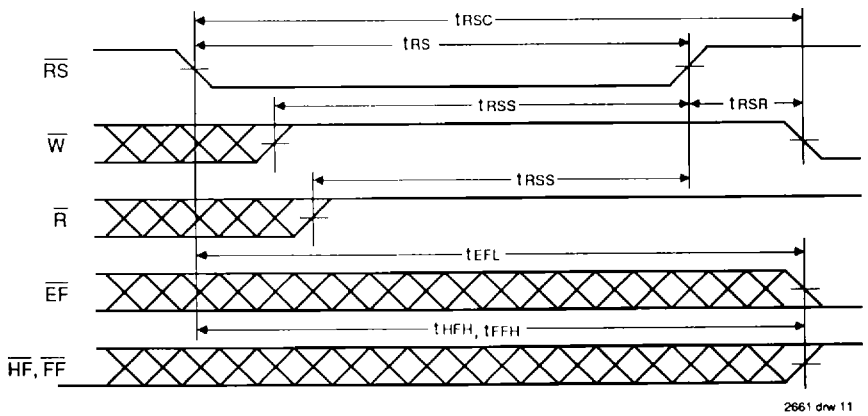
This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory. There will be an $\overline{XO}$ pulse when the Write pointer reaches the last location of memory, and an additional $\overline{XO}$ pulse when the Read pointer reaches the last location of memory.

Data Outputs (Q_0-Q_8)

Q_0-Q_8 are data outputs for 9-bit wide data. These outputs are in a high impedance condition whenever Read ($\overline{R}$) is in a high state.



NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at tRSO.
2. $\overline{W}$ and $\overline{R}$ = VIH around the rising edge of $\overline{RS}$.

Figure 2. Reset

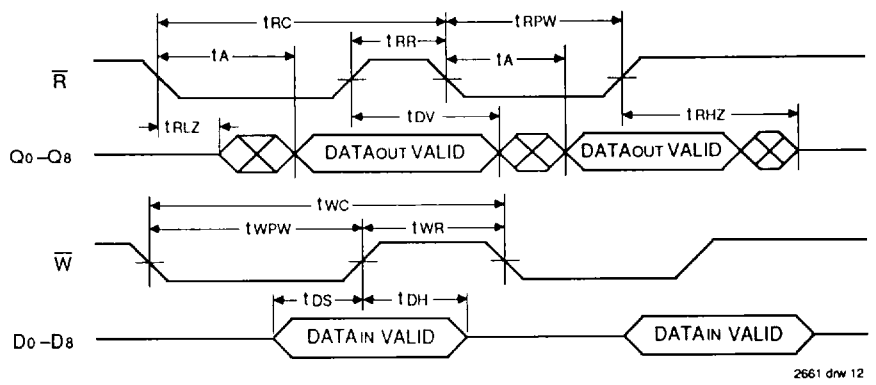


Figure 3. Asynchronous Write and Read Operation

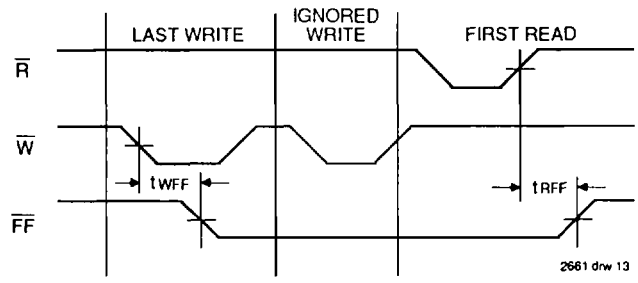


Figure 4. Full Flag From Last Write to First Read

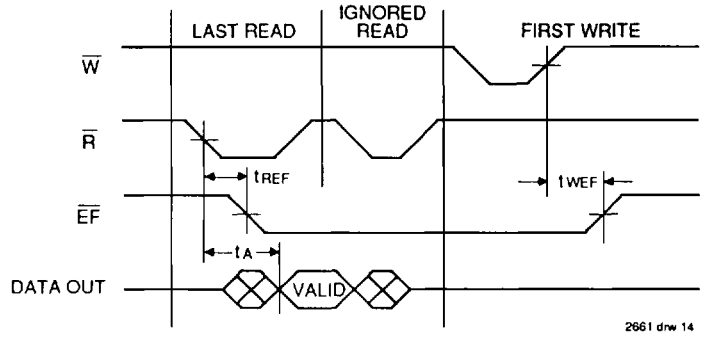
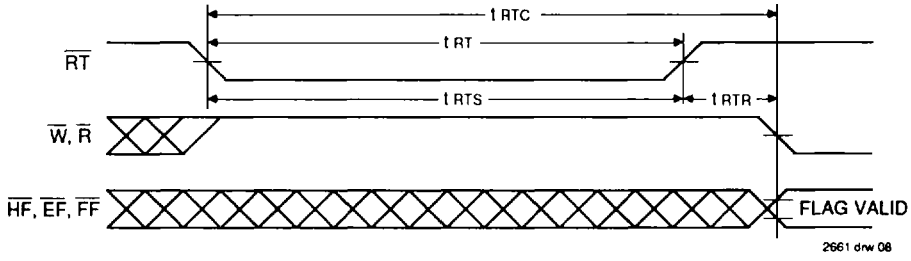


Figure 5. Empty Flag From Last Read to First Write



NOTE:
1. EF, FF and HF may change status during Retransmit, but flags will be valid at tRTC.

Figure 6. Retransmit

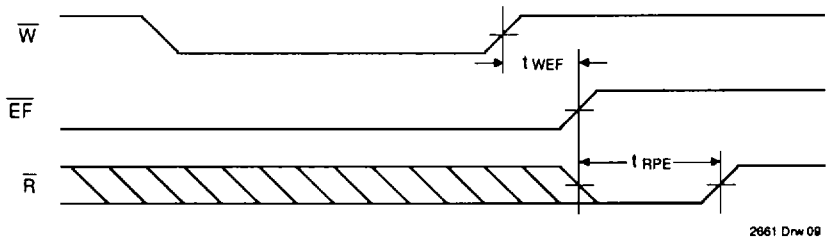


Figure 7. Empty Flag Timing

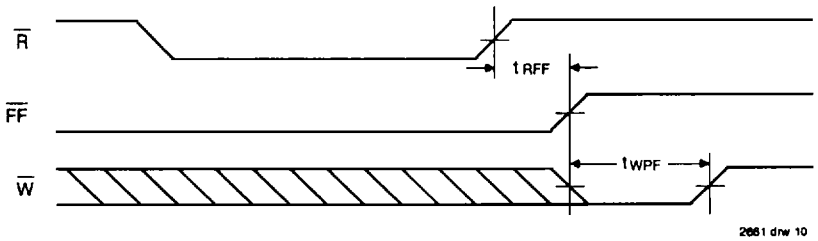


Figure 8. Full Flag Timing

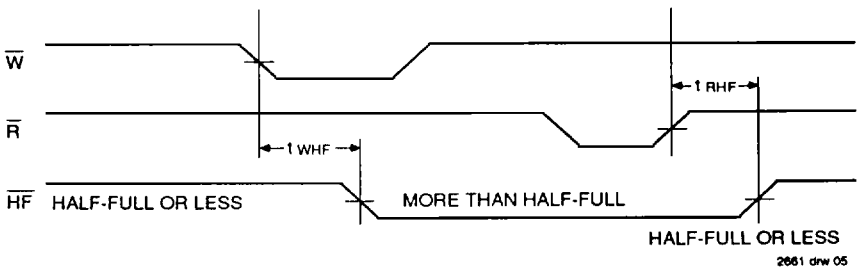


Figure 9. Half-Full Flag Timing

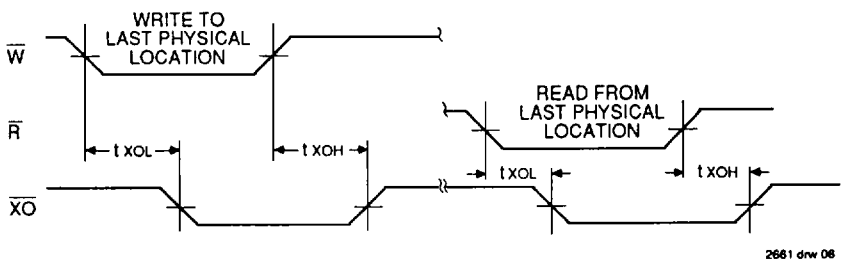


Figure 10. Expansion Out

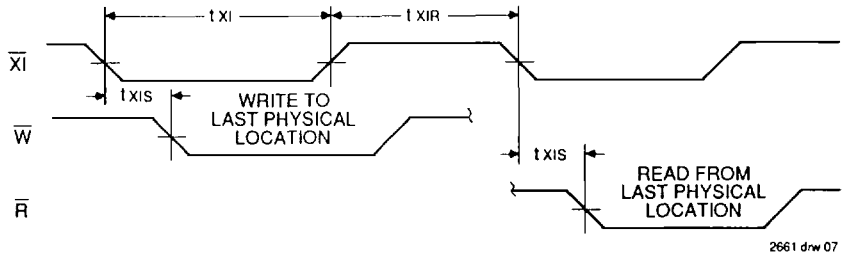


Figure 11. Expansion In

OPERATING MODES:

Single Device Mode

A single IDT7203/7204 may be used when the application requirements are for 2048/4096 words or less. The IDT7203/7204 are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7203/7204s. Any word width can be attained by adding additional IDT7203/7204s.

Depth Expansion (Daisy Chain Mode)

The IDT7203/7204 can easily be adapted to applications when the requirements are for greater than 2048/4096 words. Figure 14 demonstrates Depth Expansion using three IDT7203/7204s. Any depth can be attained by adding additional IDT7203/7204s. The IDT7203/7204 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

Bidirectional Mode

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7203/7204s as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through Modes

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge will deassert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

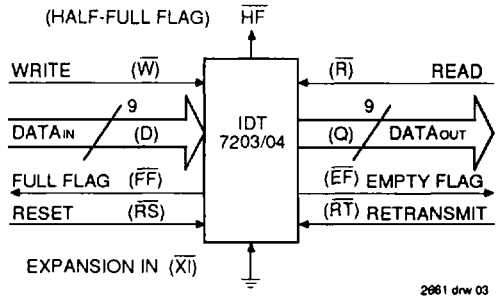
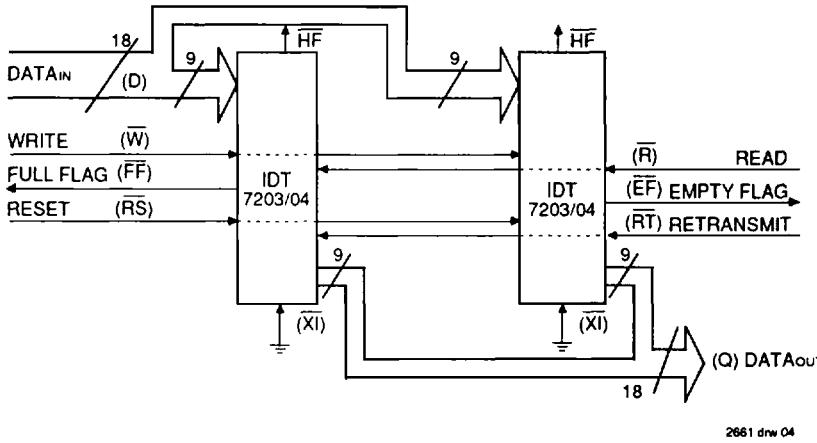


Figure 12. Block Diagram of 2048 x 9/4096 x 9 FIFO Used In Single Device Mode.



NOTE:
1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 13. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used In Width Expansion Mode

6

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will Increment if flag is high.

2661 tbl 10

TABLE II – RESET AND FIRST LOAD TRUTH TABLE

DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

2661 tbl 11

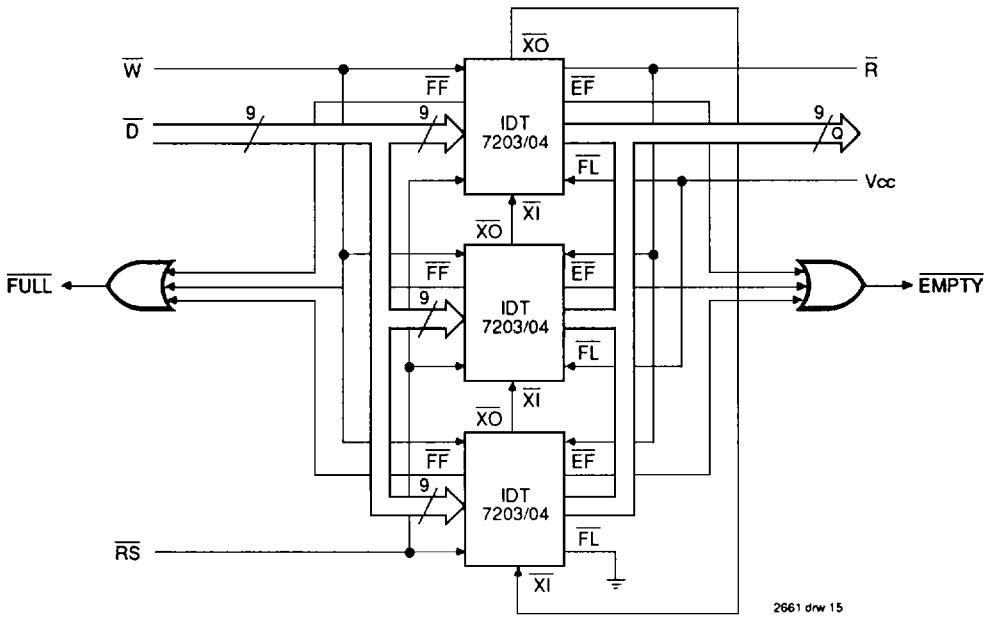
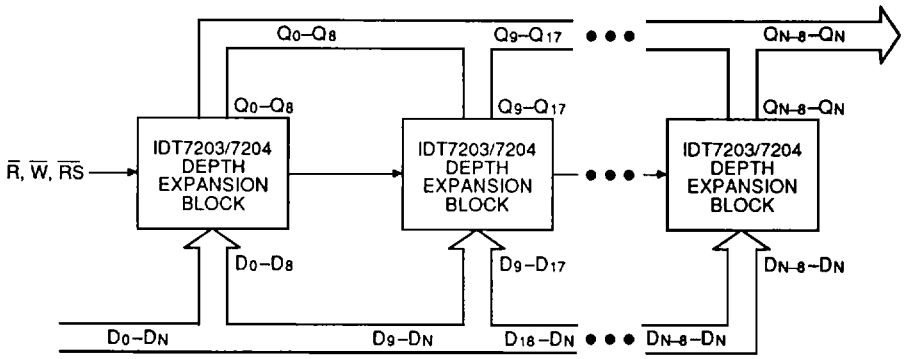


Figure 14. Block Diagram of 6,144 x 9/12,288 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

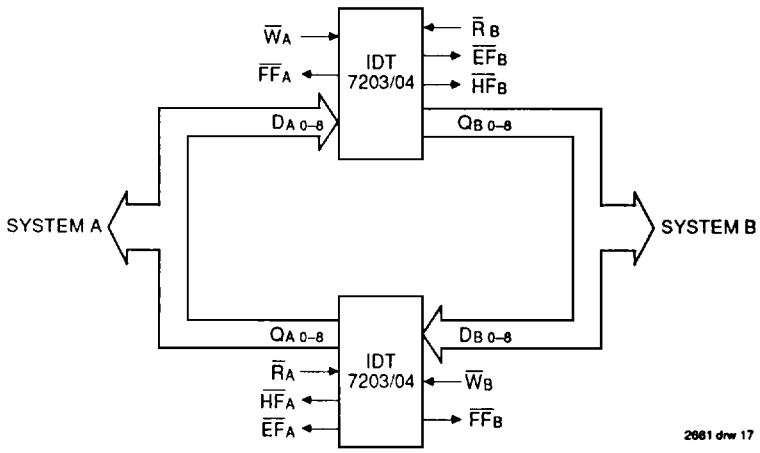


Figure 16. Bidirectional FIFO Mode

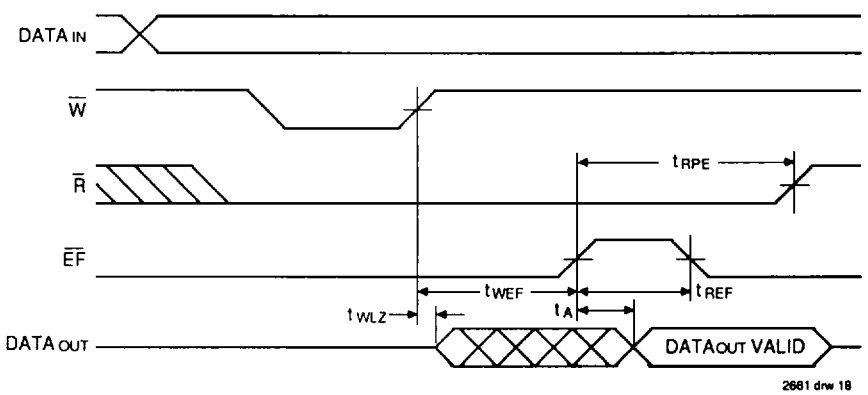


Figure 17. Read Data Flow-Through Mode

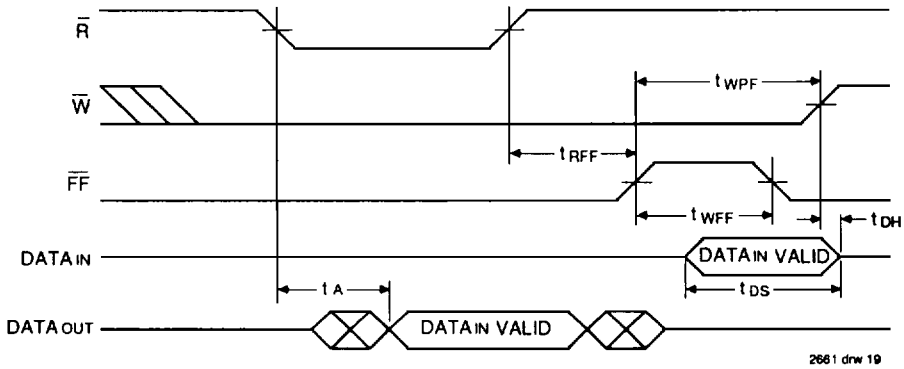


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION