FEATURES

- BCD, bi-quinary, binary counting modes
- Asynchronous clear
- Fully programmable
- May be used as 4-Bit latches

DESCRIPTION

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (LS196) or a divide-by-two and a divide-by-eight counter (LS197). THese four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

TYPICAL COUNT CONFIGURATIONS   LS196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table shown at the right.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary function table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

PIN-OUT DIAGRAM

LS196   **LS197**

Die Size .062 x .074 (both types)
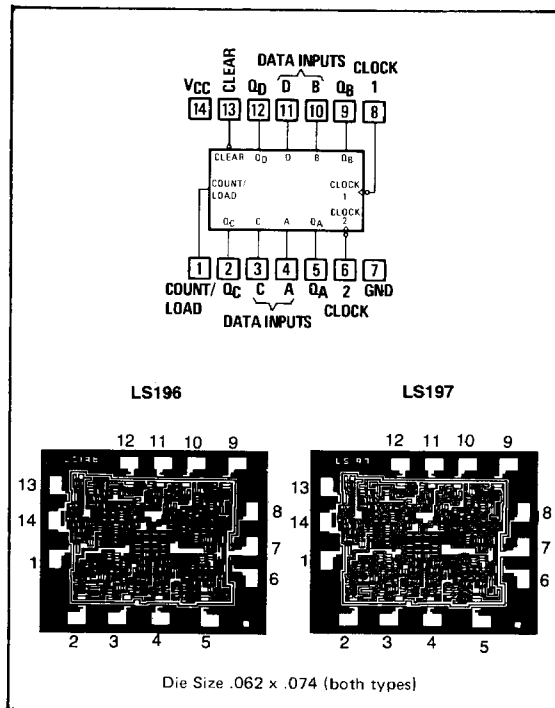
LS196 FUNCTION TABLES

DECADE (BCD)
(See Note A)

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUTS			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = high level, L = low level

NOTES: A. Output Q_A connected to clock-2 input.
    B. Output Q_D connected to clock-1 input.

LS197

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, Q_D output as shown in the function table at right.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit-ripple-through counter.

LS197 FUNCTION TABLE
(See Note A)

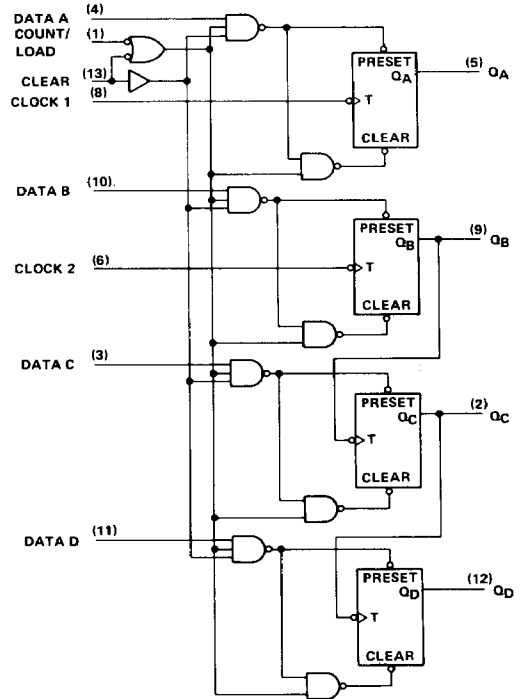| COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = high level, L = low level
NOTE A: Output Q_A connected to clock-2 input.

LOGIC DIAGRAM LS196
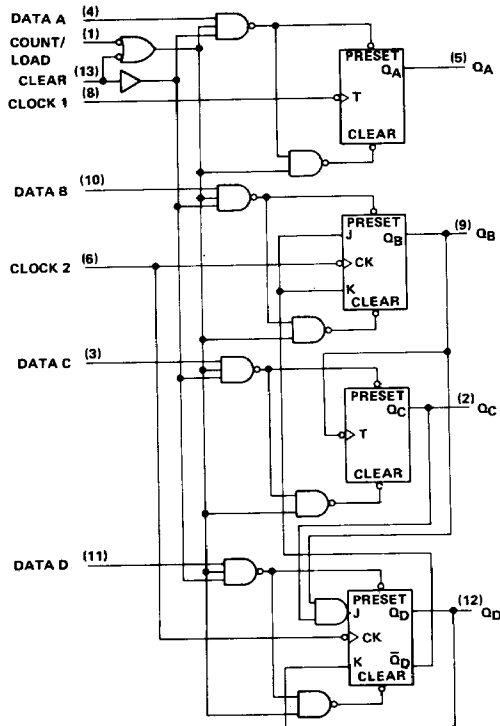
LOGIC DIAGRAM LS197

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.75	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency	Clock-1 input	0			0			MHz
	Clock-2 input	0			0			
Pulse width, t_w	Clock-1 input	20			20			ns
	Clock-2 input	30			30			
	Clear	15			15			
	Load	20			20			
Input hold time, t_{hold}	High-level data	$t_{w (load)}$						ns
	Low-level data	$t_{w (load)}$						
Input setup time, t_{setup}	High-level data	10			10			ns
	Low-level data	15			15			
Count enable time, t_{enable} (see Note 1)		20			20			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE1:
Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA¶		0.25	0.40		0.25	0.40	V
			I_{OL}=8mA					0.35	0.50	
I_I	Data, count/load	V_{CC}=MAX, V_I=7.0V				0.1			0.1	mA
	Clear, clock 1					0.2			0.2	
	Clock 2 of LS196					0.4			0.4	
	Clock 2 of LS197					0.2			0.2	
I_{IH}	Data, count/load	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Clear, clock 1					40			40	
	Clock 2 of LS196					80			80	
	Clock 2 of LS197					40			40	
I_{IL}	Data, count/load	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
	Clear					−0.8			−0.8	
	Clock 1					−2.4			−2.4	
	Clock 2 of LS196					−2.8			−2.8	
	Clock 2 of LS197					−1.3			−1.3	
I_{OS}†		V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††		V_{CC}=MAX			12	20		12	20	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
¶ Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.
†† I_{CC} is measured with all inputs grounded and all outputs open.

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Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		From (input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A on page 2-174)													
f_{max}	LS196	Clock 1	Q_A				45	70					MHz
f_{max}	LS197	Clock 1	Q_A				45	60					MHz
t_{PLH}	LS196	Clock 1	Q_A		10	15		8	12		10	15	ns
t_{PHL}					14	19		12	16		14	19	
t_{PLH}	LS197	Clock 1	Q_A		10	15		8	12		10	15	ns
t_{PHL}					14	19		12	16		14	19	
t_{PLH}	LS196	Clock 2	Q_B		13	18		11	15		13	18	ns
t_{PHL}					16	22		14	19		16	22	
t_{PLH}	LS197	Clock 2	Q_B		12	18		10	15		12	18	ns
t_{PHL}					15	21		13	18		15	21	
t_{PLH}	LS196	Clock 2	Q_C		24	37		22	34		24	37	ns
t_{PHL}					31	43		29	40		31	43	
t_{PLH}	LS197	Clock 2	Q_C		24	37		22	34		24	37	ns
t_{PHL}					28	37		26	34		28	37	
t_{PLH}	LS196	Clock 2	Q_D		13	21		11	18		13	21	ns
t_{PHL}					18	23		16	20		18	23	
t_{PLH}	LS197	Clock 2	Q_D		36	55		34	50		36	55	ns
t_{PHL}					42	60		40	55		42	60	
t_{PLH}	LS196	A, B, C, D	Q_A,Q_B,Q_C,Q_D		14	22		12	18		14	22	ns
t_{PHL}					23	38		21	34		23	38	
t_{PLH}	LS197	A, B, C, D	Q_A,Q_B,Q_C,Q_D		23	22		21	18		23	22	ns
t_{PHL}					23	38		21	34		23	38	
t_{PLH}	LS196	Load	Any		22	34		20	30		22	34	ns
t_{PHL}					33	49		31	45		33	49	
t_{PLH}	LS197	Load	Any		22	34		20	30		22	34	ns
t_{PHL}					33	49		31	45		33	49	
t_{PHL}	LS196	Clear	Any		34	49		32	45		34	49	ns
t_{PHL}	LS197	Clear	Any		34	49		32	45		34	49	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

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Switching Characteristics, V_{cc} = 5V Over Recommended Free-Air Temperature Range

Parameter		From (Input)	To (output)	-55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)													
f_{max}	LS196	Clock 1	Q_A				48	74					MHz
f_{max}	LS197	Clock 1	Q_A				48	64					MHz
t_{PLH}	LS196	Clock 1	Q_A		14	20		11	16		14	20	ns
t_{PHL}					18	24		15	20		18	24	
t_{PLH}	LS197	Clock 1	Q_A		14	20		11	16		14	20	ns
t_{PHL}					18	24		15	20		18	24	
t_{PLH}	LS196	Clock 2	Q_B		17	23		14	19		17	23	ns
t_{PHL}					20	27		17	23		20	27	
t_{PLH}	LS197	Clock 2	Q_B		16	23		13	19		16	23	ns
t_{PHL}					19	26		16	22		19	26	
t_{PLH}	LS196	Clock 2	Q_C		28	42		25	38		28	42	ns
t_{PHL}					35	48		32	44		35	48	
t_{PLH}	LS197	Clock 2	Q_C		28	42		25	38		28	42	ns
t_{PHL}					32	42		29	38		32	42	
t_{PLH}	LS196	Clock 2	Q_D		17	26		14	22		17	26	ns
t_{PHL}					22	27		19	24		22	27	
t_{PLH}	LS197	Clock 2	Q_D		40	60		37	54		40	60	ns
t_{PHL}					46	65		43	59		46	65	
t_{PLH}	LS196	A, B, C, D	Q_A, Q_B, Q_C, Q_D		18	27		15	22		18	27	ns
t_{PHL}					27	43		24	38		27	43	
t_{PLH}	LS197	A, B, C, D	Q_A, Q_B, Q_C, Q_D		27	27		24	22		27	27	ns
t_{PHL}					27	43		24	38		27	43	
t_{PLH}	LS196	Load	Any		26	39		23	34		26	39	ns
t_{PHL}					37	54		34	49		37	54	
t_{PLH}	LS197	Load	Any		26	39		23	34		26	39	ns
t_{PHL}					37	54		34	49		37	54	
t_{PHL}	LS196	Clear	Any		38	54		35	49		38	54	
t_{PHL}	LS197	Clear	Any		38	54		35	49		38	54	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.