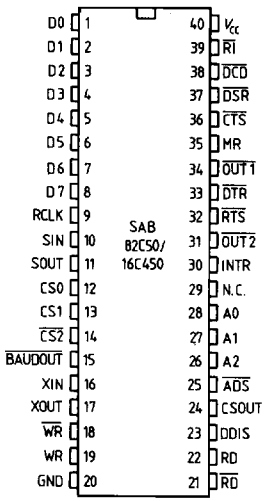
SAB 82C50/SAB 16C450 Universal Asynchronous Receiver/Transmitter

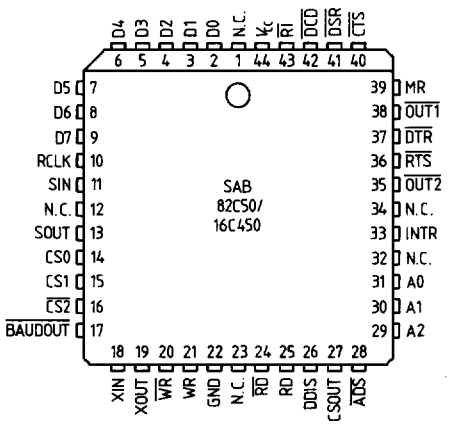
- Easily interfaces to most popular microprocessors
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from a serial data stream
- Holding and shift registers eliminate the need for precise synchronization between the CPU and the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to (2^{16}-1) and generates the internal 16× clock
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD)
- False start bit detection
- Complete status reporting capabilities
- Fully programmable serial interface characteristics:
  - 5/6/7/8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, $1^1/_2$, or 2-stop bit generation
  - Baud rate generation (DC to 512Kbaud)
- Tri-state TTL drive capability for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Fully prioritized interrupt system controls
- P-DIP-40 and PL-CC-44 packages

Pin Configurations

P-DIP-40



PL-CC-44



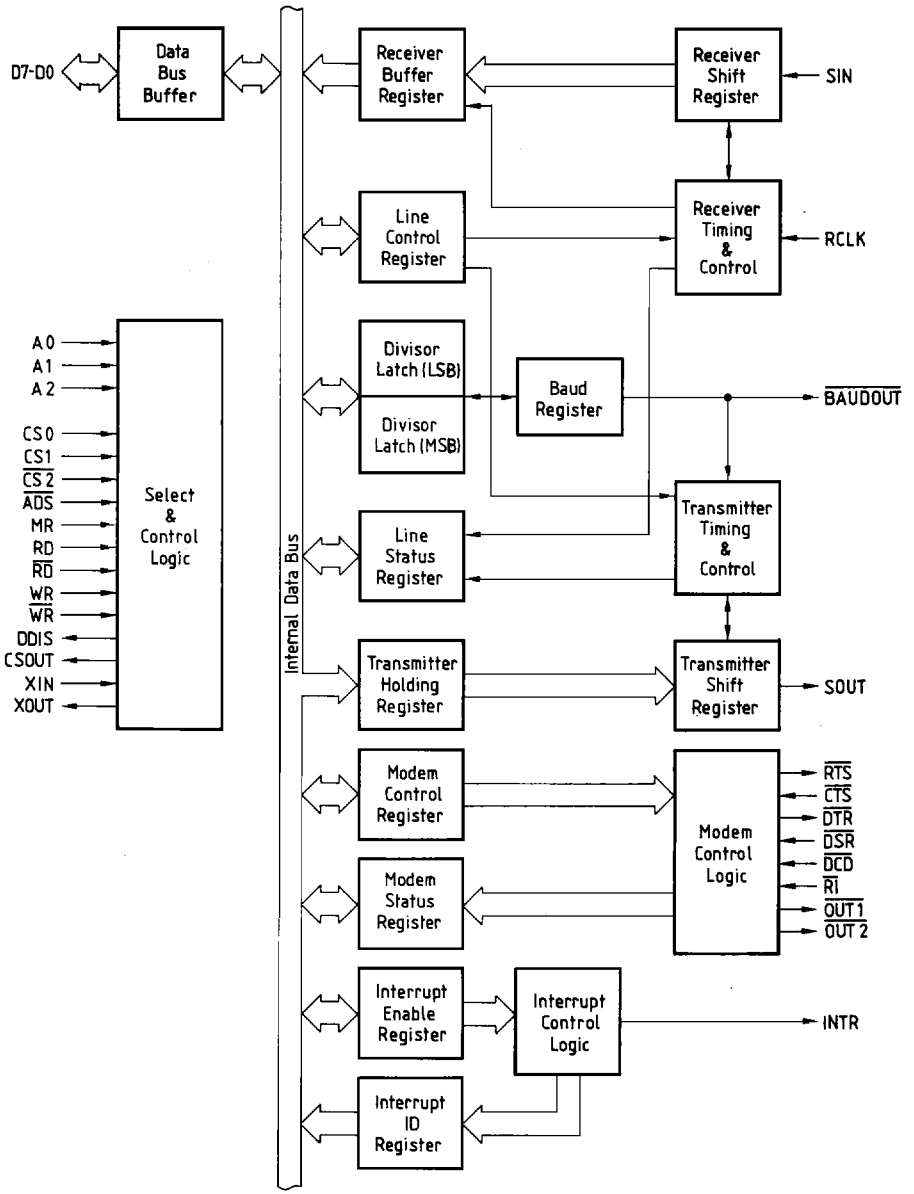
The SAB 82C50/16C450 (UART) performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error condition (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by 1 to (2^{16}-1), and of producing a 16× clock for driving the internal transmitter logic. Provisions have also been made to use this 16× clock for driving the receiver logic.

The UART features full modem-control capability and a processor interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing necessary for handling the communications link.

The SAB 82C50/16C450 is fabricated in Siemens ACMOS technology and comes in a 40-pin plastic dual-in-line package (P-DIP-40) or in a 44-pin plastic leaded chip carrier (PL-CC-44). The SAB 82C50/16C450 is compatible to the industry standard 8250/16450 communication controller.

Block Diagram



Pin Definitions and Functions

Symbol	Pin[1])	Input (I) Output (O)	Function
D0-D7	1-8	I/O	**Data bus** This bus comprises eight tri-state input/output lines. The bus provides bidirectional communication between the UART and the CPU. Data, control words, and status information are transferred via the D0-D7 data bus.
RCLK	9	I	**Receiver clock** This input is the 16× baud rate clock input for the receiver section of the chip.
SIN	10	I	**Serial data in** Serial data input from the communications link (peripheral device, modem, or data set).
SOUT	11	O	**Serial data out** This is the composite serial data output to the communications link (peripheral, modem or data set). The SOUT signal is set to the marking (logic 1) state upon a master reset operation or when the transmitter is idle.
CS0 CS1 $\overline{CS2}$	12 13 14	I I I	**Chip select** When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of an active address strobe signal latches the decoded chip select signals, completing chip selection. If $\overline{ADS}$ is always low, valid chip selects should stabilize according to the t_{CSW} parameter.
$\overline{BAUDOUT}$	15	O	**$\overline{Baud\ rate\ out}$** This is the 16× clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the baud rate generator divisor latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.
XIN XOUT	16 17	I O	**Oscillator in/out** These two pins connect the main timing reference (crystal or signal clock) to the UART. When a crystal oscillator or a clock signal is provided, it drives the UART via XIN (see typical clock circuits).
$\overline{WR}$ WR	18 19	I I	**Write/$\overline{Write}$** When WR is high or $\overline{WR}$ is low while the chip is selected, the CPU can write control words or data into the selected UART register. **Note:** Only one active WR or $\overline{WR}$ input is required to transfer data to the UART during a write operation. Therefore, tie either the WR input permanently low or the $\overline{WR}$ input permanently high, when it is not used.

[1]) Pin numbers are related to the plastic dual-in-line package (P-DIP-40).

Pin Definitions and Functions (cont'd)

Symbol	Pin[1]	Input (I) Output (O)	Function
$\overline{RD}$ RD	21 22	I I	**Read** When RD is high or $\overline{RD}$ is low while the chip is selected, the CPU can read status information or data from the selected UART register. **Note:** Only one active RD or $\overline{RD}$ input is required to transfer data from the UART during a read operation. Therefore, tie either the RD input permanently low or the $\overline{RD}$ input permanently high, when it is not used.
DDIS	23	O	**Driver disable** This signal goes low whenever the CPU is reading data from the UART. It can disable or control the direction of a data bus transceiver between the CPU and the UART.
CSOUT	24	O	**Chip select out** When high, this signal indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. CSOUT goes low when the UART is deselected.
$\overline{ADS}$	25	I	**Address strobe** The positive edge of active address strobe ($\overline{ADS}$) signal latches the register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$) signals. **Note:** An active $\overline{ADS}$ input is required when the register select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.
A2-A0	26-28	I	**Address 2–0** Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown in the following. Note that the state of the divisor latch access bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the baud rate generator divisor latches.

Register Addresses

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver buffer (read), transmitter holding register (write)
0	0	0	1	Interrupt enable
X	0	1	0	Interrupt identification (read only)
X	0	1	1	Line control
X	1	0	0	Modem control
X	1	0	1	Line status
X	1	1	0	Modem status
X	1	1	1	Scratch
1	0	0	0	Divisor latch (least significant byte)
1	0	0	1	Divisor latch (most significant byte)

[1]) Pin numbers are related to the plastic dual-in-line package (P-DIP-40).

Pin Definitions and Functions (cont'd)

Symbol	Pin[1]	Input (I) Output (O)	Function
INTR	30	O	**Interrupt request** This signal goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: receiver line status; received data available; transmitter holding register empty; and modem status. The INTR signals is reset low upon the appropriate interrupt service or a master reset operation.
$\overline{OUT2}$	31	O	**$\overline{Output\ 2}$** This user-designated output can be set to an active low by programming bit 3 (OUT 2) of the modem control register to a high level. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
$\overline{RTS}$	32	O	**$\overline{Request\ to\ send}$** When low, this signal informs the modem or data set that the UART is ready to exchange data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the modem control register. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
$\overline{DTR}$	33	O	**$\overline{Data\ terminal\ ready}$** When low, this informs the modem or data set that the UART is ready to establish a communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the modem control register to a high level. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
$\overline{OUT1}$	34	O	**$\overline{Output\ 1}$** This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the modem control register to a high level. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
MR	35	I	**Master reset** When this input is high, all the registers (except for the receiver buffer, transmitter holding, and divisor latches) and the control logic of the UART are cleared. The states of various output signals (SOUT, INTR, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to Table 2). This input is buffered with a TTL-compatible Schmitt trigger with 0.5 V typical hysteresis.
$\overline{CTS}$	36	I	**$\overline{Clear\ to\ send}$** When low, this signal indicates that the modem or data set is ready to exchange data. The $\overline{CTS}$ signal is a modem status input whose condition can be tested by the CPU reading bit 4 (CTS) of the modem status register. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the modem status register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the modem status register. $\overline{CTS}$ has no effect on the transmitter. **Note:** Whenever the CTS bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

[1]) Pin numbers are related to the plastic dual-in-line package (P-DIP-40).

Pin Definitions and Functions (cont'd)

Symbol	Pin[1]	Input (I) Output (O)	Function
$\overline{DSR}$			**$\overline{Data\ set\ ready}$** When low, this signal indicates that the modem or data set is ready to establish the communication link with the UART. The $\overline{DSR}$ signal is a modem status input whose condition can be tested by the CPU reading bit 5 (DSR) or the modem status register. Bit 5 is the complement of the $\overline{DSR}$ signal. Bit 1 (DDSR) of the modem status register indicates whether the $\overline{DSR}$ input has changed since the previous reading of the modem status register. **Note:** Whenever the DSR bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.
$\overline{DCD}$	38	I	**$\overline{Data\ carrier\ detect}$** When low, it indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a modem status whose condition can be tested by the CPU reading bit 7 (DCD) of the modem status register. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the modem status register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the modem status register. $\overline{DCD}$ has no effect on the receiver. **Note:** Whenever the DCD bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.
$\overline{RI}$	39	I	**$\overline{Ring\ indicator}$** When low, this signal indicates that a telephone ringing signal has been received by the modem or data set. The $\overline{RI}$ signal is a modem status input whose condition can be tested by the CPU reading bit 6 (RI) of the modem status register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the modem status register indicates whether the $\overline{RI}$ input signal has changed from a low to a high state since the previous reading of the modem status register. **Note**: Whenever the RI bit of the modem status register changes from a high to a low state, an interrupt is generated if the modem status interrupt is enabled.
V_{CC}	40	–	**Power supply** (+5V)
GND	20	–	**Ground** (0V)

[1]) Pin numbers are related to the plastic dual-in-line package (P-DIP-40).

Register Description

Table 1: Summary of Registers

	Register Address				
	0 (DLAB = 0)	0 (DLAB = 0)	1 (DLAB = 0)	2	3
Bit no.	Receiver buffer register (read only)	Transmitter holding register (write only)	Interrupt enable register	Interrupt ident. register (read only)	Line control register
	RBR	THR	IER	IIR	LCR
0	Data bit 0 [1]	Data bit 0 [1]	Received data available	"0" if interrupt is pending	Word length select bit 0 (WLS0)
1	Data bit 1	Data bit 1	Transmitter holding register empty	Interrupt ID bit 0	Word length select bit 1 (WLS1)
2	Data bit 2	Data bit 2	Receiver line status	Interrupt ID bit 1	Number of stop bits (STB)
3	Data bit 3	Data bit 3	Modem status	0	Parity enable (PEN)
4	Data bit 4	Data bit 4	0	0	Even parity select (EPS)
5	Data bit 5	Data bit 5	0	0	Stick parity
6	Data bit 6	Data bit 6	0	0	Set break
7	Data bit 7	Data bit 7	0	0	Divisor latch access bit (DLAB)

[1]) Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

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Table 1: Summary of Registers (cond't)

	Register Address					
	4	5	6	7	0 (DLAB = 1)	1 (DLAB = 1)
Bit no.	Modem control register	Line status register	Modem status register	Scratch register	Divisor latch (LS)	Divisor latch (MS)
	MCR	LSR	MSR	SCR	DLL	DLM
0	Data terminal ready (DTR)	Data ready (DR)	Delta clear to send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to send (RTS)	Overrun error (OE)	Delta data set ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Out 1	Parity error (PE)	Trailing edge ring indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Out 2	Framing error (FE)	Delta data carrier detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Loop	Break interrupt (BI)	Clear to send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter holding register (THRE)	Data set ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter empty (TEMT)	Ring indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	0	Data carrier detect (DCD)	Bit 7	Bit 7	Bit 15

Table 2: Register Reset Functions

Register/signal	Reset control	Reset state
Interrupt enable register	Master reset	**0000** 0000 [1]
Interrupt identification register	Master reset	**0000 0001**
Line control register	Master reset	0000 0000
Modem control register	Master reset	**0000** 0000
Line status register	Master reset	**0**110 0000
Modem status register	Master reset	XXXX 0000 [2]
SOUT	Master reset	High
INTR (RCVR errors)	Read LSR/MR	Low
INTR (RCVR data ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/write THR/MR	Low
INTR (Modem status changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master reset	High
$\overline{\text{RTS}}$	Master reset	High
$\overline{\text{DTR}}$	Master reset	High
$\overline{\text{OUT 1}}$	Master reset	High

[1]) Boldface bits are permanently low.
[2]) Bits 7-4 are driven by the input signals.

The system programmer may access any of the UART registers summarized in Table 1 via the CPU. These registers control UART operations including transmission and reception of data. Each register bit in Table 1 has its name and reset state shown in Table 2.

Line control register

The system programmer specifies the format of the asynchronous data communication exchange and sets the divisor latch access bit via the line control register (LCR). The programmer can also read the contents of the line control register. The read capability simplifies system programming and eliminates the need for separate storage of the line characteristics in system memory.

Table 1 shows the contents of the LCR. Details on each bit follow:

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one stop bit is generated or checked in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, irrespective of the number of stop bits selected.

Bit 3: This bit is the parity enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).

Bit 4: This bit is the even parity select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's is transmitted or checked.

Bit 5: This bit is the stick parity bit. When bits 3, 4 and 5 are logic 1, the parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is logic 0 then the parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 stick parity is disabled.

Bit 6: This bit is the break control bit. It causes a break condition to be transmitted by the UART. When it is set to a logic 1, the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by clearing bit 6 to a logic 0. The break control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all O's pad character in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission is to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the divisor latch access bit (DLAB). It must be set high (logic 1) to access the divisor latches of the baud generator during a read or write operation. It must be set low (logic 0) to access the receiver buffer, the transmitter holding register or the interrupt enable register.

Table 3: Baud Rates Using 1.8432 MHz Crystal

Desired baud rate	Decimal divisor used to generate 16 x clock	Percent error difference between desired and actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Programmable Baud Rate Generator

The UART contains a programmable baud rate generator that is capable of taking any clock input from DC to 8.0 MHz (SAB 16C450 only; SAB 82C50 : 3.1 MHz) and dividing it by any divisor from 1 to 2^{16}. The output frequency of the baud rate generator is 16 x the baud rate [divisor = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded.

Tables 3, 4 and 5 provide decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 8 MHz, respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommendable.

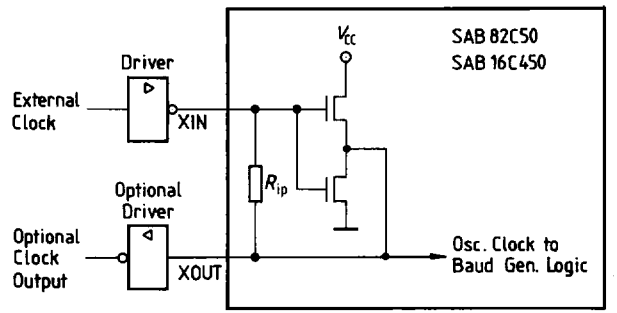
Table 4: Baud Rates Using 3.072 MHz Crystal

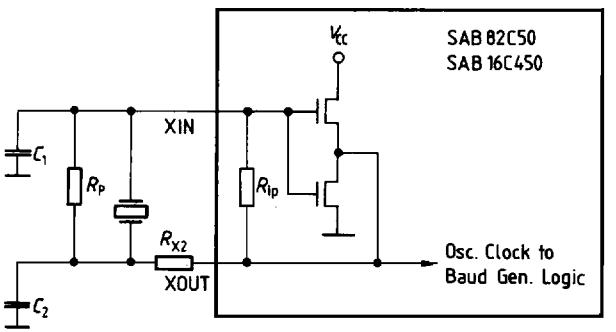
Desired baud rate	Decimal divisor used to generate 16 x clock	Percent error difference between desired and actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Table 5: Baud Rates Using 8 MHz Crystal

Desired baud rate	Decimal divisor used to generate 16 x clock	Percent error difference between desired and actual
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

Typical Clock Circuits





Typical Oscillator Networks

Crystal [1]	R_p [2]	R_{x2}	C_1	C_2
1.8-8.0 MHz	1MΩ	1.5k	10-30 pF	40-60 pF

[1] Crystal > 3.1 MHz SAB 16C450 only.
[2] Due to internal R_{ip} external, R_p may be dropped.

Line Status Register

This 8-bit register provides the CPU with status information concerning the data transfer. Table 1 shows the contents of the line status register. Details on each bit follow:

Bit 0: This bit is the receiver data ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 is reset to a logic 0 reading the data in the receiver buffer register.

Bit 1: This bit is the overrun error (OE) indicator. Bit 1 indicates that data in the receiver buffer register was not read by the CPU **before** the transfer of the next character into the receiver buffer register, thus destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the line status register.

Bit 2: This bit is the parity error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or ood parity, as selected by the even parity select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the line status register.

Bit 3: This bit is the framing error (FE) indicator. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic 1 whenever the stop bit following the last data bit or parity bit is a logic 0 (spacing level). The FE indicator is reset whenever the CPU reads the contents of the line status register. The UART will try to resynchronize after a framing error. Therefore, it assumes that the framing error was due to the next start bit, samples this "start" bit twice and then takes in the "data".

Bit 4: This bit is the break interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (i.e., the total time of start bit + data bits + parity + stop bits).
The BI indicator is reset whenever the CPU reads the contents of the line status register. Restarting after a break is received requires the SIN pin to be logic 1 for at least ½ bit time.

Note: Bits 1 through 4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Table 6: Interrupt Control Functions

Interrupt identification register				Interrupt set and reset functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority level**	**Interrupt type**	**Interrupt source**	**Interrupt reset control**
0	0	1	–	None	None	–
1	1	0	Highest	Receiver line status	Overrun error or parity error or framing error or break interrupt	Reading the line status register
1	0	0	Second	Received data available	Receive data available	Reading the receiver buffer register
0	1	0	Third	Transmitter holding register empty	Transmitter holding register empty	Reading the IIR register (if source of interrupt) or Writing into the transmitter holding register
0	0	0	Fourth	modem status	Clear to send or data set ready or ring indicator or data carrier detect	Reading the modem status register

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Bit 5: This bit is the transmitter holding register empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the transmitter holding register empty interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logic 0 whenever the CPU loads the transmitter holding register.

Bit 6: This bit is the transmitter empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: The line status register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

Interrupt Identification Register

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt identification register. The four levels of interrupt conditions in order of priority are: receiver line status, received data ready, transmitter holding register empty and modem status.
When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table 1 shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 6.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This register enables the four types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt enable register (IER). Similarly, setting bits of this register to a logic 1 enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. Table 1 shows the contents of the IER. Details on each bit follow:

Bit 0: This bit enables the received data available interrupt when set to logic 1.

Bit 1: This bit enables the transmitter holding register empty interrupt when set to logic 1.

Bit 2: This bit enables the receiver status interrupt when set to logic 1.

Bit 3: This bit enables the modem status interrupt when set to logic 1.

Bit 4 through 7: These four bits are always logic 0.

Modem Control Register

This register controls the interface to the Modem or data set (or a peripheral device emulating a Modem). The contents of the Modem control register (MCR) are indicated in Table 1 and are described below. Details on each bit follow:

Bit 0: This bit controls the data terminal ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Note: The $\overline{DTR}$ output of the UART may be applied to an EIA inverting line driver (such as the 1488) to obtain the proper polarity input at the succeeding Modem or data set.

Bit 1: This bit controls the request to send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the output ($\overline{OUT\ 1}$) signal, which is an auxiliary user-signated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter serial output (SOUT) is set to the marking (logic 1) state; the receiver serial input (SIN) is disconnected; the output of the transmitter shift register is "looped back" into the receiver shift register input; the four Modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; and the four Modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four Modem control inputs. The Modem control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem control interrupts are also operational, but the interrupt's sources are now the lower four bits of the Modem control register instead of the four Modem control inputs. The interrupts are still controlled by the interrupt enable register.

Bits 5 through 7: These bits are permanently set to logic 0.

Modem Status Register

This register provides the current state of the control lines from the Modem (or peripheral device) to the CPU. In addition to this current-state information, four bits of the Modem status register provide change information. These bits are set to a logic 1 whenever a control input from the Modem changes state. They are reset to logic 0 whenever the CPU reads the Modem status register.

Table 1 shows the contents of the MSR. Details on each bit follow:

Bit 0: This bit is the delta clear to send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the delta data set ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the trailing edge of ring indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the delta data carrier detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2 or 3 is set to logic 1, a Modem status interrupt is generated.

Bit 4: This bit is the complement of the clear to send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the data set ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

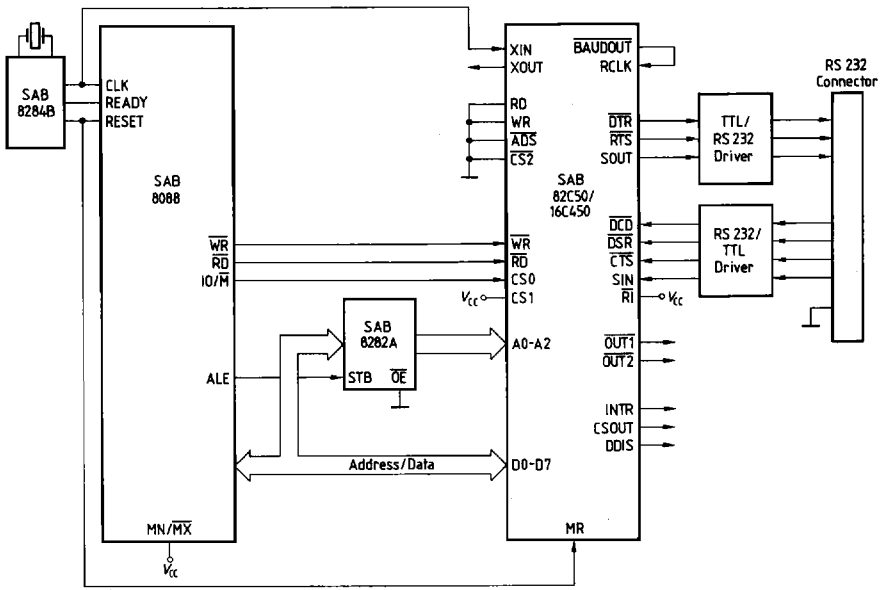
Bit 6: This bit is the complement of the ring indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the data carrier detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 in the MCR.

Scratchpad Register

This 8-bit read/write register does not control the UART in any way. It is intended as a scratch-pad register to be used by the programmer to hold data temporarily.

Typical Application



Absolute Maximum Ratings

Ambient temperature under bias	0° to	70°C
Storage temperature	−65° to	+150°C
Supply voltage	−0.5 to	+ 7.0V
Voltage on any pin with respect to ground	−0.5 to	V_{CC} + 0.5V
Power dissipation		700mW

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5V ± 5%; GND = 0V

Parameter	Symbol	Limit values		Units	Test conditions
		min.	max.		
Input low voltage	V_{IL}	−0.5	0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.4	V	I_{OL} = 1.6 mA [1])
Output high voltage	V_{OH}	2.4		V	I_{OH} = −1.0 mA [1])
Avg. power supply current	I_{CC} (AV)	–	10	mA	V_{CC} = 5.25V, T_A = 25°C No loads on output SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2.4V All other inputs = 0.4V Baud rate generator is 4 MHz Baud rate is 50 Kbaud
Input leakage current	I_{IL}	–	± 10	µA	V_{CC} = 5.25V, GND = 0V All other pins floating. V_{IN} = 0V, 5.25V
Clock leakage current	I_{CL}	–	± 20	µA	
Tri-state leakage current	I_{OZ}	–	± 20	µA	V_{CC} = 5.25V, GND = 0V V_{OUT} = 0V, 5.25V 1. Chip deselected 2. WRITE mode, chip selected
MR Schmitt V_{IL}	V_{ILMR}	–	0.8	V	–
MR Schmitt V_{IH}	V_{IHMR}	2.0	–	V	–

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Capacitance [2]

$T_A = 25°C$; $V_{CC} = GND = 0V$

Parameter	Symbol	Limit values		Units	Test conditions
		min.	max.		
Clock input capacitance	C_{XIN}	–	20	pF	$f_c = 1$ MHz Unmeasured pins returned to GND
Clock output capacitance	C_{XOUT}	–	30	pF	
Input capacitance	C_{IN}	–	10	pF	
Output capacitance	C_{OUT}	–	20	pF	

[1]) Does not apply to XOUT.
[2]) These parameters are periodically sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5V ± 5%; GND = 0V

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 16C450		SAB 82C50			
		min.	max.	min.	max.		
Address strobe width	t_{ADS}	60	–	90	–	ns	–
Address hold time	t_{AH}	0	–	0	–	ns	–
RD, $\overline{RD}$ delay from address	t_{AR}	30	–	80	–	ns	1)
Address setup time	t_{AS}	60	–	90	–	ns	–
WR, $\overline{WR}$ delay from address	t_{AW}	30	–	80	–	ns	1)
Chip select hold time	t_{CH}	0	–	0	–	ns	–
Chip select setup time	t_{CS}	60	–	90	–	ns	–
Chip select output delay from select	t_{CSC}	–	100	–	125	ns	100 pF loading 1)
RD, $\overline{RD}$ delay from chip select	t_{CSR}	30	–	80	–	ns	1)
WR, $\overline{WR}$ delay from select	t_{CSW}	30	–	80	–	ns	1)
Data hold time	t_{DH}	30	–	60	–	ns	–
Data setup time	t_{DS}	30	–	90	–	ns	–
RD, $\overline{RD}$ to floating data delay	t_{HZ}	0	100	0	100	ns	100 pF loading 2)
Master reset pulse width	t_{MR}	5	–	10	–	µs	–
Address hold time from RD, $\overline{RD}$	t_{RA}	20	–	20	–	ns	1)
Read cycle delay	t_{RC}	125	–	500	–	ns	–
Chip select hold time from RD, $\overline{RD}$	t_{RCS}	20	–	20	–	ns	1)
RD, $\overline{RD}$ strobe width	t_{RD}	125	–	175	–	ns	–
RD, $\overline{RD}$ to driver disable delay	t_{RDD}	–	60	–	75	ns	100 pF loading 2)
Delay from RD, $\overline{RD}$ to data	t_{RVD}	–	125	–	175	ns	100 pF loading
Address hold time from WR, $\overline{WR}$	t_{WA}	20	–	20	–	ns	1)
Write cycle delay	t_{WC}	150	–	500	–	ns	–
Chip select hold time from WR, $\overline{WR}$	t_{WCS}	20	–	20	–	ns	1)

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AC Characteristics (cont'd)

T_A = 0 to 70°C; V_{CC} = 5V ± 5%; GND = 0V

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 16C450		SAB 82C50			
		min.	max.	min.	max.		
WR, $\overline{WR}$ strobe width	t_{WR}	100	–	175	–	ns	–
Duration of clock high pulse	t_{XH}	55	–	140	–	ns	[3]
Duration of clock low pulse	t_{XL}	55	–	140	–	ns	[3]
Read cycle = $t_{AR} + t_{RD} + t_{RC}$	RC	280	–	755	–	ns	–
Write cycle = $t_{AW} + t_{WR} + t_{WC}$	WC	280	–	755	–	ns	–

[1] Applicable only when $\overline{ADS}$ is tied low.
[2] Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.
[3] SAB 82C50: External clock max. 3.1 MHz
SAB 16C450: External clock max. 8.0 MHz

Baud Rate Generator

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 16C450		SAB 82C50			
		min.	max.	min.	max.		
Baud divisor	N	1	2^{16}-1	1	2^{16}-1		–
Baud output positive edge delay	t_{BHD}	–	175	–	250	ns	100 pF load
Baud output negative edge delay	t_{BLD}	–	175	–	250	ns	100 pF load
Baud output up time	t_{HW}	75	–	250	–	ns	[1]
Baud output down time	t_{LW}	100	–	425	–	ns	[2]

[1] SAB 16C450: f_x = 8.0 MHz, ÷ 2, 100 pF load
SAB 82C50: f_x = 3.0 MHz, ÷ 3, 100 pF load

[2] SAB 16C450: f_x = 8.0 MHz, ÷ 2, 100 pF load
SAB 82C50: f_x = 2.0 MHz, ÷ 2, 100 pF load

Receiver and Transmitter

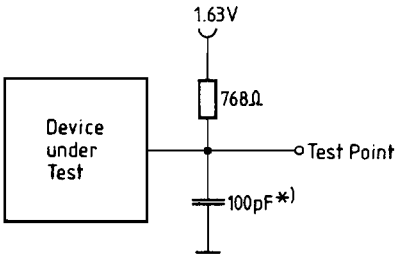
Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 16C450		SAB 82C50			
		min.	max.	min.	max.		
Delay from RD, $\overline{RD}$ (RD RBR or RD LSR) to reset interrupt	t_{RINT}	–	1	–	1	µs	100 pF load
Delay from RCLK to sample time	t_{SCD}	–	2	–	2	µs	–
Delay from stop to set interrupt	t_{SINT}	–	1	–	1	RCLK cycles	[1]
Delay from WR, $\overline{WR}$ (WR THR) to reset interrupt	t_{HR}	–	175	–	1000	ns	100 pF load
Delay from RD, $\overline{RD}$ (RD IIR) to reset interrupt (THRE)	t_{IR}	–	250	–	1000	ns	100 pF load
Delay from initial INTR reset to transmit start	t_{IRS}	24	40	24	40	BAUD-OUT cycles	–
Delay from initial write to interrupt	t_{SI}	32	48	32	48	BAUD-OUT cycles	–
Delay from stop to interrupt (THRE)	t_{STI}	8	8	8	8	BAUD-OUT cycles	–

[1] RCLK is equal to t_{XH} and t_{XL}.

Modem Control

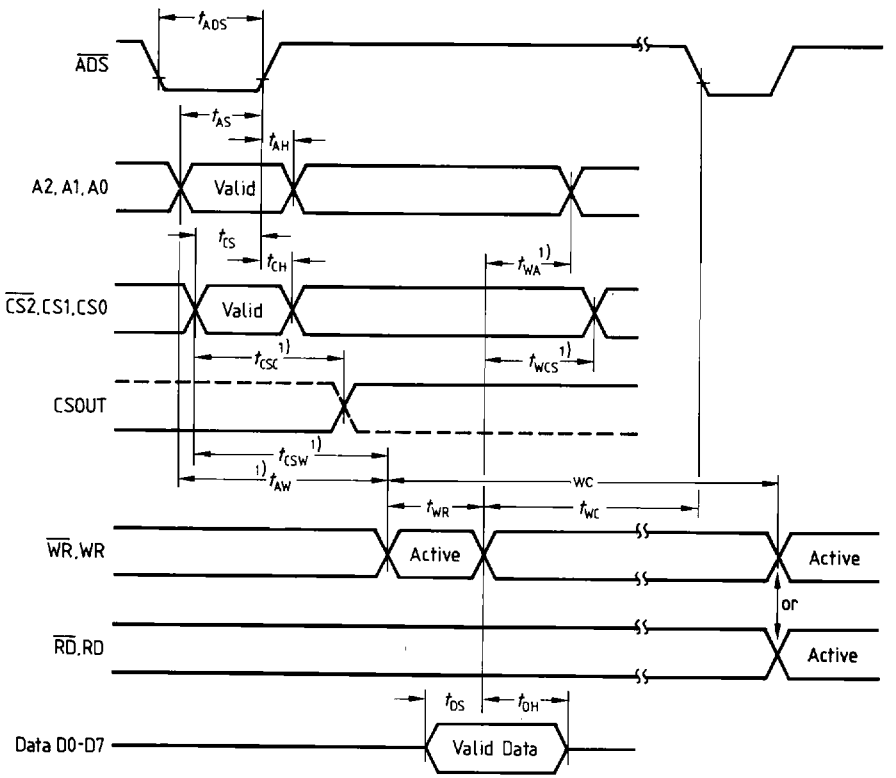
Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 16C450		SAB 82C50			
		min.	max.	min.	max.		
Delay from WR, $\overline{WR}$ (WR MCR) to output	t_{MDO}	–	200	–	1000	ns	100 pF load
Delay to reset interrupt from RD, $\overline{RD}$ (RD MSR)	t_{RIM}	–	250	–	1000	ns	100 pF load
Delay to set interrupt from Modem input	t_{SIM}	–	250	–	1000	ns	100 pF load

AC Test Circuit



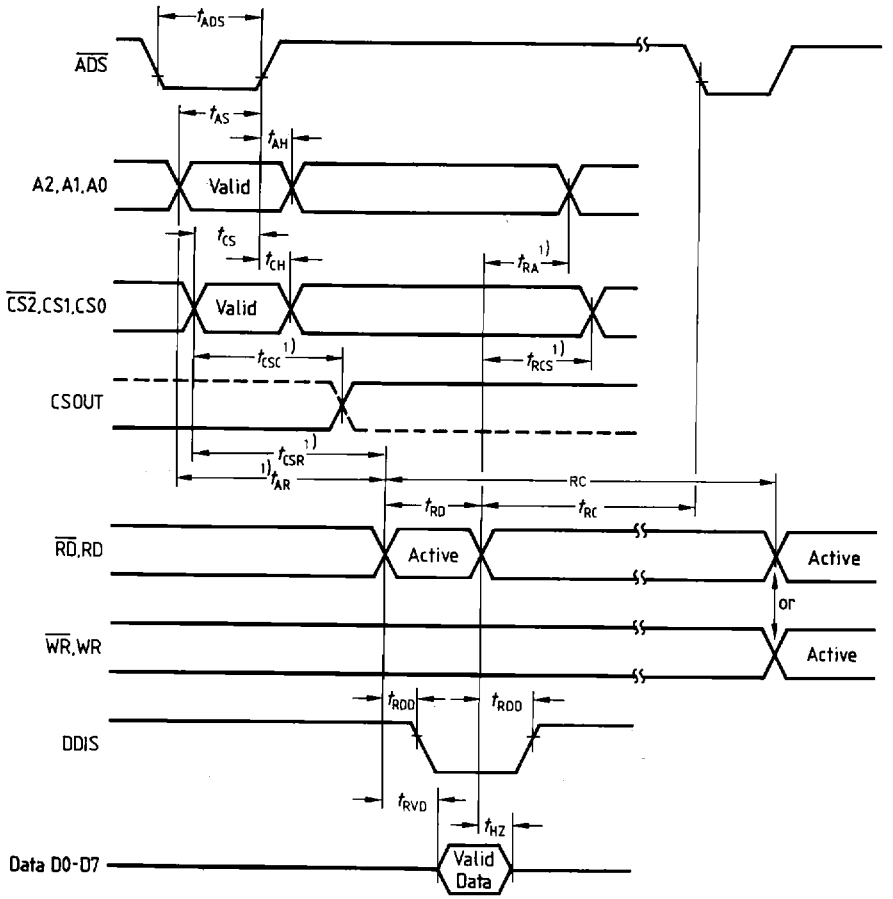
*) Includes stray and jig capacitance

Write Cycle Timing



1) Applicable only when ADS is tied low.

Read Cycle Timing



1) Applicable only when $\overline{ADS}$ is tied low.

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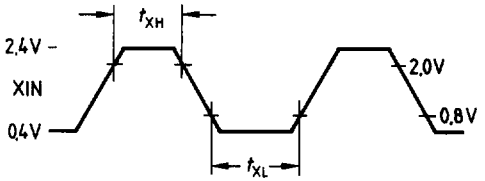
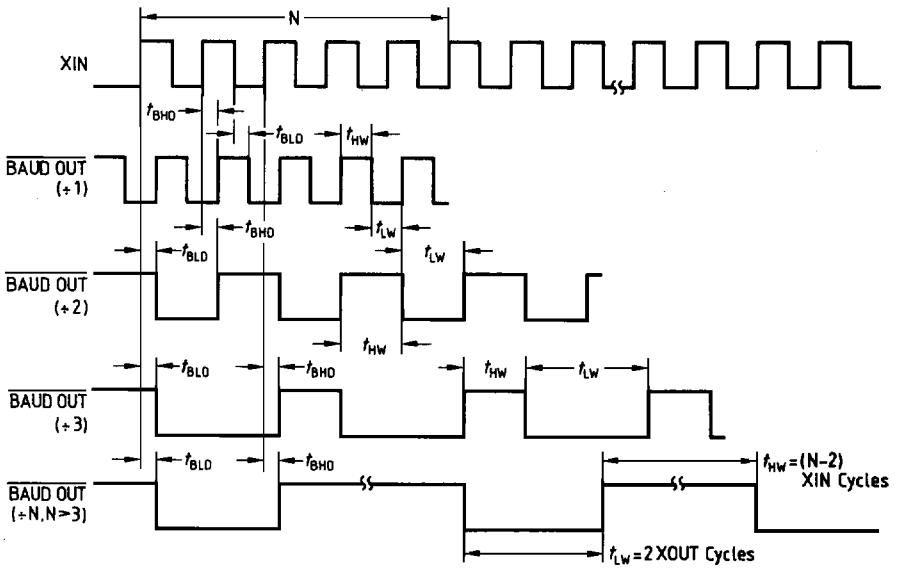
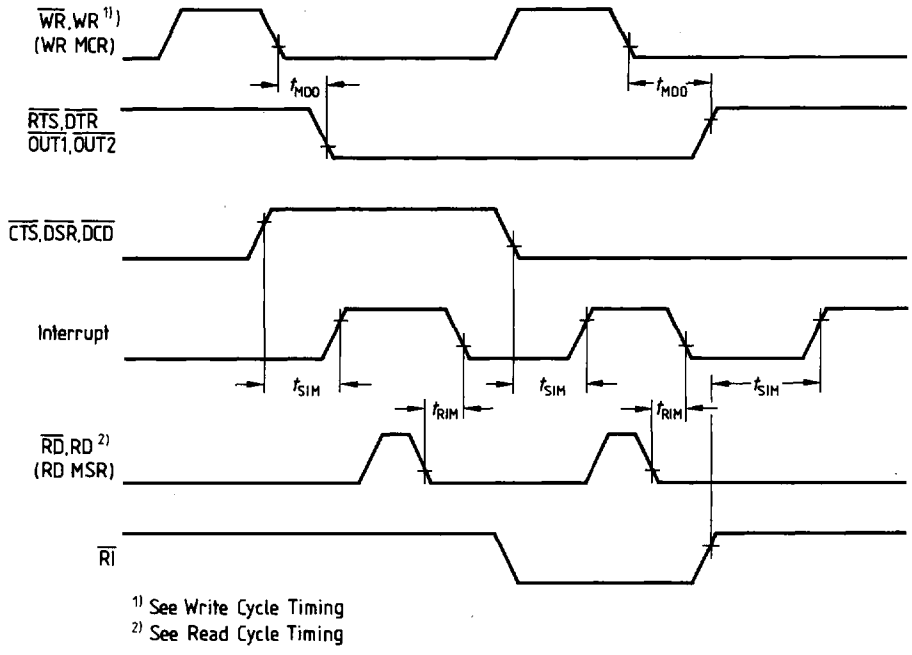
External Clock Input Timing



BAUDOUT Timing

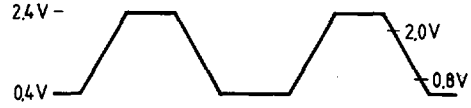


Modem Control Timing



1) See Write Cycle Timing
2) See Read Cycle Timing

AC Test Points



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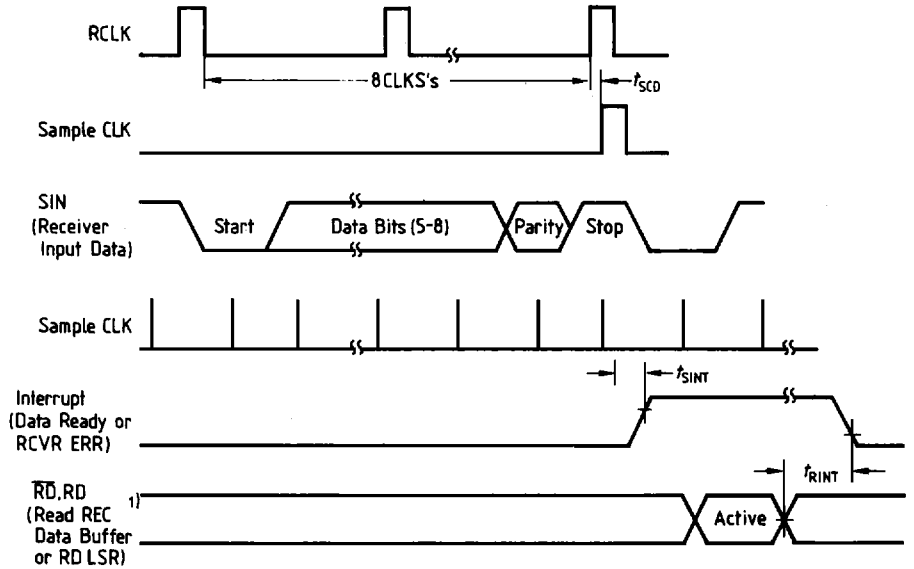
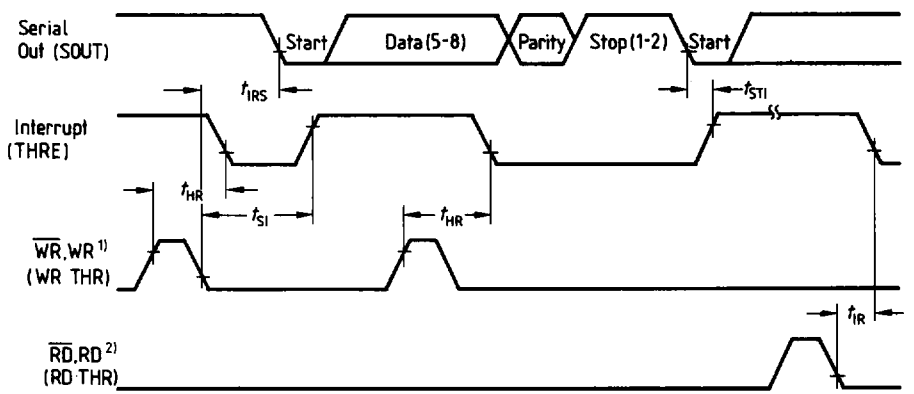
Receiver Timing



1) See Read Cycle Timing

Transmitter Timing



1) See Write Cycle Timing
2) See Read Cycle Timing