# DATA SHEET

# 74LVC139
## Dual 2-to-4 line decoder/demultiplexer

Product specification
Supersedes data of 1998 Apr 28

2003 May 19

Philips Semiconductors

PHILIPS

# Dual 2-to-4 line decoder/demultiplexer 74LVC139

## FEATURES

- Wide supply voltage range from 1.2 to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 85 °C
- In accordance with JEDEC standard no. 8-1A
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.

## DESCRIPTION

The 74LVC139 is a high-performance, low-voltage and low-power Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs ($nA_0$ and $nA_1$) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW input ($n\overline{E}$).

When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f \leq 2.5$ ns.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | propagation delay | $C_L$ = 50 pF; $V_{CC}$ = 3.3 V | | |
| | nA to $n\overline{Y}_n$ | | 3.3 | ns |
| | $n\overline{E}$ to $n\overline{Y}_n$ | | 3.2 | ns |
| $C_I$ | input capacitance | | 5.0 | pF |
| $C_{PD}$ | power dissipation capacitance per multiplexer | $V_{CC}$ = 3.3 V; notes 1 and 2 | 36 | pF |

### Notes

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   $f_i$ = input frequency in MHz;
   $f_o$ = output frequency in MHz;
   $C_L$ = output load capacitance in pF;
   $V_{CC}$ = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_I$ = GND to $V_{CC}$.

## FUNCTION TABLE

See note 1

| INPUT | | | OUTPUT | | | |
|---|---|---|---|---|---|---|
| $n\overline{E}$ | $nA_0$ | $nA_1$ | $n\overline{Y}_0$ | $n\overline{Y}_1$ | $n\overline{Y}_2$ | $n\overline{Y}_3$ |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | H | L | H | L | H | H |
| L | L | H | H | H | L | H |
| L | H | H | H | H | H | L |

**Note**

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | | |
|---|---|---|---|---|---|
| | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE |
| 74LVC139D | –40 to +85 °C | 16 | SO16 | plastic | SOT109-1 |
| 74LVC139DB | –40 to +85 °C | 16 | SSOP16 | plastic | SOT338-1 |
| 74LVC139PW | –40 to +85 °C | 16 | TSSOP16 | plastic | SOT403-1 |
| 74LVC139BQ | –40 to +85 °C | 16 | DHVQFN16 | plastic | SOT763-1 |

**PINNING**

| PIN | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | $1\overline{E}$ | enable input (active LOW) |
| 2 | $1A_0$ | address input |
| 3 | $1A_1$ | address input |
| 4 | $1\overline{Y}_0$ | output (active LOW) |
| 5 | $1\overline{Y}_1$ | output (active LOW) |
| 6 | $1\overline{Y}_2$ | output (active LOW) |
| 7 | $1\overline{Y}_3$ | output (active LOW) |
| 8 | GND | ground (0 V) |
| 9 | $2\overline{Y}_3$ | output (active LOW) |
| 10 | $2\overline{Y}_2$ | output (active LOW) |
| 11 | $2\overline{Y}_1$ | output (active LOW) |
| 12 | $2\overline{Y}_0$ | output (active LOW) |
| 13 | $2A_1$ | address input |
| 14 | $2A_0$ | address input |
| 15 | $2\overline{E}$ | enable input (active LOW) |
| 16 | $V_{CC}$ | positive supply voltage |

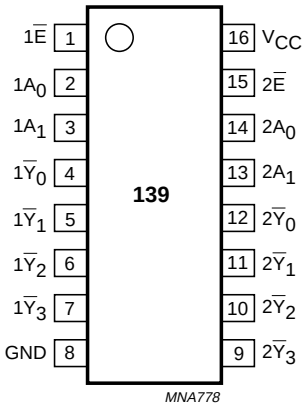
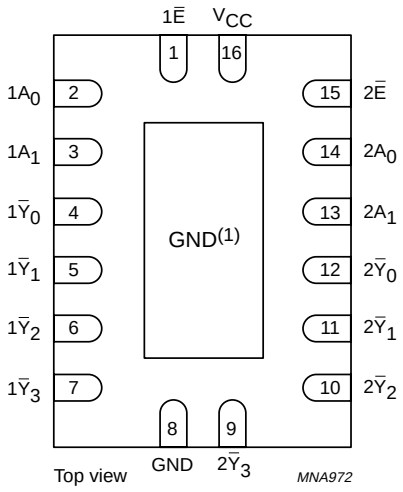



Fig.1 Pin configuration SO16 and (T)SSOP16.




(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN16.

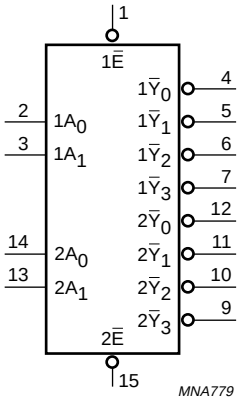
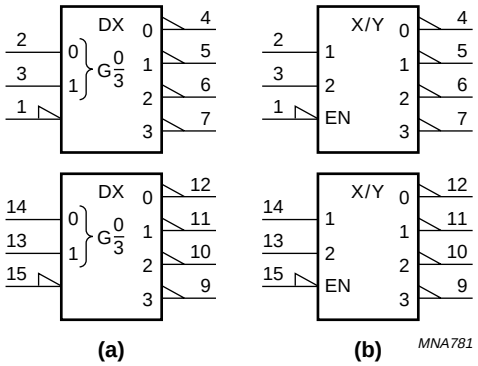



Fig.3 Logic symbol.




a) demultiplexer. b) decoder.

Fig.4 Logic symbol (IEEE/IEC).

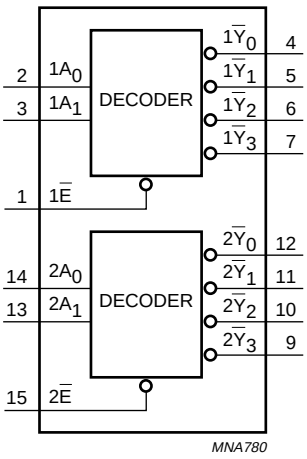



Fig.5 Functional diagram.

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | for maximum speed performance | 2.7 | 3.6 | V |
| | | for low-voltage applications | 1.2 | 3.6 | V |
| $V_I$ | input voltage | | 0 | 5.5 | V |
| $V_O$ | output voltage | | 0 | $V_{CC}$ | V |
| $T_{amb}$ | operating ambient temperature | in free air | –40 | +85 | °C |
| $t_r$, $t_f$ | input rise and fall times | $V_{CC}$ = 1.2 to 2.7 V | 0 | 20 | ns/V |
| | | $V_{CC}$ = 2.7 to 3.6 V | 0 | 10 | ns/V |

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | –0.5 | +6.5 | V |
| $I_{IK}$ | input diode current | $V_I < 0$ | – | –50 | mA |
| $V_I$ | input voltage | note 1 | –0.5 | +5.5 | V |
| $I_{OK}$ | output diode current | $V_O > V_{CC}$ or $V_O < 0$ | – | ±50 | mA |
| $V_O$ | output voltage | note 1 | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_O$ | output source or sink current | $V_O$ = 0 to $V_{CC}$ | – | ±50 | mA |
| $I_{CC}$, $I_{GND}$ | $V_{CC}$ or GND current | | – | ±100 | mA |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $P_{tot}$ | power dissipation per package | $T_{amb}$ = –40 to +85 °C; note 2 | – | 500 | mW |

**Notes**

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO16 packages: above 70 °C derate linearly with 8 mW/K.
   For SSOP16 and TSSOP16 packages: above +60 °C derate linearly with 5.5 mW/K.
   For DHVQFN16 packages: above +60 °C derate linearly with 4.5 mW/K.

**DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP.(1) | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = −40 to +85 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 1.2 | $V_{CC}$ | – | – | V |
| | | | 2.7 to 3.6 | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 1.2 | – | – | GND | V |
| | | | 2.7 to 3.6 | – | – | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = –12 mA | 2.7 | $V_{CC}$ – 0.5 | – | – | V |
| | | $I_O$ = –100 μA | 3.0 | $V_{CC}$ – 0.2 | $V_{CC}$ | – | V |
| | | $I_O$ = –12 mA | 3.0 | $V_{CC}$ – 0.6 | – | – | V |
| | | $I_O$ = –24 mA | 3.0 | $V_{CC}$ – 0.8 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 12 mA | 2.7 | – | – | 0.40 | V |
| | | $I_O$ = 100 μA | 3.0 | – | – | 0.20 | V |
| | | $I_O$ = 24 mA | 3.0 | – | – | 0.55 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 5.5 V or GND | 3.6 | – | ±0.1 | ±5 | μA |
| $I_{CC}$ | quiescent supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | 3.6 | – | 0.1 | 10 | μA |
| $\Delta I_{CC}$ | additional quiescent supply current per input pin | $V_I$ = $V_{CC}$ – 0.6 V; $I_O$ = 0 | 2.7 to 3.6 | – | 5 | 500 | μA |

**Note**

1. All typical values are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

**AC CHARACTERISTICS**

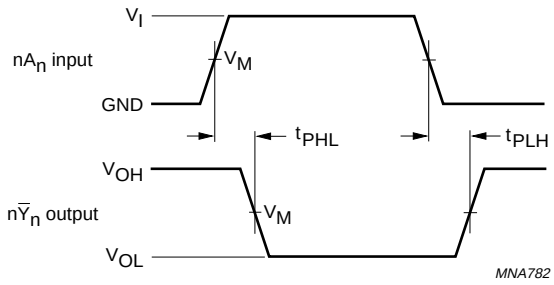
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L$ = 50 pF; $R_L$ = 500 Ω.

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP.(1) | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | WAVEFORM | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = −40 to +85 °C** | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay | | | | | | |
| | $nA_n$ to $\overline{Y}_n$ | see Figs 6 and 8 | 3.0 to 3.6 | 1.5 | 3.3 | 6.0 | ns |
| | $n\overline{E}$ to $\overline{Y}_n$ | see Figs 7 and 8 | 3.0 to 3.6 | 1.5 | 3.2 | 5.5 | ns |
| $t_{PHL}/t_{PLH}$ | propagation delay | | | | | | |
| | $nA_n$ to $\overline{Y}_n$ | see Figs 6 and 8 | 2.7 | – | – | 7.5 | ns |
| | $n\overline{E}$ to $\overline{Y}_n$ | see Figs 7 and 8 | 2.7 | – | – | 6.5 | ns |

**Note**

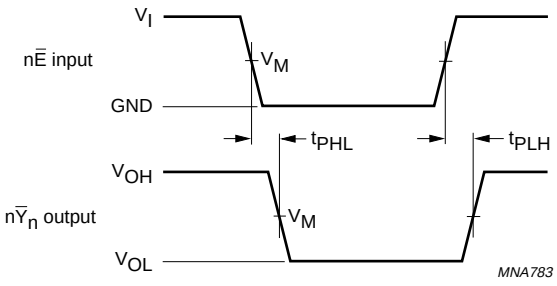
1. All typical values are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

## AC WAVEFORMS



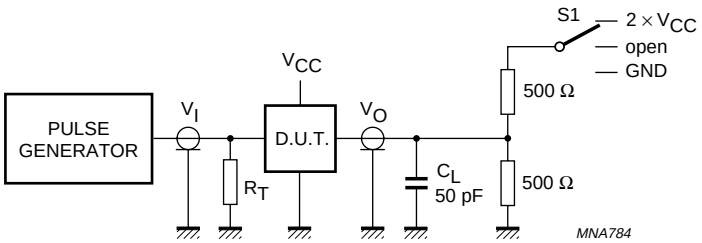

$V_M$ = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5V_{CC}$ at $V_{CC}$ < 2.7 V.
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.

Fig.6 Input ($nA_n$) to output ($n\overline{Y}_n$) propagation delays.




$V_M$ = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5V_{CC}$ at $V_{CC}$ < 2.7 V.
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.

Fig.7 Enable input ($n\overline{E}$) to output ($n\overline{Y}_n$) propagation delays.




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | open |

| $V_{CC}$ | $V_I$ |
|---|---|
| <2.7 V | $V_{CC}$ |
| 2.7 to 3.6 V | 2.7 V |

Definitions for test circuits:

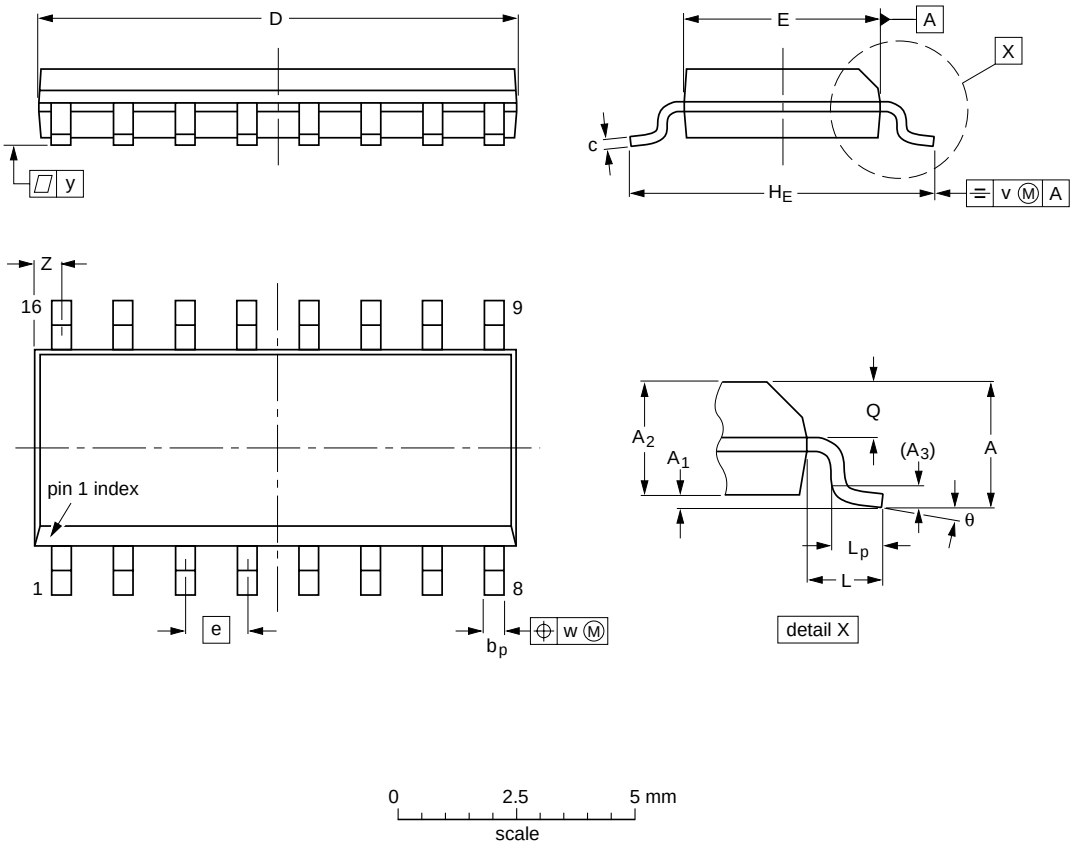
$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

Fig.8 Load circuitry for switching times.

## PACKAGE OUTLINES

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

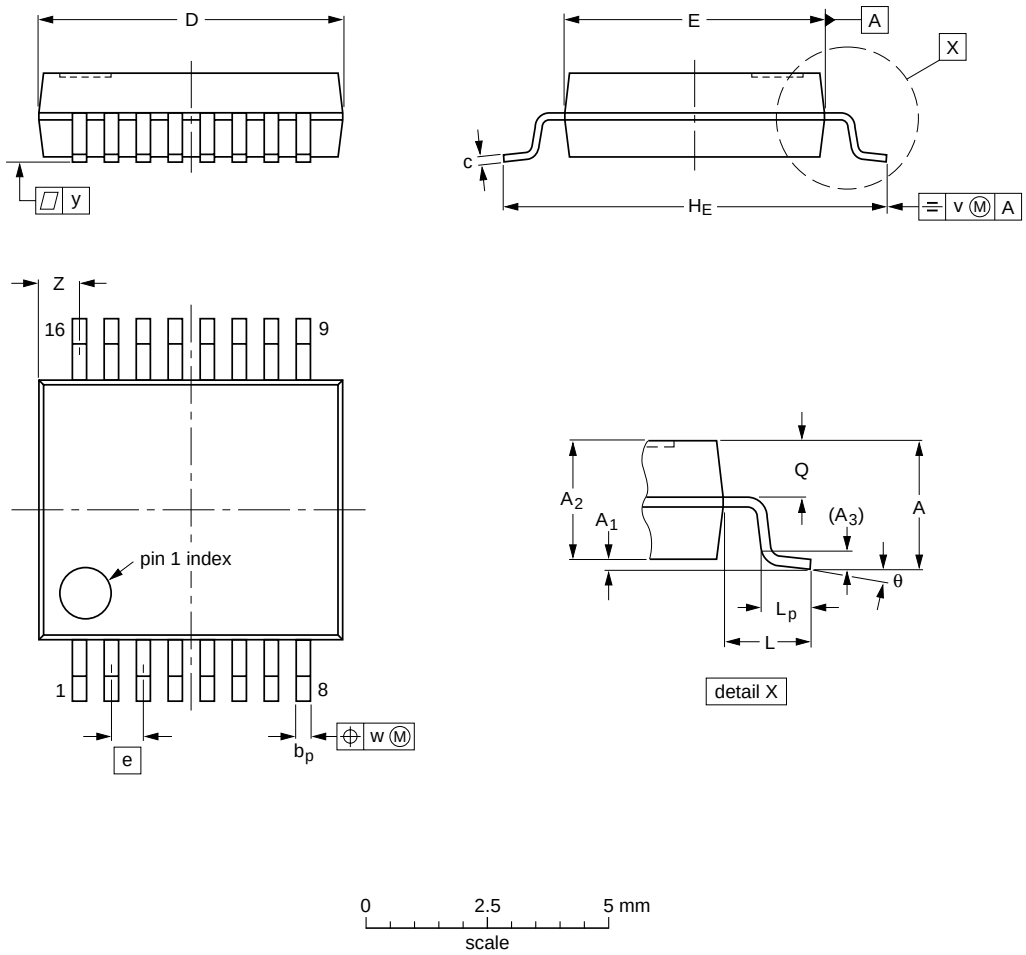
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm** **SOT338-1**




**DIMENSIONS (mm are the original dimensions)**

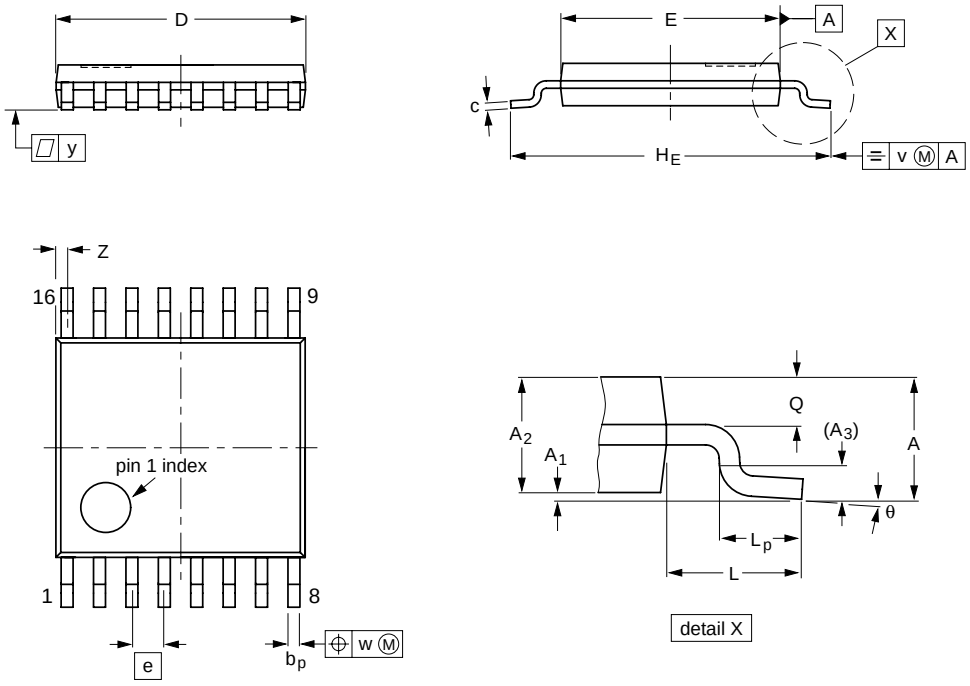
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.00<br>0.55 | $8^o$<br>$0^o$ |

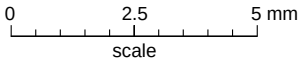
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT338-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

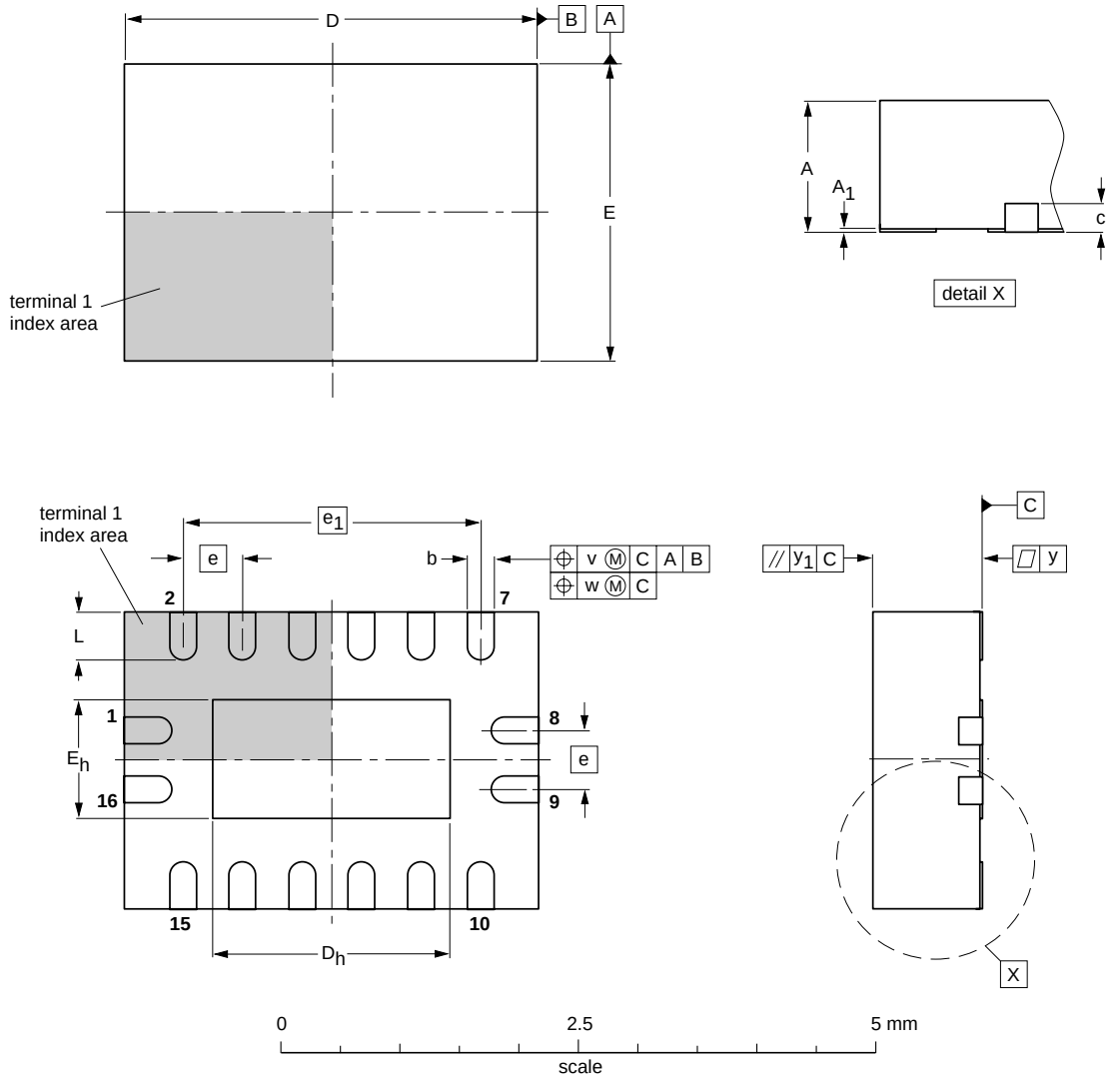
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm** **SOT763-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 3.6<br>3.4 | 2.15<br>1.85 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT763-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

## SOLDERING

### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 $mm^3$ so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 $mm^3$ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**Suitability of surface mount IC packages for wave and reflow soldering methods**

| PACKAGE[1] | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW[2] |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA | not suitable | suitable |
| DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable[3] | suitable |
| PLCC[4], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended[4][5] | suitable |
| SSOP, TSSOP, VSO, VSSOP | not recommended[6] | suitable |

**Notes**

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

**DATA SHEET STATUS**

| LEVEL | DATA SHEET STATUS(1) | PRODUCT STATUS(2)(3) | DEFINITION |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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**Notes**

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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