



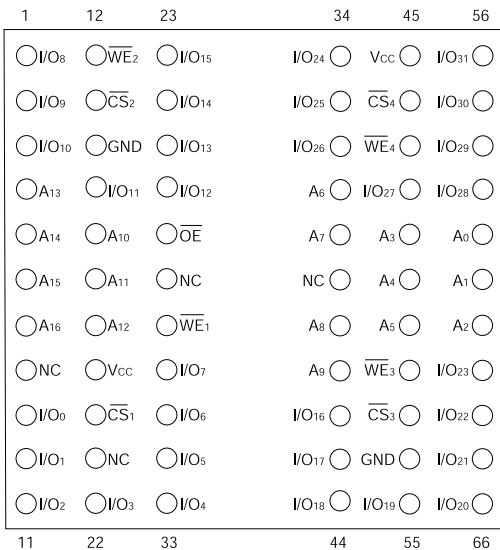
# 128Kx32 SRAM MODULE, SMD 5962-93187

## FEATURES

- Access Times of 70, 85, 100, 120ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400).
  - 68 lead, 40mm Low Profile CQFP, 3.56mm (0.140") (Package 502).
  - 68 lead, Hermetic CQFP, 22.4mm (0.880 inch) square. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint.
    - G2 (Package 500), 5.08mm (0.200 inch) high
    - G2U (Package 510), 4.57mm (0.140 inch) high
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  - WS128K32-XG2X - 8 grams typical
  - WS128K32-XG2UX - 8 grams typical
  - WS128K32-XH1X - 13 grams typical
  - WS128K32-XG4TX - 20 grams typical
- All devices are upgradeable to 512Kx32

FIG. 1 PIN CONFIGURATION FOR WS128K32N-XH1X

### TOP VIEW



### PIN DESCRIPTION

I/O <sub>0-31</sub>	Data Inputs/Outputs
A <sub>0-16</sub>	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V <sub>CC</sub>	Power Supply
GND	Ground
NC	Not Connected

### BLOCK DIAGRAM

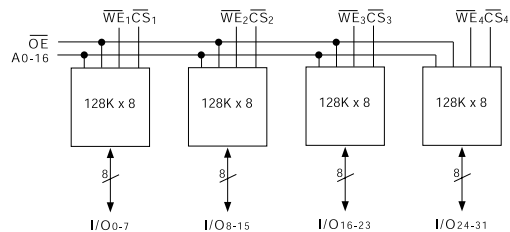




FIG. 2 PIN CONFIGURATION FOR WS128K32-XG4TX

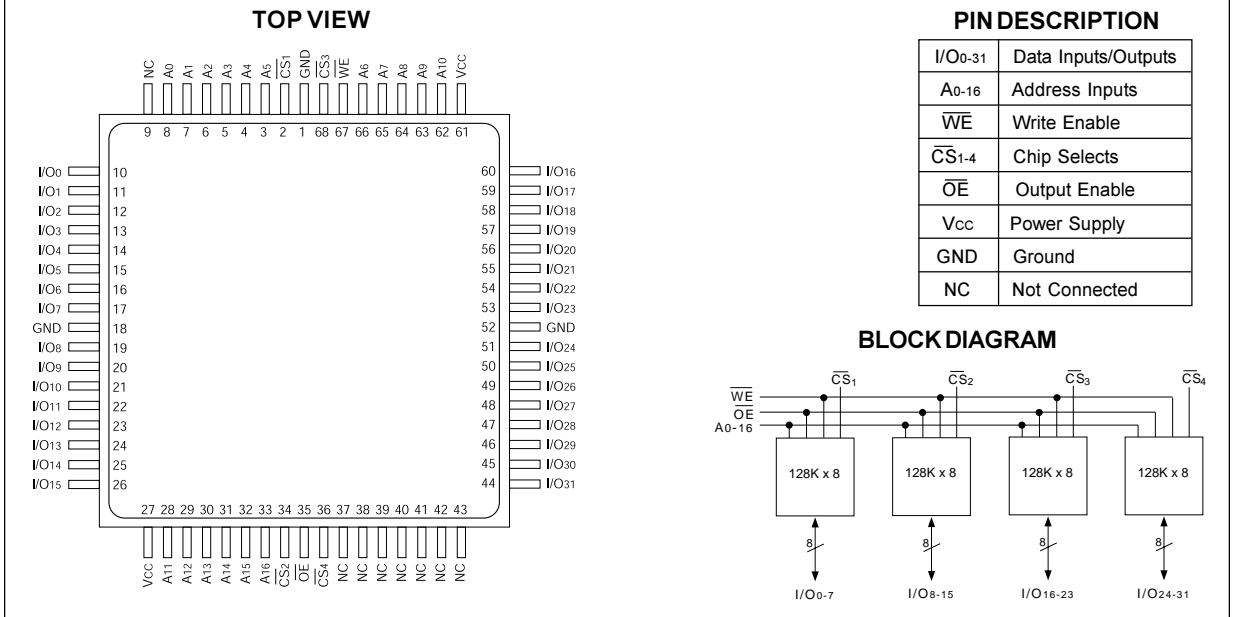
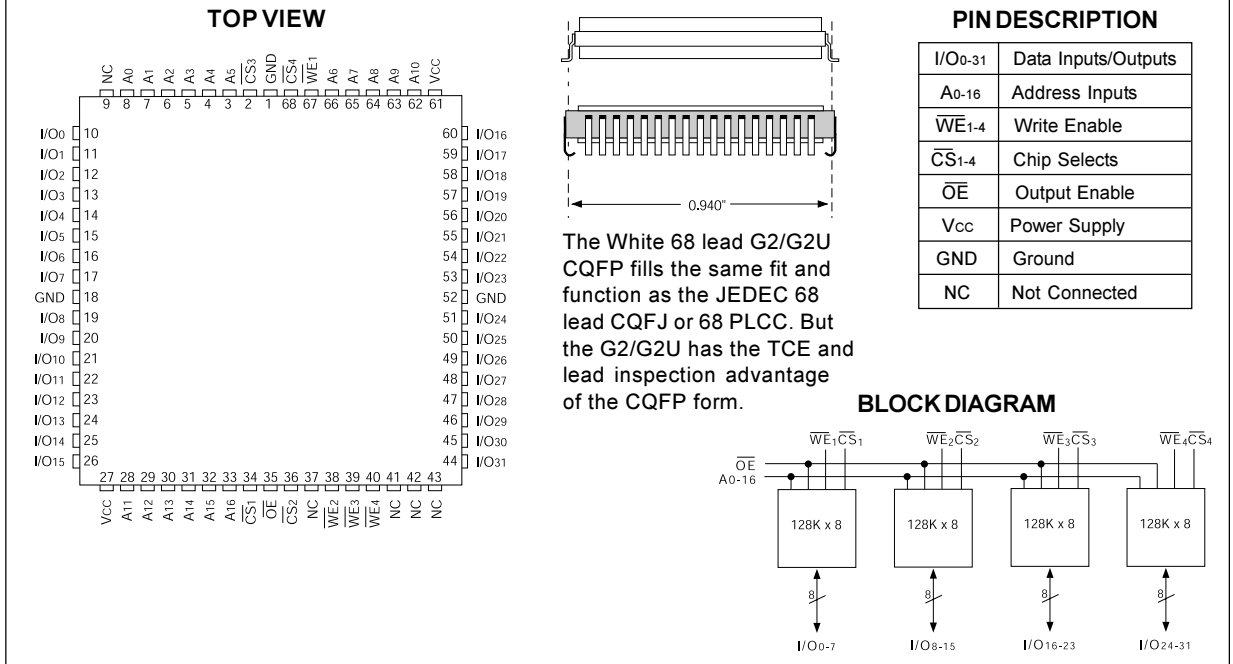


FIG. 3 PIN CONFIGURATION FOR WS128K32-XG2X AND WS128K32-XG2UX





**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V

**TRUTH TABLE**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

**CAPACITANCE**  
(T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ 1-4 capacitance HIP (PGA)	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20	pF
CQFP G4			50	
CQFP G2			20	
CQFP G2U			15	
$\overline{CS}$ 1-4 capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>IO</sub> = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS**

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Sym	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	ILI	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10		10		10		10	µA
Output Leakage Current	ILO	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10		10		10		10	µA
Operating Supply Current	I <sub>CC</sub>	$\overline{CS}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		120		120		120		120	mA
Standby Current	ISB	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		20		20		20		20	mA
Output Low Voltage	VOL	IOL = 2.1mA, V <sub>CC</sub> = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	VOH	IOH = -1.0mA, V <sub>CC</sub> = 4.5	2.4		2.4		2.4		2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

**DATA RETENTION CHARACTERISTICS**

(T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Data Retention Supply Voltage	V <sub>DR</sub>	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	5.5	2.0	5.5	2.0	5.5	2.0	5.5	V
Data Retention Current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3V		4		4		4		4	mA



**AC CHARACTERISTICS**  
(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C To +125°C)

Parameter	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	70		85		100		120		ns
Address Access Time	t <sub>AA</sub>		70		85		100		120	ns
Output Hold from Address Change	t <sub>OH</sub>	3		3		3		3		ns
Chip Select Access Time	t <sub>ACS</sub>		70		85		100		120	ns
Output Enable to Output Valid	t <sub>OE</sub>		35		45		50		60	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	3		3		3		3		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		0		0		0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		25		25		35		35	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		25		25		35		35	ns

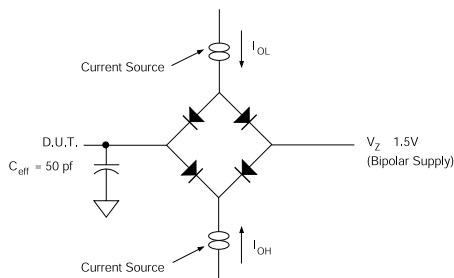
1. This parameter is guaranteed by design but not tested.

**AC CHARACTERISTICS**  
(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C To +125°C)

Parameter	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	70		85		100		120		ns
Chip Select to End of Write	t <sub>CW</sub>	60		75		80		100		ns
Address Valid to End of Write	t <sub>AW</sub>	60		75		80		100		ns
Data Valid to End of Write	t <sub>DW</sub>	30		35		40		50		ns
Write Pulse Width	t <sub>WP</sub>	50		55		70		80		ns
Address Setup Time	t <sub>AS</sub>	5		5		5		5		ns
Address Hold Time	t <sub>AH</sub>	5		5		5		5		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	5		5		5		5		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		25		25		35		35	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

**FIG. 4**  
**AC TEST CIRCUIT**



**AC TEST CONDITIONS**

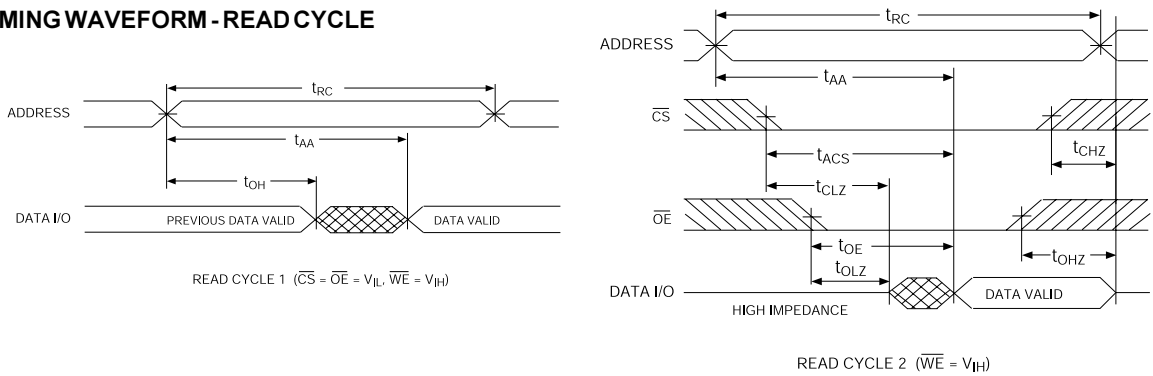
Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

**NOTES:**

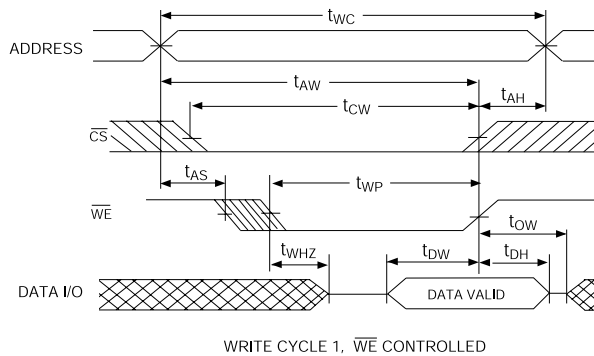
V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



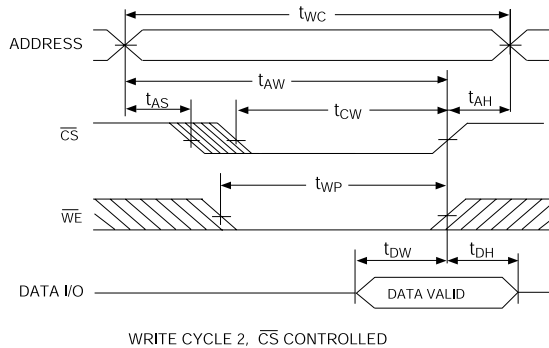
**FIG. 5**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 6**  
**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**

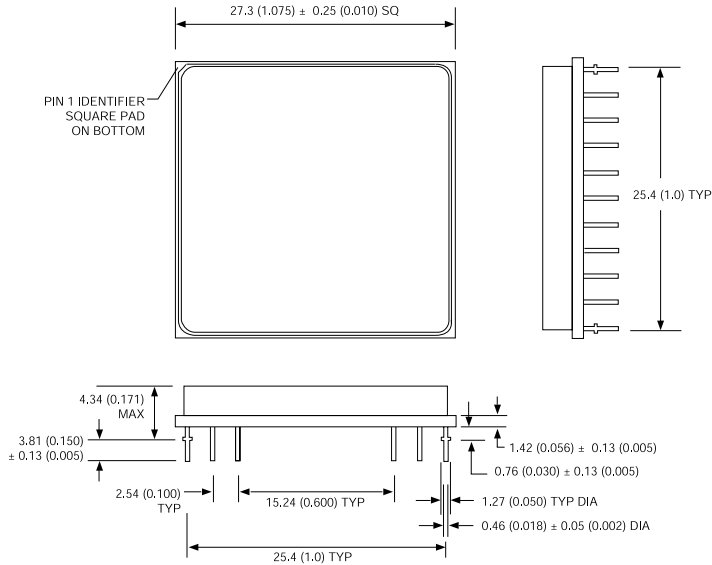


**FIG. 7**  
**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**



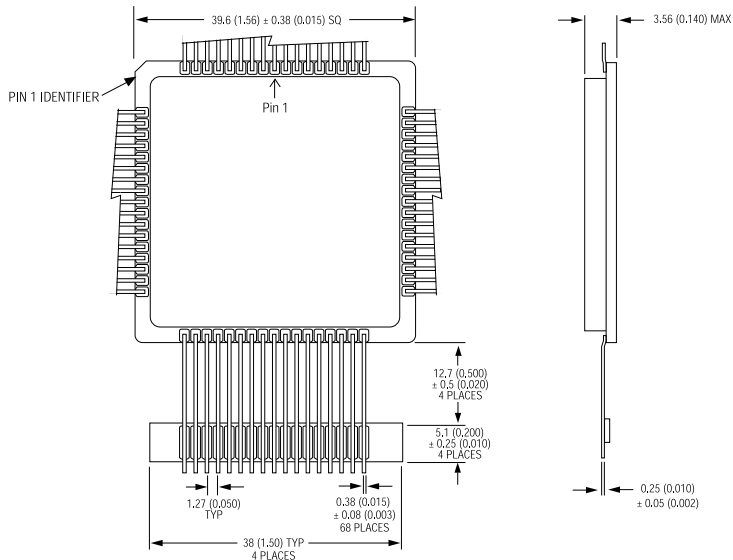


PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

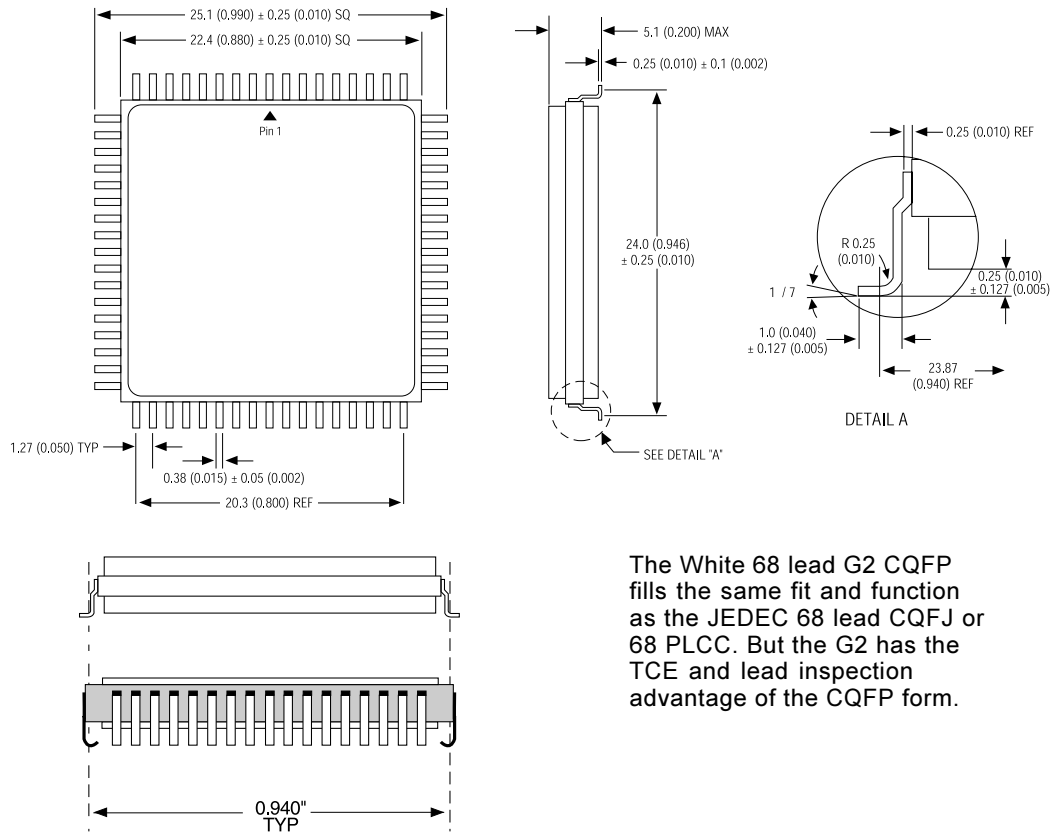
PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)

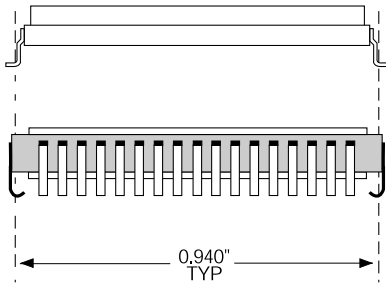
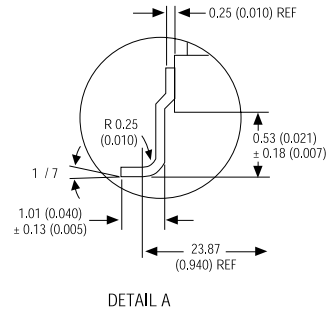
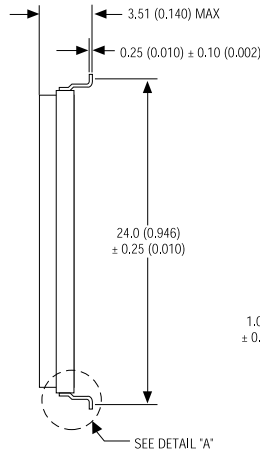
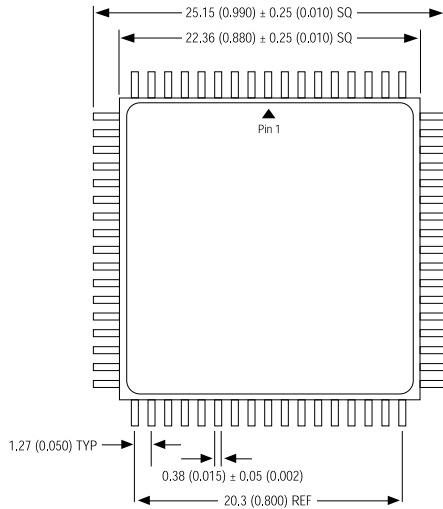


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)



The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES





**ORDERING INFORMATION**

**W S 128K 32 X - XXX X X X**

**LEAD FINISH:**

- Blank = Gold plated leads
- A = Solder dip leads

**DEVICE GRADE:**

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

**PACKAGE TYPE:**

- H1 = 1.075" sq. Ceramic Hex-In-line Package, HIP (Package 400)
- G2 = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 500)
- G2U = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 510)
- G4T = 40 mm Low Profile CQFP (Package 502)

**ACCESS TIME (ns)**

**IMPROVEMENT MARK:**

- N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades

**ORGANIZATION, 128Kx32**

- User configurable as 256Kx16 or 512Kx8

**SRAM**

**WHITE ELECTRONIC DESIGNS CORPORATION**



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 SRAM Module	120ns	66 pin HIP (H1)	5962-93187 01H5X
128K x 32 SRAM Module	100ns	66 pin HIP (H1)	5962-93187 02H5X
128K x 32 SRAM Module	85ns	66 pin HIP (H1)	5962-93187 03H5X
128K x 32 SRAM Module	70ns	66 pin HIP (H1)	5962-93187 04H5X
128K x 32 SRAM Module	120ns	68 lead CQFP/J (G2)	5962-95595 01HMX
128K x 32 SRAM Module	100ns	68 lead CQFP/J (G2)	5962-95595 02HMX
128K x 32 SRAM Module	85ns	68 lead CQFP/J (G2)	5962-95595 03HMX
128K x 32 SRAM Module	70ns	68 lead CQFP/J (G2)	5962-95595 04HMX
128K x 32 SRAM Module	120ns	68 lead CQFP/J (G2U)	5962-95595 01HNX
128K x 32 SRAM Module	100ns	68 lead CQFP/J (G2U)	5962-95595 02HNX
128K x 32 SRAM Module	85ns	68 lead CQFP/J (G2U)	5962-95595 03HNX
128K x 32 SRAM Module	70ns	68 lead CQFP/J (G2U)	5962-95595 04HNX
128K x 32 SRAM Module	120ns	68 lead CQFP Low Profile (G4T)	5962-95595 01HYX
128K x 32 SRAM Module	100ns	68 lead CQFP Low Profile (G4T)	5962-95595 02HYX
128K x 32 SRAM Module	85ns	68 lead CQFP Low Profile (G4T)	5962-95595 03HYX
128K x 32 SRAM Module	70ns	68 lead CQFP Low Profile (G4T)	5962-95595 04HYX