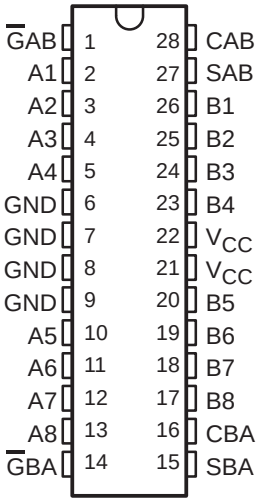
- **Inputs Are TTL-Voltage Compatible**
- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Inverting Data Paths**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enables GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

A low input level selects real-time data and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers. Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The 74ACT11651 is characterized for operation from – 40°C to 85°C.

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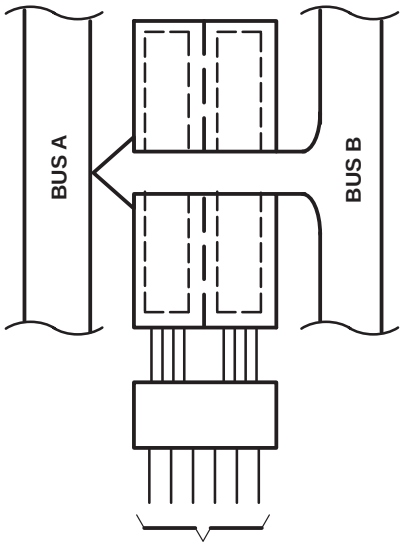
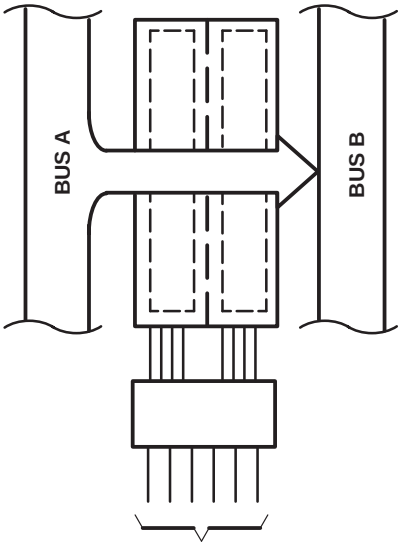


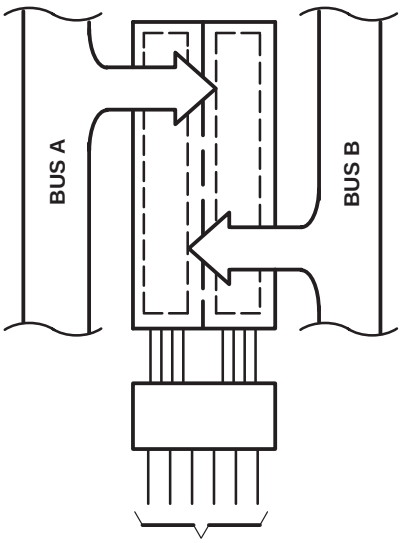
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



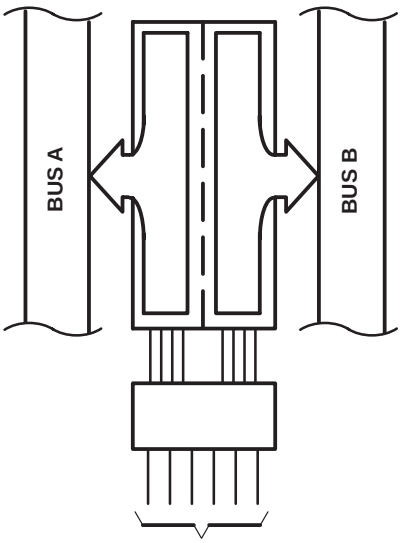
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

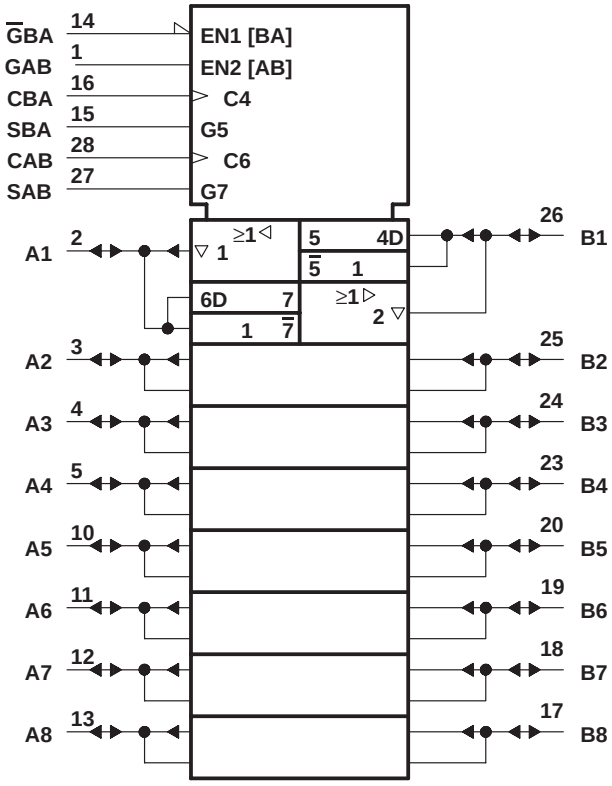
Figure 1. Bus Transfer Diagram

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, Hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, Store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus

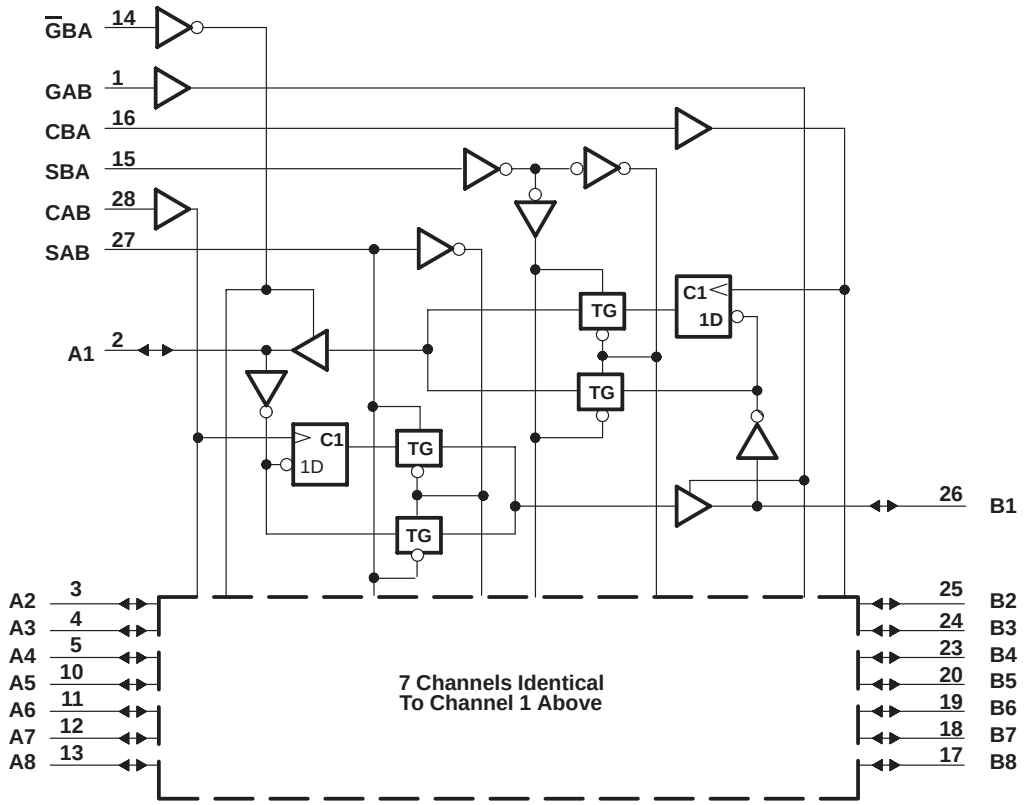
† The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously. Select control = H: clocks must be staggered in order to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . . ± 200 mA
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_{OZ}	A or B ports§	$V_I = V_{CC}$ or GND	5.5 V			± 0.5		± 5	μA
I_I	Control Inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡		$V_I = V_{CC}$ or GND	5.5 V			0.9		1	mA
C_i	Control Inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_{io}	A or B ports	$V_I = V_{CC}$ or GND	5 V		10				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	90	0	100	MHz
t_w	Pulse duration, CAB or CBA high or low	5.5		5		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	4.5		4.5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	2		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

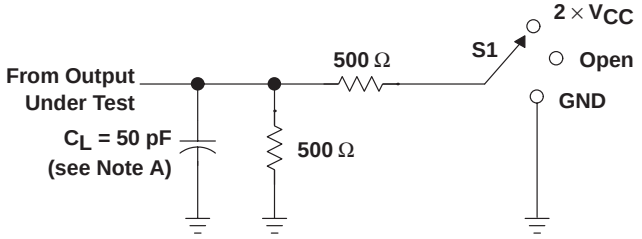
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			90			90		MHz
t_{PLH}	A or B	B or A	2.6	5.6	8.9	2.6	9.9	ns
t_{PHL}			4.7	7.7	10.7	4.7	11.9	
t_{PLH}	CBA or CAB	A or B	5.5	8.4	11.2	5.5	12.7	ns
t_{PHL}			6.3	9.5	12.7	6.3	14.1	
t_{PLH}	SBA or SAB† with A or B high	A or B	4.8	7.6	10.4	4.8	11.8	ns
t_{PHL}			4.1	7.7	11.2	4.1	12.4	
t_{PLH}	SBA or SAB† with A or B low	A or B	3	6.2	9.3	3	10.4	ns
t_{PHL}			5.6	8.7	11.7	5.6	13	
t_{PZH}	$\overline{G}$BA	A	4	7.4	10.7	4	11.9	ns
t_{PZL}			4.3	8.2	11.9	4.3	13.3	
t_{PHZ}	$\overline{G}$BA	A	5.9	7.7	9.5	5.9	10	ns
t_{PLZ}			5.1	6.9	8.7	5.1	9.2	
t_{PZH}	GAB	B	5.9	9	12.1	5.9	13.7	ns
t_{PZL}			6.4	9.8	13.2	6.4	14.9	
t_{PHZ}	GAB	B	4.7	7.1	9.5	4.7	10	ns
t_{PLZ}			3.8	6.1	8.4	3.8	8.8	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

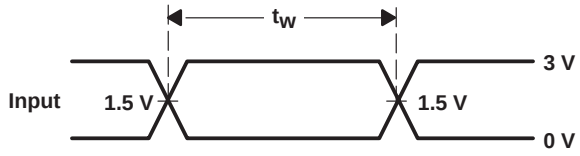
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	Outputs enabled	C_L = 50 pF, f = 1 MHz	61	pF
		Outputs disabled		15	

PARAMETER MEASUREMENT INFORMATION

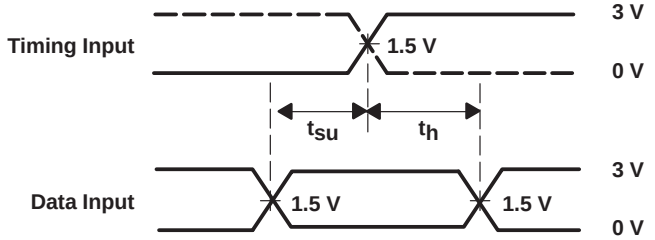


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

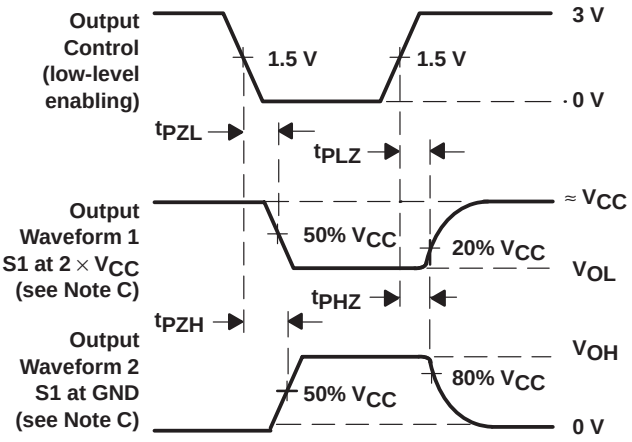
LOAD CIRCUIT FOR OUTPUTS



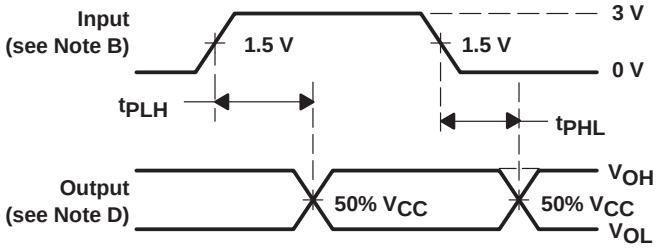
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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