TC74AC160P/F/FN, TC74AC161P/F/FN, TC74AC162P/F/FN, TC74AC163P/F/FN

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER
TC74AC160P/F/FN DECADE, ASYNCHRONOUS CLEAR
TC74AC161P/F/FN BINARY, ASYNCHRONOUS CLEAR
TC74AC162P/F/FN DECADE, SYNCHRONOUS CLEAR
TC74AC163P/F/FN BINARY, SYNCHRONOUS CLEAR

The TC74AC160, 161, 162 and 163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The TC74AC160/162 are BCD decade counters and the TC74AC161/163 are 4 bit binary counters.

The CK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLR}$ inputs are active when low.

Presetting of all four IC's is synchronous to the rising edge of CK.

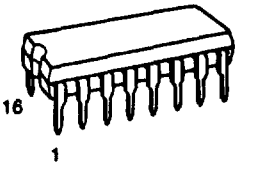
The clear function of the TC74AC162/163 is synchronous to CK, while the TC74AC160/161 are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

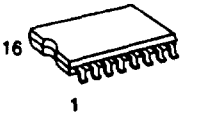
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

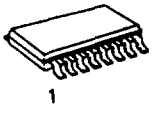
FEATURES:

- High Speed ..... f_{MAX}=170MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 160/161/162/163



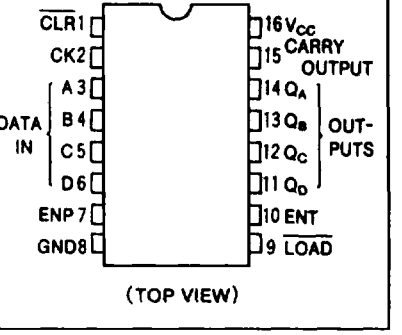
P(DIP16-P-300A)





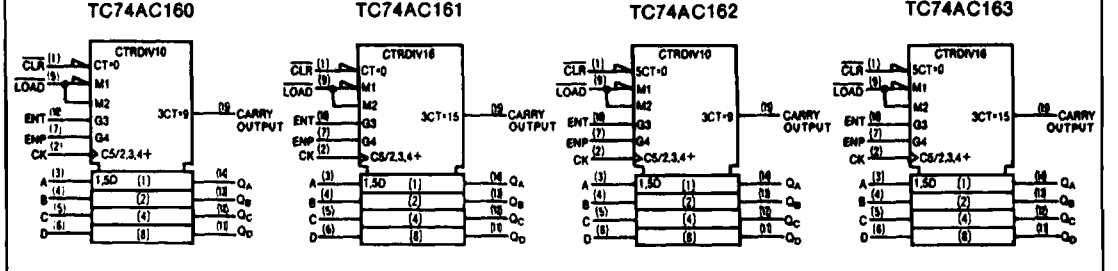
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±125	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TRUTH TABLE

TC74AC160/161 INPUTS					TC74AC162/163 INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	Q_A	Q_B	Q_C	Q_D	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	RESET TO "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	PRESET DATA
H	H	X	L	↑	H	H	X	L	↑	NO CHANGE				NO COUNT
H	H	L	X	↑	H	H	L	X	↑	NO CHANGE				NO COUNT
H	H	H	H	↑	H	H	H	H	↑	COUNT UP				COUNT
H	X	X	X	↓	X	X	X	X	↓	NO CHANGE				NO COUNT

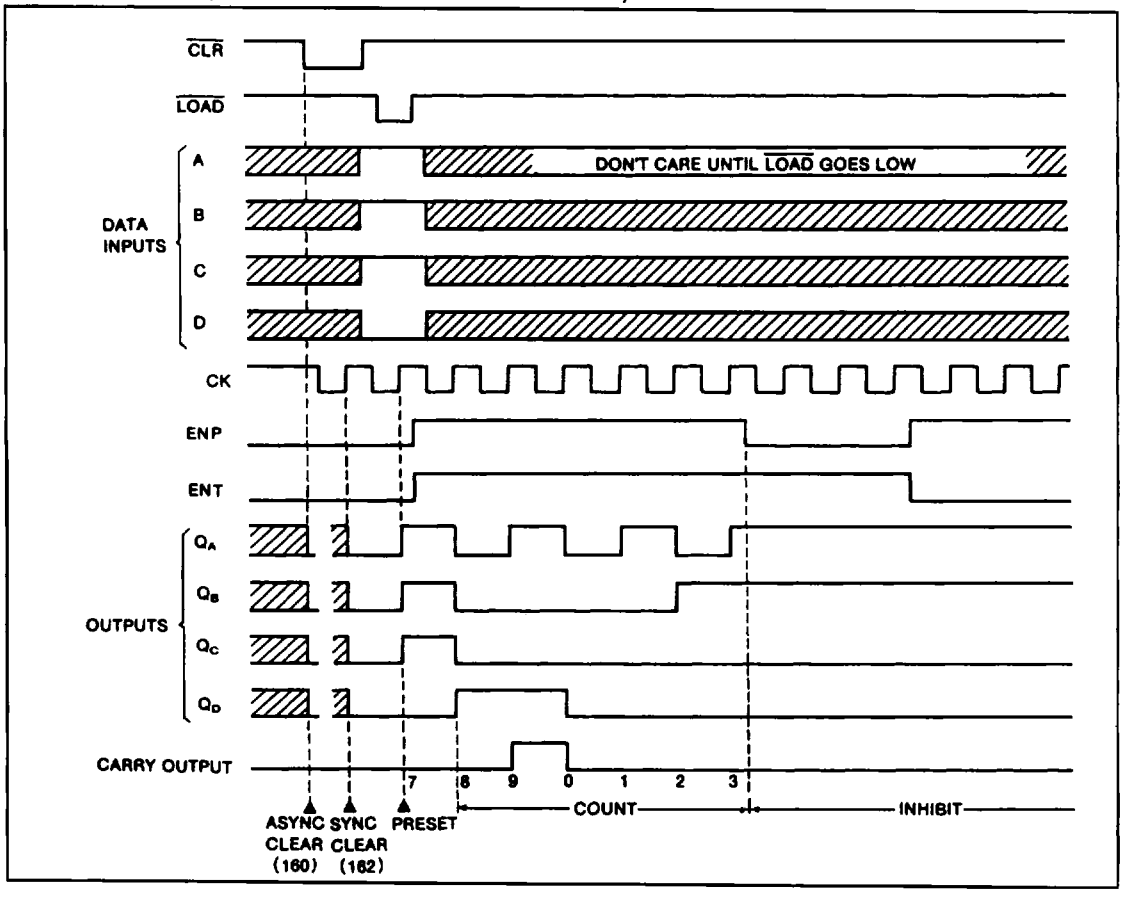
Note X : Don't care

A, B, C, D : Logic Level of Data Inputs

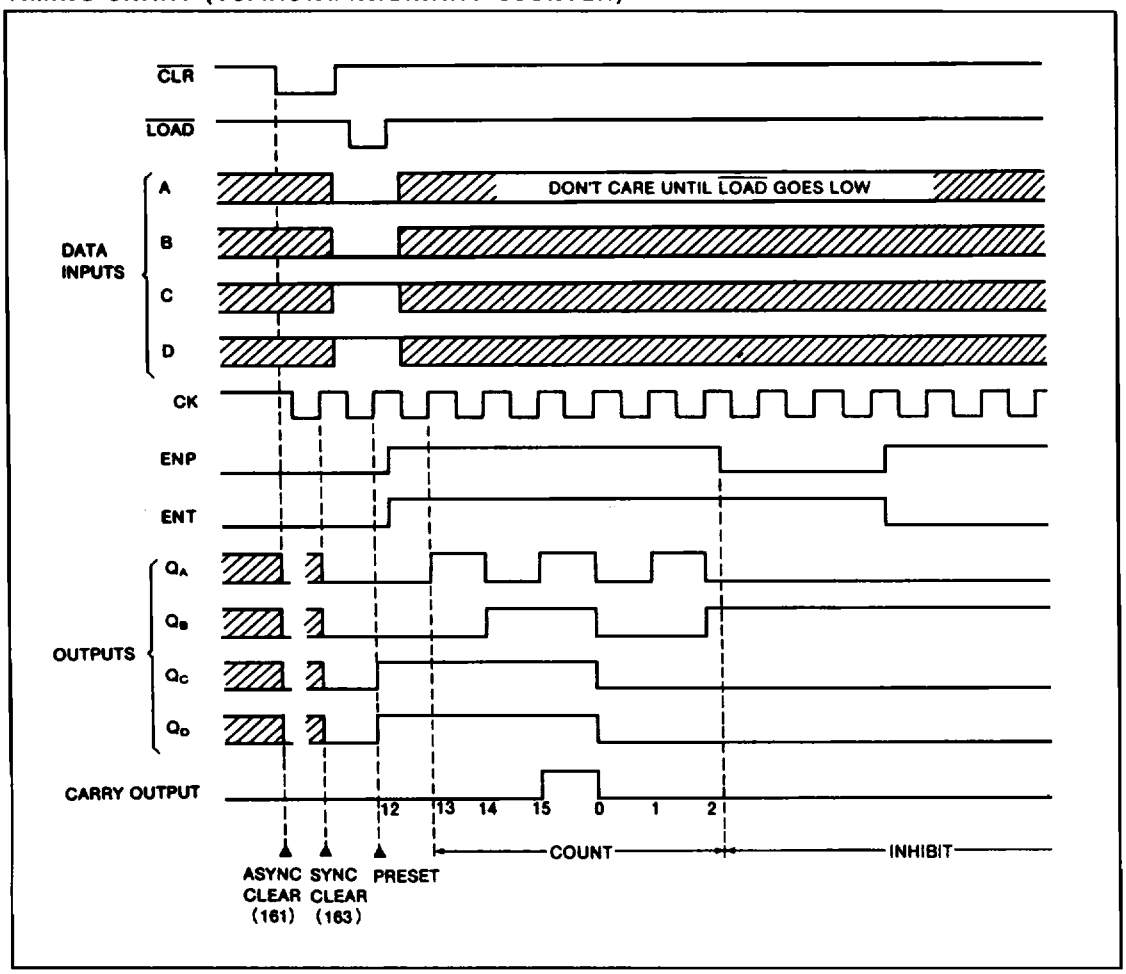
Carry : CARRY = ENT · Q_A · $\overline{Q_B}$ · $\overline{Q_C}$ · Q_D ····· (TC74AC160/162)

CARRY = ENT · Q_A · Q_B · Q_C · Q_D ····· (TC74AC161/163)

TIMING CHART (TC74AC160/162: DECADE COUNTER)

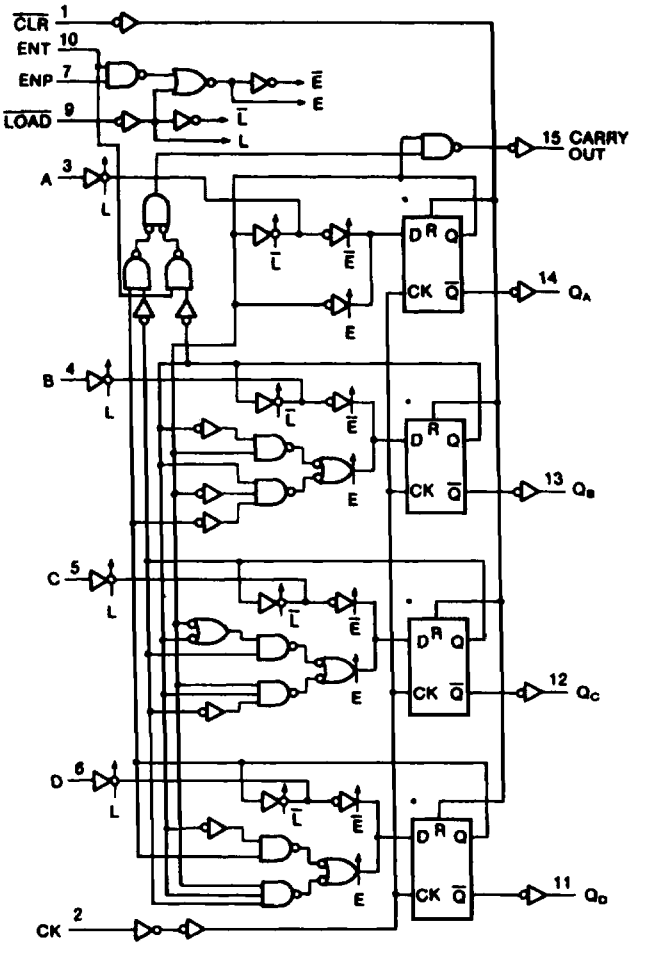


TIMING CHART (TC74AC161/163: BINARY COUNTER)



SYSTEM DIAGRAM

TC74AC160/TC74AC162



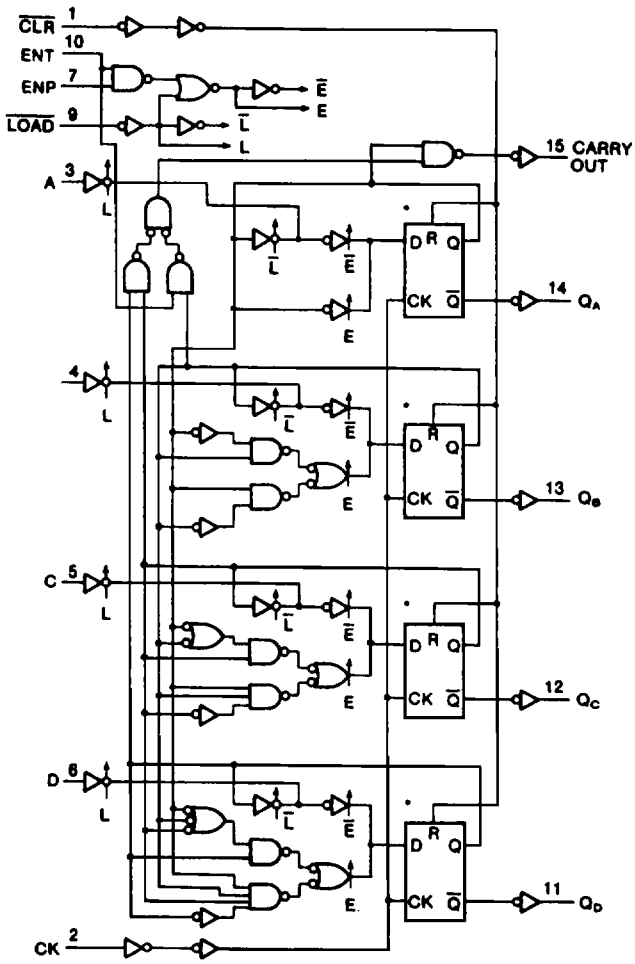
*TRUTH TABLE OF INTERNAL F/F

TC74AC160					TC74AC162				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	H	L	H	X	↓	H	L	H
L	↓	L	L	H	L	↓	L	L	H
H	↓	L	H	L	H	↓	L	H	L
X	↑	L	NO CHANGE		L	↑	L	NO CHANGE	

X : Don't Care

SYSTEM DIAGRAM

TC74AC161/TC74AC163



*TRUTH TABLE OF INTERNAL F/F

TC74AC161					TC74AC163				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	H	L	H	X	↓	H	L	H
L	↓	L	L	H	L	↓	L	L	H
H	↓	L	H	L	H	↓	L	H	L
X	↑	L	NO CHANGE		L	↑	L	NO CHANGE	

X : Don't Care

TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25℃			Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	ns
Minimum Pulse Width ($\overline{CLR}$)•	$t_{W(L)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	
Minimum Set-up Time ($\overline{LOAD}$, ENP, ENT)	t_s		3.3±0.3 5.0±0.5	− −	11.0 7.0	13.0 7.0	
Minimum Set-up Time (A, B, C, D)	t_s		3.3±0.3 5.0±0.5	− −	8.0 4.0	8.0 4.0	
Minimum Set-up Time ($\overline{CLR}$)••	t_s		3.3±0.3 5.0±0.5	− −	6.0 4.0	6.0 4.0	
Minimum Hold Time	t_h		3.3±0.3 5.0±0.5	− −	1.0 1.0	1.0 1.0	
Minimum Removal Time ($\overline{CLR}$)•	t_{rem}		3.3±0.3 5.0±0.5	− −	6.0 4.0	6.0 4.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	8.8 6.5	15.8 9.6	1.0 1.0	18.0 11.0	ns
Propagation Delay Time (CK-CARRY, Count Mode)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	10.4 8.1	18.4 11.8	1.0 1.0	21.0 13.5	
Propagation Delay Time (CK-CARRY, Preset MODE)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	12.9 9.1	22.4 13.2	1.0 1.0	25.5 15.0	
Propagation Delay Time (ENT-CARRY)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	7.5 5.8	13.2 8.3	1.0 1.0	15.0 9.5	
Propagation Delay Time ($\overline{CLR}$-Q)•	t_{pHL}		3.3±0.3 5.0±0.5	− −	10.6 7.7	18.4 11.4	1.0 1.0	21.0 13.0	
Propagation Delay Time ($\overline{CLR}$-CARRY)•	t_{pHL}		3.3±0.3 5.0±0.5	− −	12.0 8.6	21.0 12.7	1.0 1.0	24.0 14.5	
Maximum Clock Frequency	f_{MAX}		3.3±0.3 5.0±0.5	50 90	110 140	− −	50 90	− −	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	85	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and $\triangle I_{CC}$ which is obtained from the following formula:

In case of TC74AC160/162:

$$\triangle I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{5} + \frac{C_{QC}}{10} + \frac{C_{QD}}{10} + \frac{C_{CO}}{10} \right)$$

In case of TC74AC161/163:

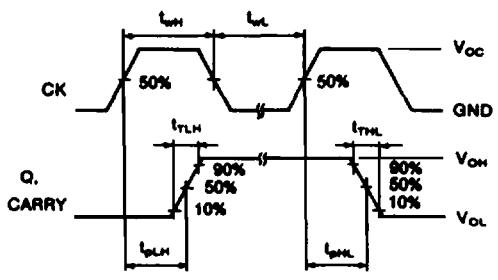
$$\triangle I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

$C_{QA} \sim C_{QD}$ and C_{CO} are the capacitances at QA~QD and CARRY OUT, respectively.
f_{CK} is the input frequency of the CK.

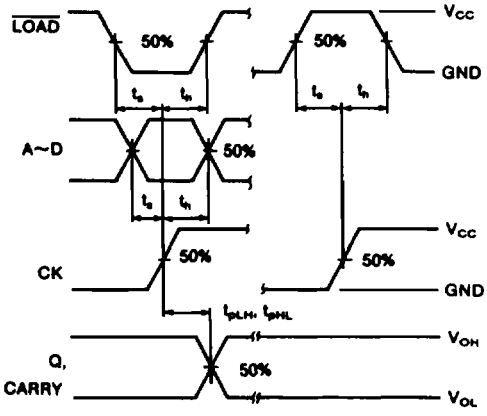
(2) * for TC74AC160/161 only
** for TC74AC162/163 only

SWITCHING CHARACTERISTICS TEST WAVEFORM

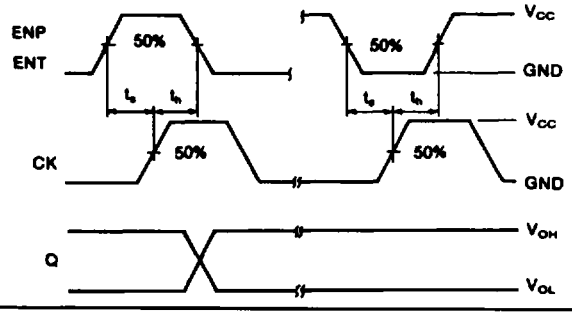
COUNT MODE (Fig. 1)



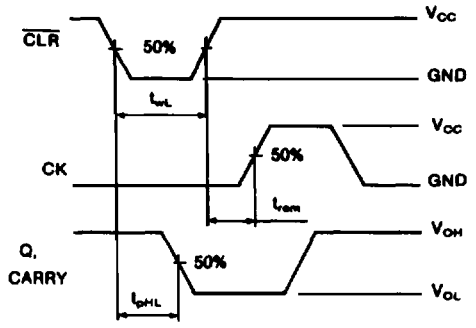
PRESET MODE (Fig. 2)



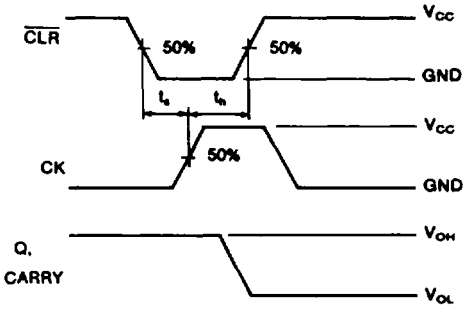
COUNT ENABLE MODE (Fig. 3)



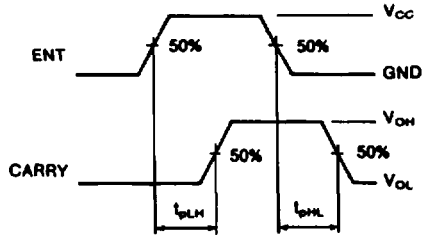
CLEAR MODE (TC74AC160/161) (Fig. 4)



CLEAR MODE (TC74AC162/163) (Fig. 5)



CASCADE MODE (Fig. 6)
(Fix Maximum Count)



TYPICAL APPLICATION

PARALLEL CARRY N-BIT COUNTER