NIPPON PRECISION CIRCUITS INC.

SM8721AB

3-PLL Multi-Output Clock Generator

OVERVIEW

The SM8721AB is a clock generator IC with 3 built-in PLLs. It can simultaneously generate and output 3 clocks with different frequency derived from a single master clock. The generated output clock frequency can be switched using control pins and one clock can be turned ON/OFF (CLK2). The master clock can be selected from a low-cost 14.31818MHz or small 28.636363MHz crystal. The device is available in compact 20-pin QFN packages, making it ideal for portable digital still cameras and other applications which require multiple clocks.

FEATURES

- 3.0 to 3.6V supply voltage
- Crystal oscillator circuit built-in
- 14.318182/28.636363MHz master clock (internal PLL reference clock)
- Generated clocks
  - 14.318182/17.734450MHz (REF_CLK)
  - 71.877274/90.314686/96.016044 /114.54546MHz (CLK1)
  - 48.008022/96.016044MHz (CLK2)
- Low jitter output
  - 30ps typ. (1-sigma)
  - 180ps typ. (peak-to-peak)
- Output load
  - 15pF
- 20-pin QFN package (Pb free)

APPLICATIONS

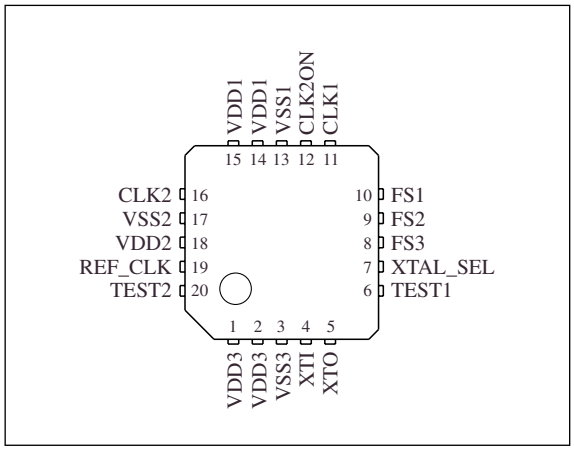
- Digital still cameras

ORDERING INFORMATION

Device	Package
SM8721AB	20-pin QFN

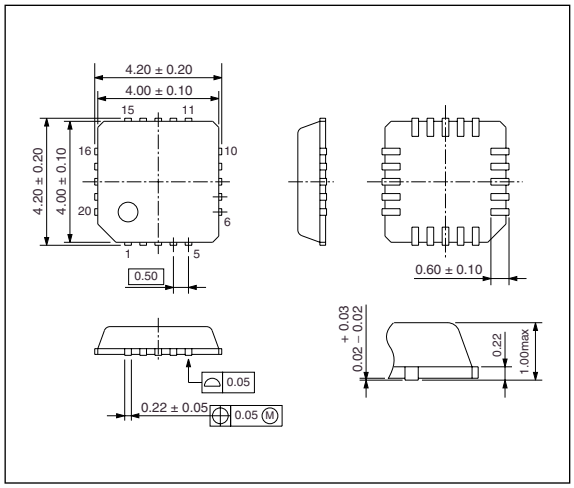
PINOUT

(Top view)

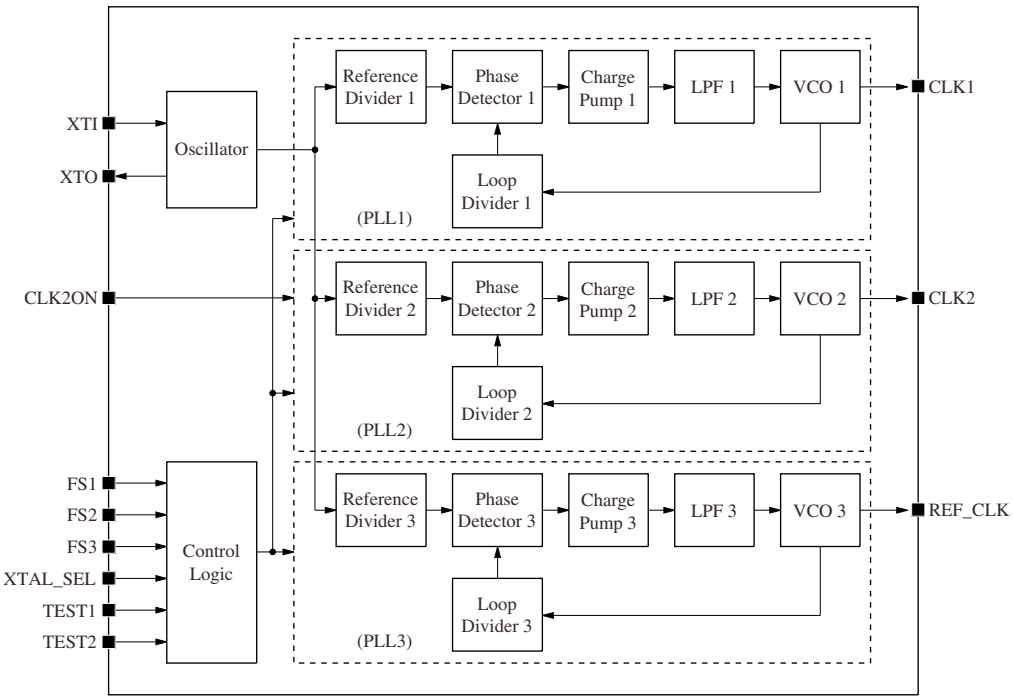


PACKAGE DIMENSIONS

(Unit: mm)
Weight: 0.037g



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	VDD3	–	Analog supply voltage 3
2	VDD3	–	Analog supply voltage 3
3	VSS3	–	Analog supply ground 3
4	XTI	I	Crystal oscillator element connection pin (14.318182/28.636363MHz)
5	XTO	O	Crystal oscillator element connection pin
6	TEST1	I	Test pin 1. Built-in pull-down resistance (leave open circuit or connect to VSS)
7	XTAL_SEL	I	Crystal oscillator element selection pin. Built-in pull-up resistance (HIGH = 28.636MHz, LOW = 14.318MHz)
8	FS3	I	CLK1, CLK2 output select 3. Built-in pull-up resistance
9	FS2	I	CLK1, CLK2 output select 2. Built-in pull-up resistance
10	FS1	I	REF_CLK output select 1. Built-in pull-up resistance
11	CLK1	O	Clock output (71/90/96/114MHz switchable output)
12	CLK2ON	I	CLK2 output enable. Built-in pull-up resistance (HIGH = enable, LOW = disable)
13	VSS1	–	Digital supply ground 1
14	VDD1	–	Digital supply voltage 1
15	VDD1	–	Digital supply voltage 1
16	CLK2	O	Clock output (48/96MHz switchable output)
17	VSS2	–	Digital supply ground 2
18	VDD2	–	Digital supply voltage 2
19	REF_CLK	O	Clock output (14.318/17.734MHz switchable output)
20	TEST2	I	Test pin 2. Built-in pull-down resistance (leave open circuit or connect to VSS)

ABSOLUTE MAXIMUM RATINGS

$V_{DD} = (V_{DD1}, V_{DD2}, V_{DD3})$, $V_{SS} = (V_{SS1}, V_{SS2}, V_{SS3})$ unless otherwise noted.

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD1}, V_{DD2}, V_{DD3}	–0.3 to 6.5	V
Supply voltage deviation	$V_{DD1} - V_{DD2}$, $V_{DD1} - V_{DD3}$, $V_{DD2} - V_{DD3}$	±0.1	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	–0.3 to V_{DD} + 0.3	V
Power dissipation*1	P_D	215	mW
Storage temperature range	T_{STG}	–55 to 125	°C

*1. The power dissipation rating is for a surface-mounted device operating at 85°C.

RECOMMENDED OPERATING CONDITIONS

$V_{SS} = (V_{SS1}, V_{SS2}, V_{SS3}) = 0V$, unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
Supply voltage*1	V_{DD1}, V_{DD2}, V_{DD3}		3.0	–	3.6	V
Output load capacitance	C_L	All outputs excluding XTO	–	–	15	pF
Master clock frequency	f_{XTAL1}	XTAL_SEL = LOW	–	14.318182	–	MHz
	f_{XTAL2}	XTAL_SEL = HIGH	–	28.636363	–	MHz
Operating temperature	T_{OPR}		–40	–	+85	°C

*1. The supply voltages are with reference to V_{SS} = 0V.
It is recommended that the voltages applied to pins VDD1, VDD2, VDD3 be supplied from a single source.
If various voltage sources are used on pins VDD1, VDD2, VDD3, the voltage supplies should be applied simultaneously. If the timing of applying voltage supplies varies, the device may be damaged.

ELECTRICAL CHARACTERISTICS

DC Characteristics

$V_{DD} = (V_{DD1}, V_{DD2}, V_{DD3}) = 3.3 \pm 0.3V$, $V_{SS} = (V_{SS1}, V_{SS2}, V_{SS3}) = 0V$, Ta = –40 to +85°C unless otherwise noted.

Parameter	Symbol	Pins	Conditions	Rating			Unit
				min	typ	max	
Current consumption	I_{DD}	VDD	V_{DD} = 3.3V, Ta = 25°C, all outputs operating without load	–	40	50	mA
Input voltage	V_{IH}	XTAL_SEL, FS1, FS2, FS3, CLK2ON, TEST1, TEST2*1,*2	V_{DD} = 3.3V	$0.8V_{DD}$	–	–	V
	V_{IL}			–	–	$0.2V_{DD}$	V
Input current	I_{IH1}	XTAL_SEL, FS1, FS2, FS3, CLK2ON*1	$V_{IN} = V_{DD}$	–	–	1	µA
	I_{IL1}		V_{IN} = 0V	–100	–	–	µA
	I_{IH2}	TEST1, TEST2*2	$V_{IN} = V_{DD}$	–	–	100	µA
	I_{IL2}		V_{IN} = 0V	–1	–	–	µA
	I_{IH3}	XTI	$V_{IN} = V_{DD}$	–	–	40	µA
	I_{IL3}		V_{IN} = 0V	–40	–	–	µA
Output voltage	V_{OH}	CLK1, CLK2, REF_CLK	I_{OH} = –2mA	V_{DD} – 0.4	–	–	V
	V_{OL}		I_{OL} = 2mA	–	–	0.4	V

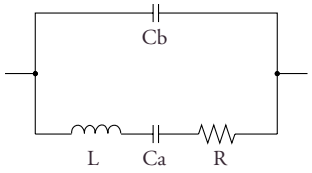
*1. XTAL_SEL, FS1, FS2, FS3, CLK2ON pins have Schmitt-trigger inputs with internal pull-up resistance.
*2. TEST1, TEST2 pins have Schmitt-trigger inputs with internal pull-down resistance.

AC Characteristics

$V_{DD} = (V_{DD1}, V_{DD2}, V_{DD3}) = 3.3 \pm 0.3V$, $V_{SS} = (V_{SS1}, V_{SS2}, V_{SS3}) = 0V$, Ta = –40 to +85°C unless otherwise noted.

Parameter	Symbol	Pins	Conditions	Rating			Unit
				min	typ	max	
Output clock rise time*1	t_r	CLK1, CLK2, REF_CLK	C_L = 15pF, $V_{OL} = 0.2V_{DD}$ to $V_{OH} = 0.8V_{DD}$ transition	–	2.0	–	ns
Output clock fall time*1	t_f	CLK1, CLK2, REF_CLK	C_L = 15pF, $V_{OH} = 0.8V_{DD}$ to $V_{OL} = 0.2V_{DD}$ transition	–	2.0	–	ns
Output clock jitter*2,*3	t_{jitter} (1-sigma)	CLK1, CLK2, REF_CLK	Ta = 25°C, C_L = 15pF, $V_O = 0.5V_{DD}$	–	30	–	ps
	t_{jitter} (peak-peak)	CLK1, CLK2, REF_CLK	Ta = 25°C, C_L = 15pF, $V_O = 0.5V_{DD}$	–	180	–	ps
Output clock duty cycle*1, *3	Dt1	CLK1, CLK2, REF_CLK	Ta = 25°C, C_L = 15pF, $V_O = 0.5V_{DD}$	45	50	55	%
	Dt2	CLK1	Ta = 25°C, C_L = 15pF, $V_O = 0.5V_{DD}$, 114.54546MHz	40	50	60	%
Power-up time*3,*4,*5	t_P	CLK1, CLK2, REF_CLK		–	1	5	ms

*1. Measured using the circuit shown in figure 1 on the NPC standard evaluation board.
*2. Measured using the circuit shown in figure 2 on the NPC standard evaluation board.
*3. The crystal oscillator element coefficients for characteristics measurements are described below (HP4195 measurement equipment).
f = 14.318182MHz crystal: R = 12.16Ω, L = 10.34mH, Ca = 11.95fF, Cb = 4.03pF
f = 28.636363MHz crystal: R = 12.50Ω, L = 5.89mH, Ca = 5.25fF, Cb = 1.65pF



*4. The power-up time is the time from when the supply reaches 3.0V after the supply is turned ON until each output clock reaches its designated frequency to within ±0.1%.
*5. Measured using the NPC standard evaluation board.

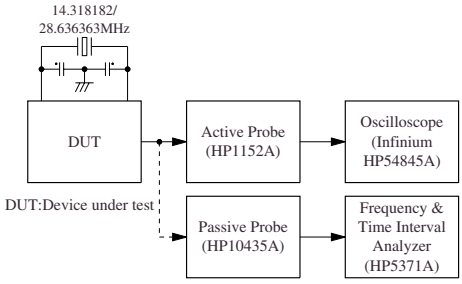


Figure 1. Measurement circuit 1

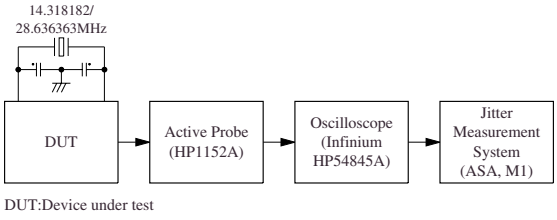


Figure 2. Measurement circuit 2

FUNCTIONAL DESCRIPTION

14.318182/28.636363MHz Master Clock

The 14.318182/28.636363MHz master clock is generated by the crystal oscillator formed by connecting a crystal (14.318182/28.636363MHz fundamental frequency) between pins XTI (pin 4) and XTO (pin 5), as shown in figure 3.

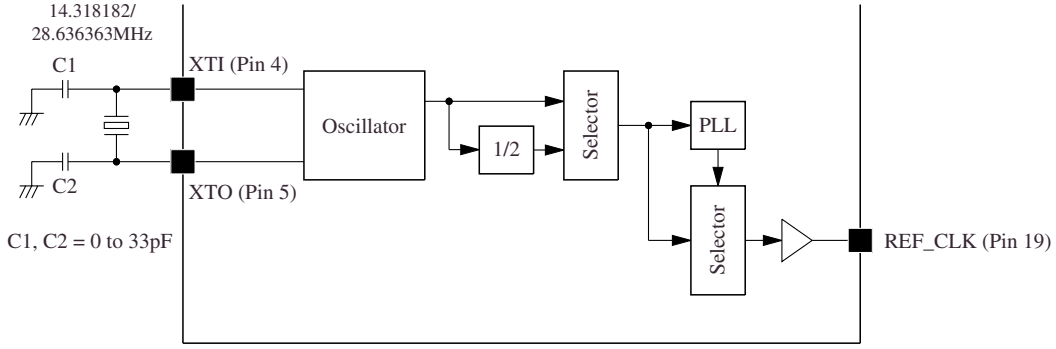


Figure 3. Crystal oscillator connection

Output Clock Frequency

The SM8721AB generates 3 output clocks with frequency 14.318182/17.734450MHz (REF_CLK), 71.877274/90.314686/96.016044/114.54546MHz (CLK1), and 48.008022/96.016044MHz (CLK2), derived from the master clock.

A list of the supported clock frequency and control settings is shown in table 1.

Table 1. Output clock frequency
14.318182MHz master clock frequency: XTAL_SEL = LOW
28.636363MHz master clock frequency: XTAL_SEL = HIGH

FS1 (Pin 10)	FS2 (Pin 9)	FS3 (pin 8)	CLK2ON (pin 12)	Output clock frequency [MHz]		
				REF_CLK (Pin 19)	CLK1 (Pin 11)	CLK2 (Pin 16)
HIGH	HIGH	HIGH	HIGH	14.318182	96.016044	48.008022
LOW				17.734450		
HIGH	LOW			14.318182	90.314686	
LOW				17.734450		
HIGH	HIGH	LOW		14.318182	71.877274	
LOW				17.734450		
HIGH	LOW			14.318182	114.54546	96.016044
LOW				17.734450		
HIGH	HIGH	HIGH	LOW	14.318182	96.016044	Fixed LOW
LOW				17.734450		
HIGH	LOW			14.318182	90.314686	
LOW				17.734450		
HIGH	HIGH	LOW		14.318182	71.877274	
LOW				17.734450		
HIGH	LOW			14.318182	114.54546	
LOW				17.734450		

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