

FEATURES

- Very Low Total Harmonic Distortion
- Lower Glitch Energy
- Four Quadrant Multiplication
- On-Chip Latches for Both DACs
- +10.8 V to +15.75 V Operation
- Low Power Consumption
- TTL/5V CMOS Compatible
- Latch-Up Free
- Second Source to AD7628
- 5 V Operation: MP7529B

BENEFITS

- Quiet Operation in Audio Applications
- Easy Interface to Microprocessors

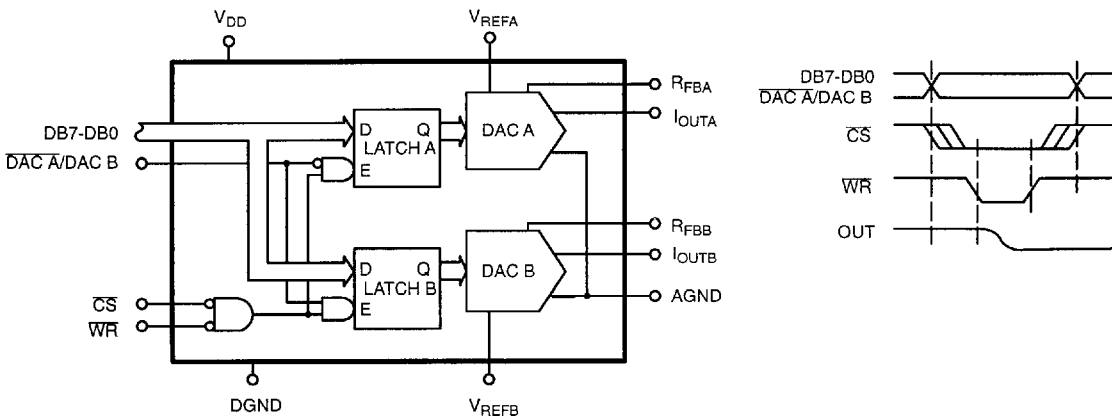
GENERAL DESCRIPTION

The MP7529A is a dual 8-bit Digital-to-Analog Converter featuring excellent DAC-to-DAC matching, tracking and specifically optimized for applications requiring low total harmonic distortion. The MP7529A is manufactured using advanced thin film resistors on a double metal CMOS process. The MP7529A incorporates a unique decoding technique yielding lower glitch energy, higher speed and excellent accuracy over temperature and time.

Data is transferred to either of the two D/A Converter latches via a common 8-bit TTL/5 V CMOS compatible input port. The control input $\overline{\text{DAC A/DAC B}}$ determines which DAC is to be loaded.

The device is specified for operation from +10.8 V to +15.75 V power supply, and is TTL-compatible over this range. Power dissipation is only 20 mW. Both DACs offer excellent four quadrant multiplication characteristics, and include separate reference inputs and feedback resistors. An improved latch-up resistant design eliminates the need for external protective Schottky diodes in most applications.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

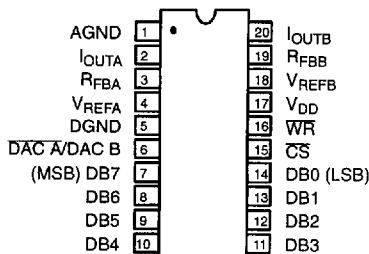


ORDERING INFORMATION

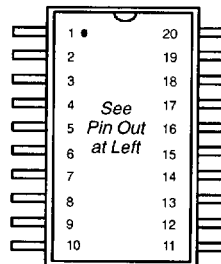
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	-40 to +85°C	MP7529AJN	±1	±1	±5
Plastic Dip	-40 to +85°C	MP7529AKN	±1/2	±1	±3
SOIC	-40 to +85°C	MP7529AJS	±1	±1	±5
SOIC	-40 to +85°C	MP7529AKS	±1/2	±1	±3
PLCC	-40 to +85°C	MP7529AJP	±1	±1	±5
PLCC	-40 to +85°C	MP7529AKP	±1/2	±1	±3

PIN CONFIGURATIONS

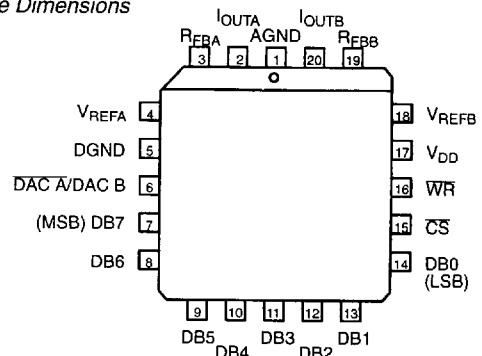
See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300")
S20



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	AGND	Analog Ground
2	I _{OUTA}	Current Output of DAC A
3	R _{FBA}	Internal Feedback Resistor of DAC A
4	V _{REFA}	Reference Input Voltage of DAC A
5	DGND	Digital Ground
6	DAC A/DAC B	DAC selection control
7	DB7	Data Input Input Bit 7 (MSB)
8	DB6	Data Input Bit 6
9	DB5	Data Input Bit 5
10	DB4	Data Input Bit 4

PIN NO.	NAME	DESCRIPTION
11	DB3	Data Input Bit 3
12	DB2	Data Input Bit 2
13	DB1	Data Input Bit 1
14	DB0	Data Input Bit 0 (LSB)
15	CS	Chip Select (Active Low)
16	WR	Write Enable (Active Low)
17	V _{DD}	Power Supply
18	V _{REFB}	Reference Input Voltage of DAC B
19	R _{FBB}	Internal Feedback Resistor of DAC B
20	I _{OUTB}	Current Output of DAC B

ELECTRICAL CHARACTERISTICS

($V_{DD} = +10.8\text{ V}$ to $+15.75\text{ V}$, $V_{REF} = +10\text{ V}$ unless otherwise noted)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
STATIC PERFORMANCE¹								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec.
J				±1		±1		
K				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J				±1		±1		
K				±1		±1		
Gain Error	GE						LSB	Using Internal R _{FB}
J				±4		±5		
K				±2		±3		
Gain Temperature Coefficient ²	TC _{GE}	±15				±35	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±100		±200	ppm/%	ΔGain/ΔV _{DD} , ΔV _{DD} = ± 5% V _{DD} = 10.8 V, ±5%, & 15.75 V ±5%
Output Leakage Current	I _{LKG}			±50		±200	nA	
DYNAMIC PERFORMANCE²								
Harmonic Distortion	THD		-95				dB	V _{IN} = 6V _{RMS} @ 1 kHz
Digital Crosstalk	Q		30				nVs	
AC Feedthrough	F _T						dB	
V _{REFA} to I _{OUTA}	F _{TA}		-70			-65	dB	
V _{REFB} to I _{OUTB}	F _{TB}		-70			-65	dB	
Channel-to-Channel Isolation	CCI						dB	
V _{REFA} to I _{OUTB}	C _{CIAB}		-77				dB	
V _{REFB} to I _{OUTA}	C _{CIAB}		-77				dB	
Glitch Energy	E _{gl}		10				nVs	All zeros to all ones Input Change
Current Settling Time	t _S		200			250	ns	To 1/2 LSB, R _L =100Ω, C _{EXT} =13pF
Propagation Delay	t _{PD}		100			150	ns	From 50% of digital input to 90% of final analog output current R _L =100Ω, C _{EXT} =13pF
REFERENCE INPUT¹								
Input Resistance	R _{IN}	8		15	8	15	kΩ	
Input Resistance Matching				±1		±1	%	
DIGITAL INPUTS³								
Logical "1" Voltage	V _{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V _{IL}			0.8		0.8	V	
Input Leakage Current	I _{LKG}			±1		±10	μA	
Input Capacitance ²								
Data	C _{IN}			10		10	pF	
Control	C _{IN}			15		15	pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C		Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min		
ANALOG OUTPUTS²							
Output Capacitance	C _{OUTA/B} C _{OUTA/B}			120		pF	DAC inputs all 1's DAC inputs all 0's
				50		50	
POWER SUPPLY¹							
Supply Current	I _{DD}			1 2		mA mA	All digital inputs = 0 V, or all = 5 V All digital inputs = V _{IL} , or all = V _{IH}
TIMING SPECIFICATIONS⁴							
Chip Select to Write Set-Up Time	t _{CS}	60			80	ns	
Chip Select to Write Hold Time	t _{CH}	15			20	ns	
DAC Select to Write Set-Up Time	t _{AS}	60			80	ns	
DAC Select to Write Hold Time	t _{AH}	15			20	ns	
Data Valid to Write Set-Up Time	t _{DS}	60			80	ns	
Data Valid to Write Hold Time	t _{DH}	0			0	ns	
Write Pulse Width ⁵	t _{WR}	60			80	ns	

NOTES:

- 1 Full Scale Range (FSR) is 10V for unipolar mode.
- 2 Guaranteed but not production tested.
- 3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- 4 See timing diagram *Figure 1*.
- 5 t_{WR} = 40ns minimum if t_{DH} > 15ns (@T = 25°C).

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)^{1, 2, 3}

V _{DD} to GND	GND -0.5 to +17 V	V _{RFBA} , V _{RFBB} to GND	±25 V
AGND to DGND	±1 V	Storage Temperature	-65°C to +150°C
(Functionality Guaranteed ±0.5 V)		Lead Temperature (Soldering, 10 seconds)	+300°C
Digital Input Voltage to GND	GND -0.5 V to +7 V	Package Power Dissipation Rating to 75°C	
I _{OUTA} , I _{OUTB} to GND	GND -0.5 V to +7 V	PDIP, SOIC, PLCC	900mW
V _{REFA} , V _{REFB} to GND	±25 V	Derates above 75°C	12mW/°C

NOTES:

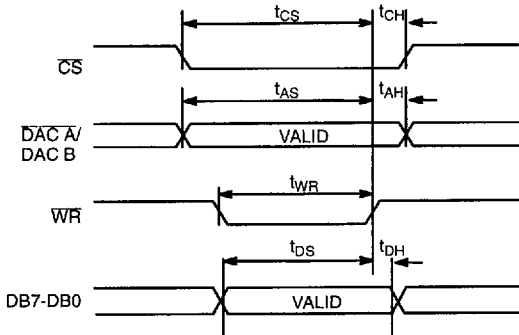
- 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
- 3 GND refers to AGND and DGND.

DIGITAL INTERFACE

The digital inputs are designed to be both TTL and 5 V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 10nA.

The control input $\overline{\text{DAC A/DAC B}}$ selects which DAC can accept data from the input port. Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC (Table 1.). When $\overline{\text{CS}}$ and $\overline{\text{WR}}$

are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0-DB7 (Write mode). The selected DAC latch retains the data which was present on DB0-DB7 just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches (Hold mode).



NOTE:

1. Timing measured from $(V_{\text{IH}} + V_{\text{IL}}) / 2$

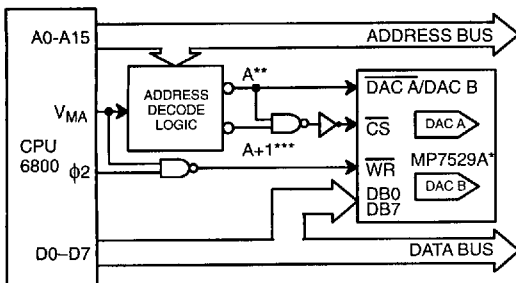
DAC A/ DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Figure 1. Write Cycle Timing Diagram

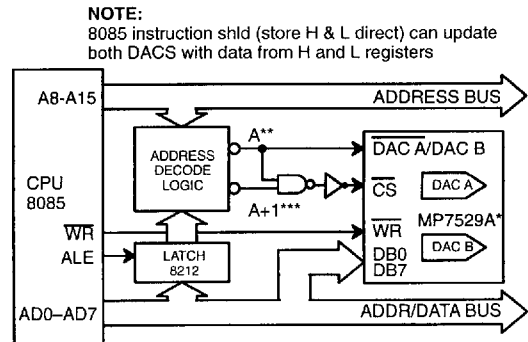
Table 1. DACs Mode Selection

MICROPROCESSOR INTERFACE



*Analog circuitry has been omitted for clarity
 **A = Decoded 7529A DAC A Address
 ***A+1 = Decoded 7529A DAC B Address

Figure 2. MP7529A Dual DAC to 6800 CPU Interface

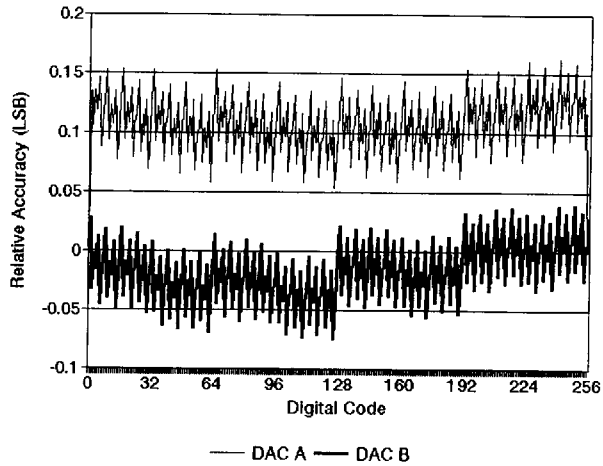


NOTE:
 8085 instruction shld (store H & L direct) can update both DACs with data from H and L registers

*Analog circuitry has been omitted for clarity
 **A = Decoded 7529A DAC A Address
 ***A+1 = Decoded 7529A DAC B Address

Figure 3. MP7529A Dual DAC to 8085 CPU Interface

PERFORMANCE CHARACTERISTICS



Graph 1. Relative Accuracy vs. Digital Code

APPLICATION NOTES

Refer to Section 8 for Applications Information