LOW SKEW, 1-TO-4 LVCMOS-TO-3.3V LVPECL FANOUT BUFFER

IDT8535-01
NRND

NOT RECOMMENDED FOR NEW DESIGNS

FEATURES:

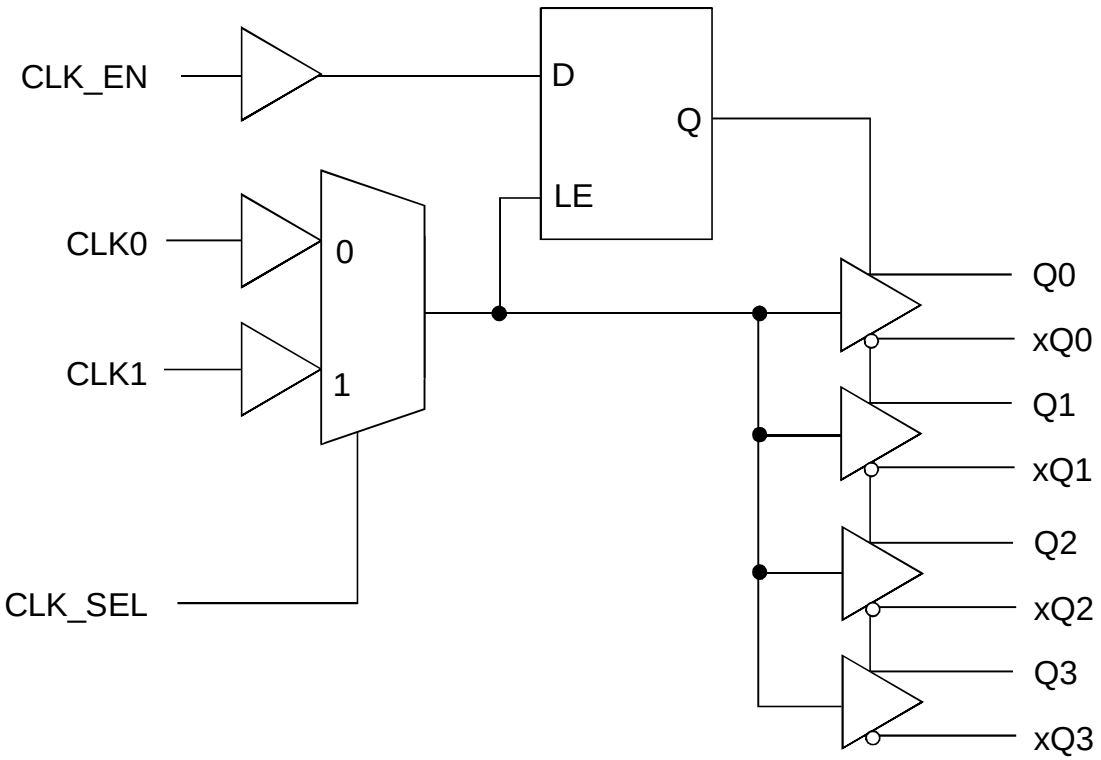
- **Four differential 3.3V LVPECL outputs**
- **Selectable CLK0 or CLK1 inputs for redundant and multiple frequency fanout applications**
- **Maximum output frequency: 266MHz**
- **CLK0 or CLK1 can accept LVCMOS or LVTTL input levels**
- **Translates LVCMOS and LVTTL levels to 3.3V LVPECL levels**
- **Output skew: 30ps (max.)**
- **Part-to-part skew: as low as 150ps**
- **Propagation delay: 1.9ns (max.)**
- **3.3V operating supply**
- **Available in TSSOP package**
- **Not Recommended For New Designs**

DESCRIPTION:

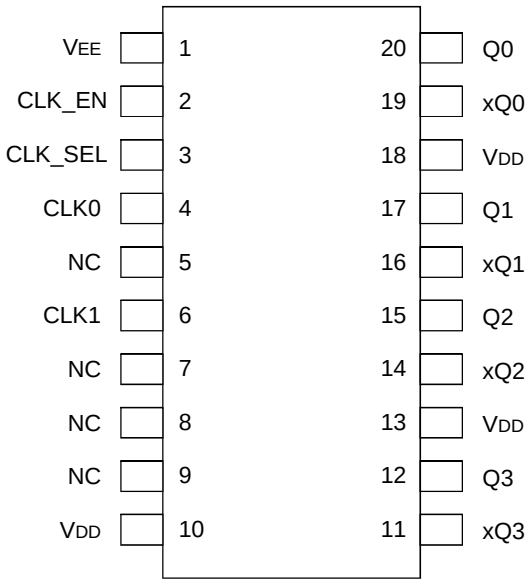
The IDT8535-01 is a low skew, high performance 1-to-4 LVCMOS-to-3.3V LVPECL fanout buffer. It has two single-ended clock inputs. The single-ended clock input accepts LVCMOS or LVTTL input levels and translates them to 3.3V LVPECL levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the IDT8535-01 ideal for those applications demanding well-defined performance and repeatability.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{DD}	Power Supply Voltage	4.6	V
V_I	Input Voltage	–0.5 to V_{DD}+0.5	V
V_O	Output Voltage	–0.5 to V_{DD}+0.5	V
θ_{JA}	Package Thermal Impedance (0 lfpm)	92.6	°C/W
T_{STG}	Storage Temperature	–65 to +150	°C

NOTE:
1. Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Typ.	Max.	Unit
C_{IN}	Input Capacitance	—	4	pF
R_{PULLUP}	Input Pullup Resistor	51	—	KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor	51	—	KΩ

PIN DESCRIPTION(1)

Symbol	Number	Type		Description
V_{EE}	1	Power		Negative Supply Pin
CLK_EN	2	Input	Pullup	Synchronizing Clock Enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced LOW, xQ outputs are forced HIGH. LVCMOS / LVTTL interface levels.
CLK_SEL	3	Input	Pulldown	Clock Select Input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
CLK0	4	Input	Pulldown	LVCMOS / LVTTL Clock Input
CLK1	6	Input	Pulldown	LVCMOS / LVTTL Clock Input
NC	5, 7, 8, 9	Unused		No Connection
V_{DD}	10, 13, 18	Power		Positive Supply Pins
xQ3, Q3	11, 12	Output		Differential Output Pair. LVPECL interface levels.
xQ2 Q2	14, 15	Output		Differential Output Pair. LVPECL interface levels.
xQ1, Q1	16, 17	Output		Differential Output Pair. LVPECL interface levels.
xQ0, Q0	19, 20	Output		Differential Output Pair. LVPECL interface levels.

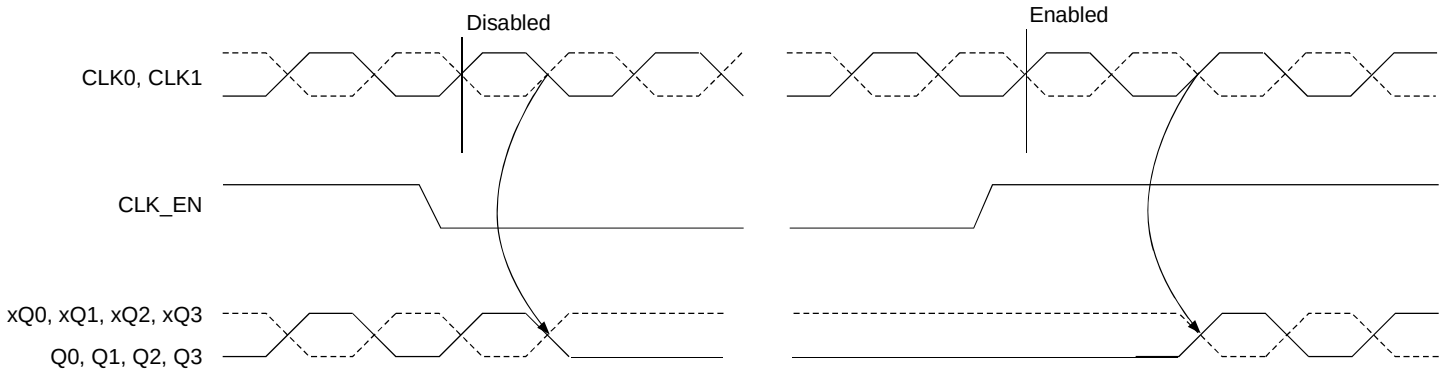
NOTE:
1. Pullup and Pulldown refer to internal input resistors. See Capacitance table for typical values.

CONTROL INPUT FUNCTION TABLE(1,2)

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0 to Q3**	**xQ0 to xQ3**
0	0	CLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

NOTES:

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in the CLK_EN Timing Diagram below.
2. In active mode, the state of the outputs is a function of the CLK / xCLK and PCLK / xPCLK inputs as described in the Clock Input Function table.



CLK_EN Timing Diagram

CLOCK INPUT FUNCTION TABLE(1)

Inputs	Outputs	
CLK0 or CLK1	**Q0 to Q3**	**xQ0 to xQ3**
0	L	H
1	H	L

NOTE:

1. H = HIGH
   L = LOW

POWER SUPPLY CHARACTERISTICS - COMMERCIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current		—	—	50	mA

DC ELECTRICAL CHARACTERISTICS, LVCMOS / LVTTL - COMMERCIAL

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input Voltage HIGH			2		V_{DD} + 0.3	V
V_{IL}	Input Voltage LOW	CLK0, CLK1		-0.3		1.3	V
		CLK_EN, CLK_SEL		-0.3		0.8	
I_{IH}	Input Current HIGH	CLK0, CLK1, CLK_SEL	V_{IN} = V_{DD} = 3.465V			150	µA
		CLK_EN	V_{IN} = V_{DD} = 3.465V			5	
I_{IL}	Input Current LOW	CLK0, CLK1, CLK_SEL	V_{IN} = 0V, V_{DD} = 3.465V	-5			µA
		CLK_EN	V_{IN} = 0V, V_{DD} = 3.465V	-150			

DC ELECTRICAL CHARACTERISTICS, LVPECL - COMMERCIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output Voltage HIGH[1]		V_{DD} - 1.4		V_{DD} - 1	V
V_{OL}	Output Voltage LOW[1]		V_{DD} - 2		V_{DD} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE:

1. Outputs terminated with 50Ω to V_{DD} - 2V.

AC ELECTRICAL CHARACTERISTICS - COMMERCIAL

All parameters measured at 266MHz unless noted otherwise;
Cycle-to-cycle jitter on input = jitter on output; the part does not add jitter

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay[1]	f ≤ 266MHz	1		1.9	ns
$t_{SK(O)}$	Output Skew[2,4]			11	30	ps
$t_{SK(PP)}$	Part-to-Part Skew[3,4]				150	ps
t_R	Output Rise Time	20 - 80% @ 50MHz	300		700	ps
t_F	Output Fall Time	20 - 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48	50	52	%

NOTES:

1. Measured from the V_{DD}/2 of the input to the differential output crossingpoint.
2. Defined as skew between outputs as the same supply voltage and with equal load conditions. Measured at the output differential crosspoints
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
4. This parameter is defined in accordance with JEDEC Standard 65.

POWER SUPPLY CHARACTERISTICS - INDUSTRIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current		—	—	55	mA

DC ELECTRICAL CHARACTERISTICS, LVCMOS / LVTTL - INDUSTRIAL

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input Voltage HIGH			2		V_{DD} + 0.3	V
V_{IL}	Input Voltage LOW	CLK0, CLK1		-0.3		1.3	V
		CLK_EN, CLK_SEL		-0.3		0.8	
I_{IH}	Input Current HIGH	CLK0, CLK1, CLK_SEL	V_{IN} = V_{DD} = 3.465V			150	µA
		CLK_EN	V_{IN} = V_{DD} = 3.465V			5	
I_{IL}	Input Current LOW	CLK0, CLK1, CLK_SEL	V_{IN} = 0V, V_{DD} = 3.465V	-5			µA
		CLK_EN	V_{IN} = 0V, V_{DD} = 3.465V	-150			

DC ELECTRICAL CHARACTERISTICS, LVPECL - INDUSTRIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output Voltage HIGH[1]		V_{DD} - 1.4		V_{DD} - 1	V
V_{OL}	Output Voltage LOW[1]		V_{DD} - 2		V_{DD} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE:

1. Outputs terminated with 50Ω to V_{DD} - 2V.

AC ELECTRICAL CHARACTERISTICS - INDUSTRIAL

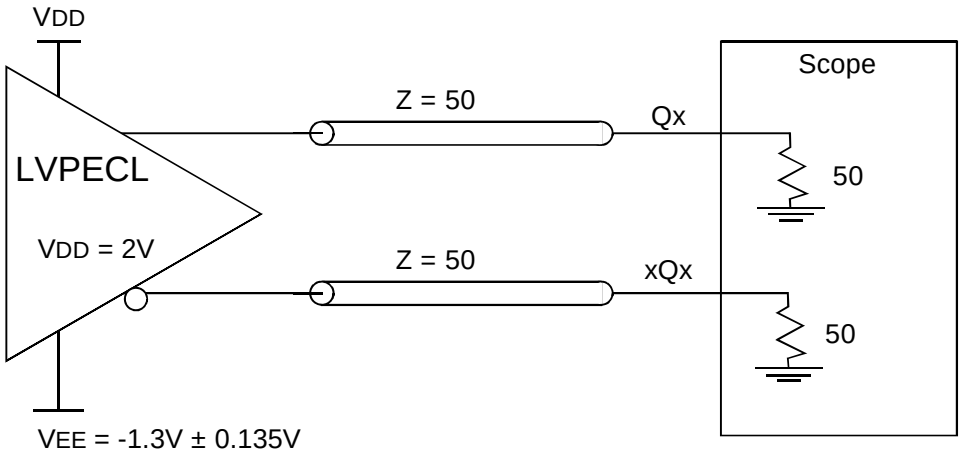
All parameters measured at 266MHz unless noted otherwise;
Cycle-to-cycle jitter on input = jitter on output; the part does not add jitter

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay[1]	f ≤ 266MHz	1		1.9	ns
$t_{SK(O)}$	Output Skew[2,4]				30	ps
$t_{SK(PP)}$	Part-to-Part Skew[3,4]				200	ps
t_R	Output Rise Time	20 - 80% @ 50MHz	300		700	ps
t_F	Output Fall Time	20 - 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48	50	52	%

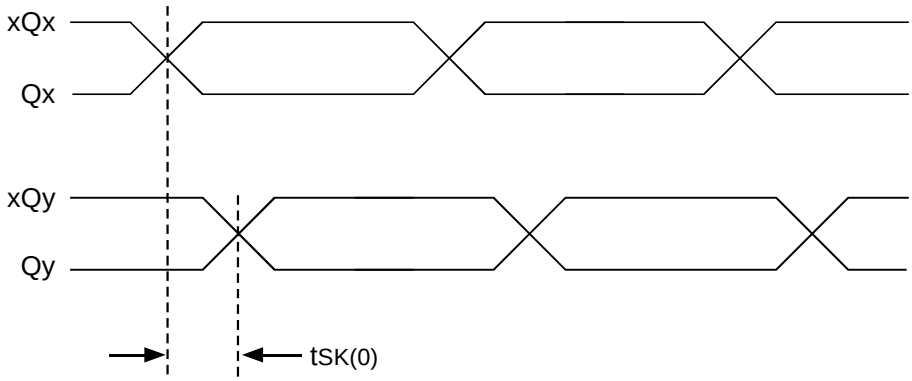
NOTES:

1. Measured from the V_{DD}/2 of the input to the differential output crossingpoint.
2. Defined as skew between outputs as the same supply voltage and with equal load conditions. Measured at the output differential crosspoints
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
4. This parameter is defined in accordance with JEDEC Standard 65.

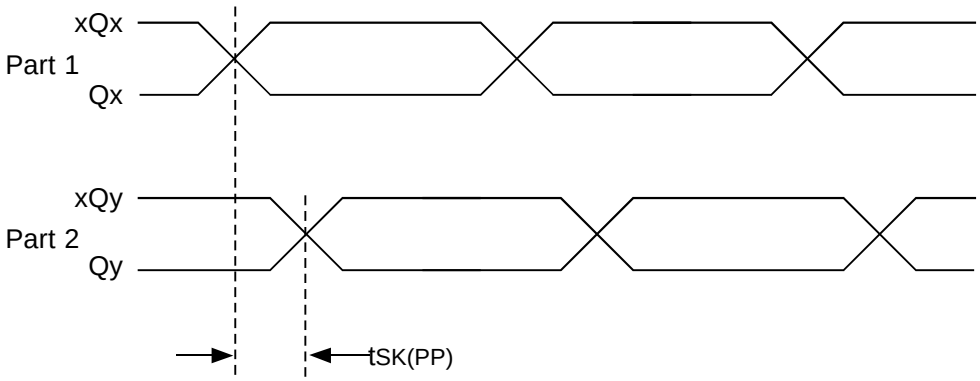
PARAMETER MEASUREMENT INFORMATION



Output Load Test Circuit

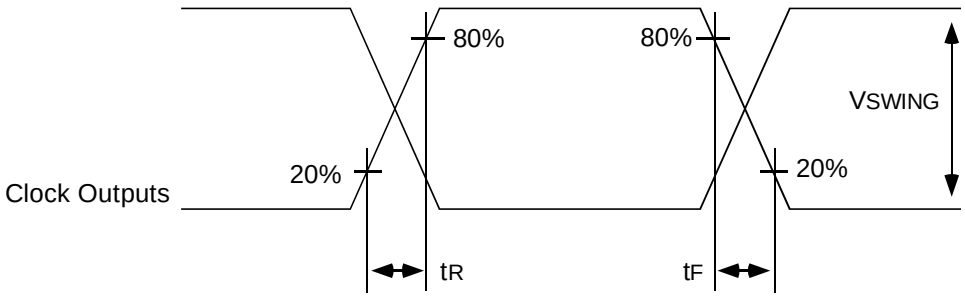


Output Skew

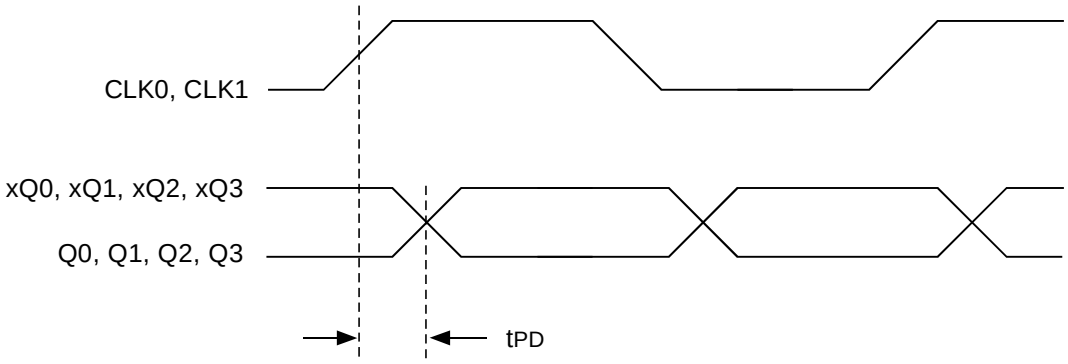


Part-to-Part Skew

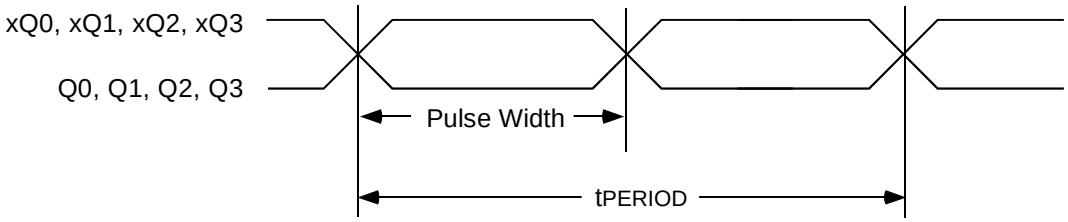
PARAMETER MEASUREMENT INFORMATION - CONTINUED



Output Rise and Fall Time



Propagation Delay



$$odc = \frac{tW}{tPERIOD}$$

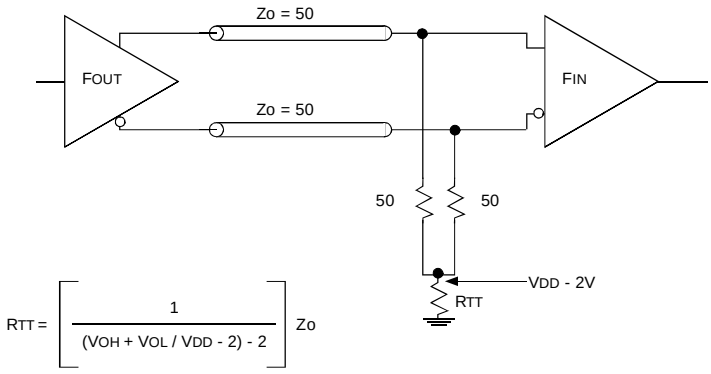
odc and t_{PERIOD}

APPLICATION INFORMATION

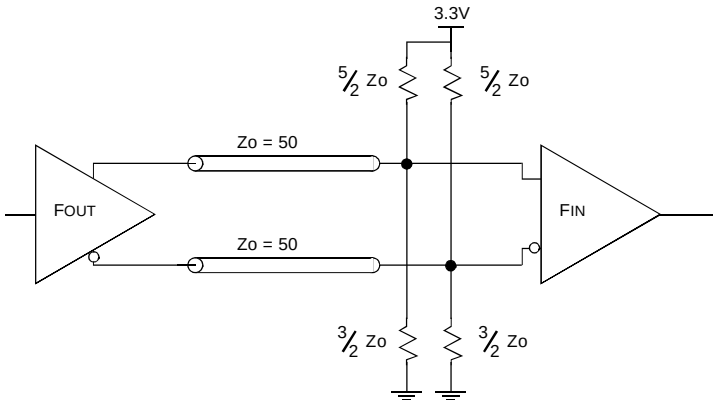
TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and xFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. The diagrams below show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist. It is recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



LVPECL Output Termination, layout A



LVPECL Output Termination, layout B

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the IDT8535-01. Equations and example calculations are also provided.

POWER DISSIPATION:

The total power dissipation for the IDT8535-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for the V_{DD} = 3.3V + 5% = 3.465V and Industrial Temperature grade, which gives worst case results. Please refer to the following section, **Calculations and Equations**, for details on calculating power dissipated in the load.

Power (core)$_{MAX}$ = V_{DD_MAX} * I_{CC_MAX} = 3.465 * 55mA = 190.57mW
Power (outputs)$_{MAX}$ = 30.2mW/Loaded Output Pair
If all outputs are loaded, the total power is 4 * 30.2mW = 120.8mW

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 190.57mW + 120.8mW = 311.37mW

JUNCTION TEMPERATURE:

Junction temperature (t_J) is the temperature at the junction of the bond wire and bond pad. It directly affects the reliability of the device. The maximum recommended junction temperature for this device is 125°C.

The equation for is as follows: $t_J = \theta_{JA} * Pd\_total + T_A$
t_J = Junction Temperature
θ_{JA} = Junction-to-Ambient Thermal Resistance
Pd_total = Total Device Power Dissipation (example calculation is in **Power Dissipation**, above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance (θ_{JA}) must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 77.6°C/W per the following **Thermal Resistance** table. Therefore, t_J for an ambient temperature of 85°C with all its outputs switching is:

85°C + 0.311W * 77.6°C/W = 109.16°C. This is well below the limit of 125°C.

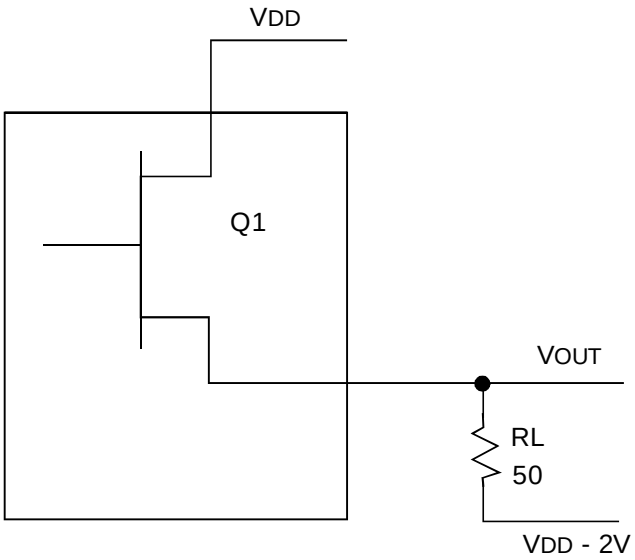
This calculation is only an example. t_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single-layer or multi-layer).

THERMAL RESISTANCE

θ_{JA} for 20-pin TSSOP, forced convection

θ_{JA} by Velocity (Linear Feet per mInute)				
	0	**200**	**400**	**Unit**
Multi-Layer PCB, JEDEC Standard Test boards	92.6	77.6	70.9	°C/W

CALCULATIONS AND EQUATIONS



LVPECL Output Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations, which assume a 50Ω load and a termination voltage of V_{DD} – 2V.

For Logic HIGH: $V_{OUT} = V_{OH\_MAX} = V_{DD\_MAX} – 1V$.
$(V_{DD\_MAX} – V_{OH\_MAX}) = 1V$

For Logic LOW: $V_{OUT} = V_{OL\_MAX} = V_{DD\_MAX} – 1.7V$.
$(V_{DD\_MAX} – V_{OL\_MAX}) = 1.7V$

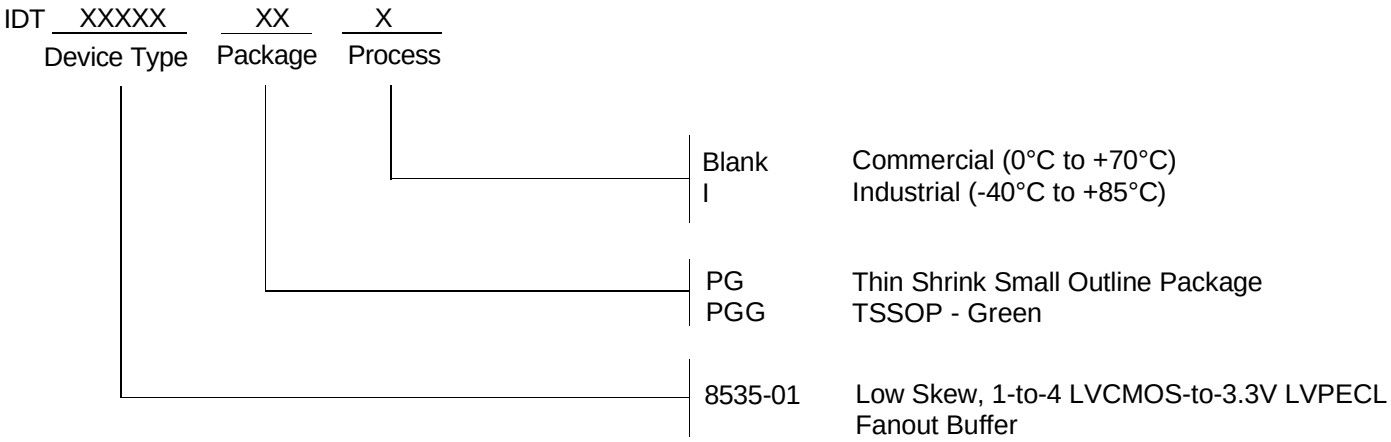
Pd_H is power dissipation when the output drives HIGH.
Pd_L is power dissipation when the output drives LOW.

$Pd\_H = \{[V_{OH\_MAX} – (V_{DD\_MAX} – 2V)] / R_L\} * (V_{DD\_MAX} – V_{OH\_MAX}) = \{[2V – (V_{DD\_MAX} – V_{OH\_MAX})] / R_L\} * (V_{DD\_MAX} – V_{OH\_MAX}) = [(2V – 1V) / 50Ω] * 1V = 20mW$.

$Pd\_L = \{[V_{OL\_MAX} – (V_{DD\_MAX} – 2V)] / R_L\} * (V_{DD\_MAX} – V_{OL\_MAX}) = \{[2V – (V_{DD\_MAX} – V_{OL\_MAX})] / R_L\} * (V_{DD\_MAX} – V_{OL\_MAX}) = [(2V – 1.7V) / 50Ω] * 1.7V = 10.2mW$.

Total Power Dissipation per output pair = Pd_H + Pd_L = 30.2mW

ORDERING INFORMATION



REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		1	NRND - Not Recommended For New Designs	5/20/2013

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