

## SNx4HC132 Quadruple Positive-NAND Gates With Schmitt-Trigger Inputs

### 1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive up to 10 LSTTL Loads
- Low Power Consumption, 20- $\mu$ A Maximum  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Maximum
- Operation from Very Slow Input Transitions
- Temperature-Compensated Threshold Levels
- High Noise Immunity
- Same Pinouts as SN74HC00

### 2 Applications

- Electronic Points-of-Sale
- Telecom Infrastructure
- Network Switches
- Tests and Measurements

### 3 Description

The SNx4HC132 device functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive and negative going signals. The SNx4HC132 devices perform the Boolean function  $Y = A \cdot B$  or  $Y = \bar{A} + \bar{B}$  in positive logic.

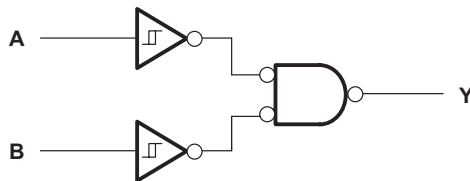
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
SN54HC132J	CDIP (14)	19.56 mm x 6.67 mm
SN74HC132D	SOIC (14)	4.90 mm x 3.91 mm
SN74HC132N	PDIP (14)	19.30 mm x 6.35 mm
SN54HC132FK	LCCC (20)	8.89 mm x 8.89 mm
SN54HC132W	CFP (14)	9.21 mm x 5.97 mm
SN74HC132PW	TSSOP (14)	5.00 mm x 4.40 mm
SN74HC132NS	SO (14)	10.30 mm x 5.30 mm
SN74HC132DB	SSOP (14)	6.20 mm x 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.3 Feature Description.....	<b>8</b>
<b>2 Applications</b> .....	<b>1</b>	8.4 Device Functional Modes.....	<b>8</b>
<b>3 Description</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>9</b>
<b>4 Revision History</b> .....	<b>2</b>	9.1 Application Information.....	<b>9</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	9.2 Typical Application .....	<b>9</b>
<b>6 Specifications</b> .....	<b>4</b>	<b>10 Power Supply Recommendations</b> .....	<b>10</b>
6.1 Absolute Maximum Ratings .....	<b>4</b>	<b>11 Layout</b> .....	<b>10</b>
6.2 ESD Ratings.....	<b>4</b>	11.1 Layout Guidelines .....	<b>10</b>
6.3 Recommended Operating Conditions.....	<b>4</b>	11.2 Layout Example .....	<b>10</b>
6.4 Thermal Information .....	<b>4</b>	<b>12 Device and Documentation Support</b> .....	<b>11</b>
6.5 Electrical Characteristics.....	<b>5</b>	12.1 Documentation Support .....	<b>11</b>
6.6 Switching Characteristics .....	<b>6</b>	12.2 Related Links .....	<b>11</b>
6.7 Operating Characteristics.....	<b>6</b>	12.3 Receiving Notification of Documentation Updates	<b>11</b>
6.8 Typical Characteristics.....	<b>6</b>	12.4 Community Resources.....	<b>11</b>
<b>7 Parameter Measurement Information</b> .....	<b>7</b>	12.5 Trademarks .....	<b>11</b>
<b>8 Detailed Description</b> .....	<b>8</b>	12.6 Electrostatic Discharge Caution.....	<b>11</b>
8.1 Overview .....	<b>8</b>	12.7 Glossary .....	<b>11</b>
8.2 Functional Block Diagram .....	<b>8</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>11</b>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

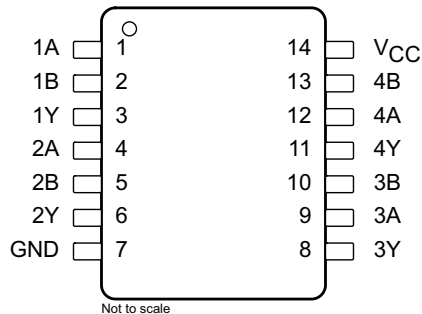
### Changes from Revision F (November 2004) to Revision G

Page

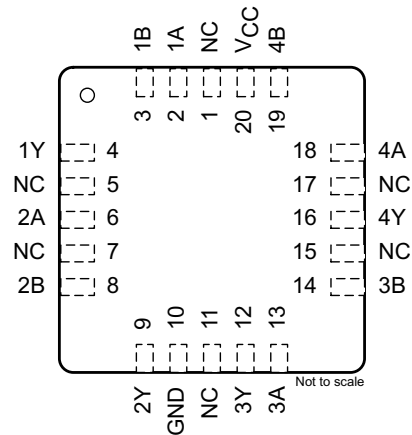
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... **1**
- Removed Ordering Information table, see POA at the end of the data sheet..... **1**

## 5 Pin Configuration and Functions

**D, DB, N, NS, J, W, or PW Package  
14-Pin SOIC, SSOP, PDIP, SO, or TSSOP  
Top View**



**FK Package  
20-Pin LCCC  
Top View**



**Pin Functions<sup>(1)</sup>**

NAME	PIN		I/O	DESCRIPTION
	SOIC, SSOP, PDIP, SO, TSSOP	LCCC		
1A	1	2	I	1A Input
1B	2	3	I	1B Input
1Y	3	4	O	1Y Output
2A	4	6	I	2A Input
2B	5	8	I	2B Input
2Y	6	9	O	2Y Output
3A	9	13	I	3A Input
3B	10	14	I	3B Input
3Y	8	12	O	3Y Output
4A	12	18	I	4A Input
4B	13	19	I	4B Input
4Y	11	16	O	4Y Output
GND	7	10	—	Ground Pin
NC	—	1, 5, 7, 11, 15, 17	—	No Connection
V <sub>CC</sub>	14	20	—	Power Pin

(1) NC – no connection

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>		±20 mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25 mA
	Continuous current through V <sub>CC</sub> or GND			±50 mA
T <sub>J</sub>	Junction temperature			150 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

See <sup>(1)</sup>

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
T <sub>A</sub>	Operating free-air temperature	SN54HC132		125	°C
		SN74HC132		85	

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74HC132					UNIT	
	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)		
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	84.3	99.1	50.9	84.3	113.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	44.8	51.3	38.2	42.2	42.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	38.5	46.3	30.8	43.0	54.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	13.9	17.7	23.1	13.5	4.0	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	38.2	45.8	30.7	42.7	54.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the application report, [Semiconductor and IC Package Thermal Metrics](#).
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP	MAX	UNIT		
V <sub>T+</sub>			2 V	0.7	1.2	1.5	V		
			4.5 V	1.55	2.5	3.15			
			6 V	2.1	3.3	4.2			
V <sub>T-</sub>			2 V	0.3	0.6	1	V		
			4.5 V	0.9	1.6	2.45			
			6 V	1.2	2	3.2			
V <sub>T+</sub> – V <sub>T-</sub>			2 V	0.2	0.6	1.2	V		
			4.5 V	0.4	0.9	2.1			
			6 V	0.5	1.3	2.5			
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = –20 μA	2 V	1.9	1.998		V		
			4.5 V	4.4	4.499				
			6 V	5.9	5.999				
		I <sub>OH</sub> = –4 mA	T <sub>A</sub> = 25°C		4.5 V	3.98		4.3	
			SN54HC132					3.7	
			SN74HC132					3.84	
		I <sub>OH</sub> = –5.2 mA	T <sub>A</sub> = 25°C		6 V	5.48		5.8	
			SN54HC132					5.2	
			SN74HC132					5.34	
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1	V		
			4.5 V		0.001	0.1			
			6 V		0.001	0.1			
		I <sub>OL</sub> = 4 mA	T <sub>A</sub> = 25°C		4.5 V	0.17		0.26	
			SN54HC132					0.4	
			SN74HC132					0.33	
		I <sub>OL</sub> = 5.2 mA	T <sub>A</sub> = 25°C		6 V	0.15		0.26	
			SN54HC132					0.4	
			SN74HC132					0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	T <sub>A</sub> = 25°C		6 V	±0.1		±100		
		SN54HC132, SN74HC132					±1000		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	T <sub>A</sub> = 25°C		6 V			2		
		SN54HC132					40		
		SN74HC132					20		
C <sub>i</sub>			2 V to 6 V	3		10	pF		

## 6.6 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A$	MIN	TYP	MAX	UNIT
$t_{pd}$	A or B	Y	2 V	$T_A = 25^\circ\text{C}$		60	120	ns
				SN54HC132			186	
				SN74HC132			156	
			4.5 V	$T_A = 25^\circ\text{C}$		18	25	
				SN54HC132			37	
				SN74HC132			31	
			6 V	$T_A = 25^\circ\text{C}$		14	21	
				SN54HC132			32	
				SN74HC132			27	
$t_t$	Any	Any	2 V	$T_A = 25^\circ\text{C}$		28	75	ns
				SN54HC132			110	
				SN74HC132			95	
			4.5 V	$T_A = 25^\circ\text{C}$		8	15	
				SN54HC132			22	
				SN74HC132			19	
			6 V	$T_A = 25^\circ\text{C}$		6	13	
				SN54HC132			19	
				SN74HC132			16	

## 6.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per gate	No load	20	pF

## 6.8 Typical Characteristics

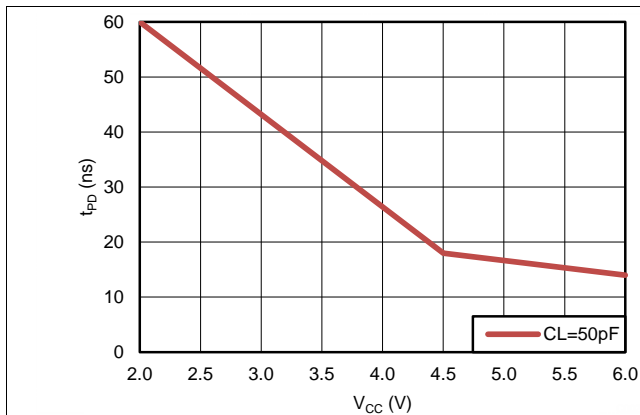


Figure 1. Propagation Delay vs  $V_{CC}$

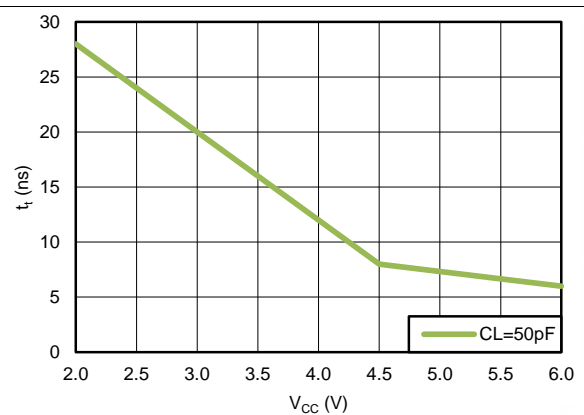
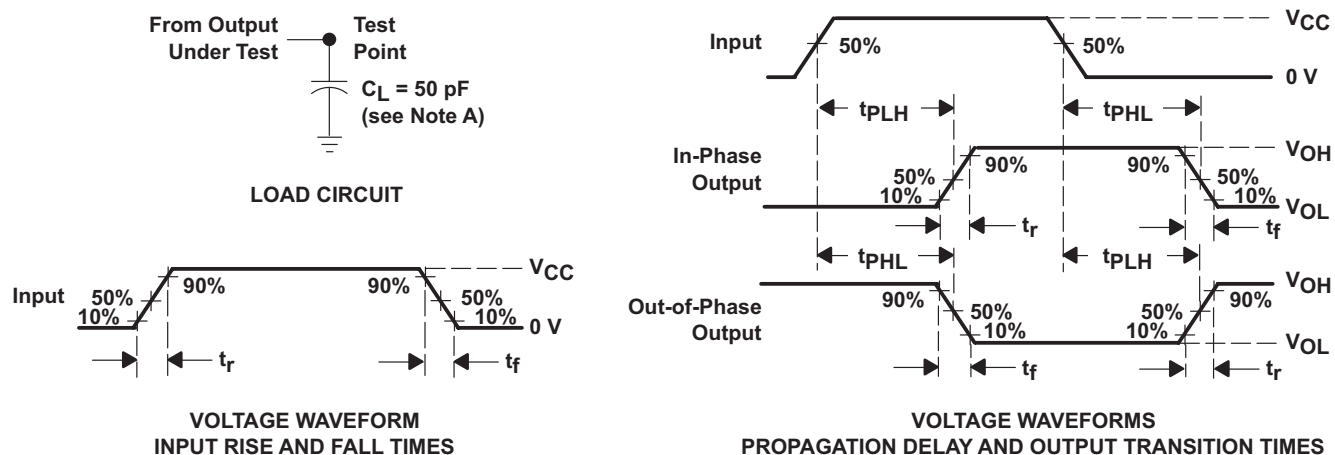


Figure 2. Transition Time vs  $V_{CC}$

## 7 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.  
 C. The outputs are measured one at a time, with one input transition per measurement.  
 D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 3. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SNx4HC132 is a quadruple 2-input positive-NAND gate with low drive that produces slow rise and fall times. This reduces ringing on the output signal.

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

### 8.2 Functional Block Diagram

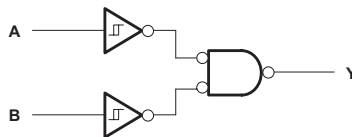


Figure 4. Logic Diagram (Positive Logic)

### 8.3 Feature Description

The SNx4HC132 has a wide operating range of 2 V to 6 V. The SNx4HC132 also has a low power consumption where the maximum ICC is 20  $\mu$ A.

### 8.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4HC132.

Table 1. Function Table (Each Gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74HC132 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates minimize overshoot and undershoot on the outputs. The inputs can accept voltages to  $V_{CC}$ . The current consumption of the device is low with maximum  $20\text{-}\mu\text{A } I_{CC}$ .

### 9.2 Typical Application

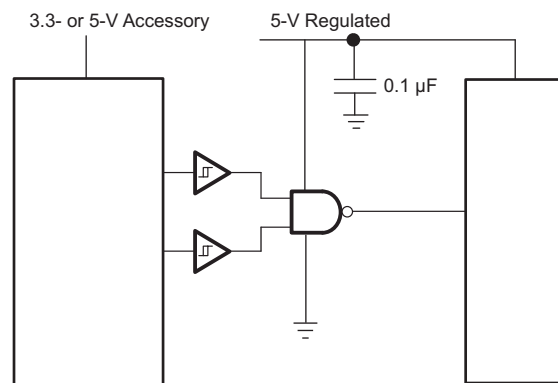


Figure 5. Typical Application Diagram

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the [Recommended Operating Conditions](#) table.
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [Recommended Operating Conditions](#) table.
2. Recommend Output Conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs must not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 9.2.3 Application Curve

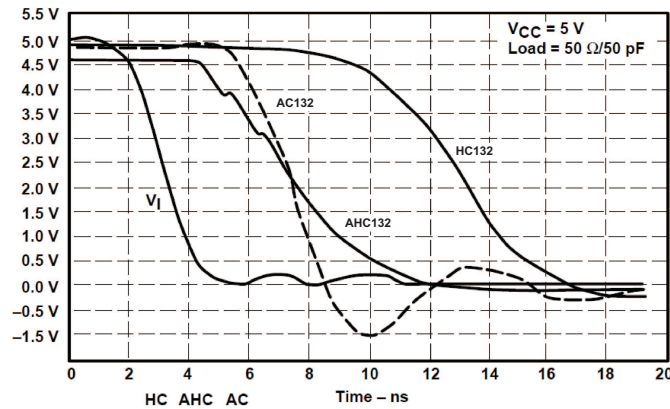


Figure 6. Switching Characteristics Comparison

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply-voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins then a 0.01  $\mu\text{F}$  or a 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and a 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the I/Os so they also cannot float when disabled.

### 11.2 Layout Example

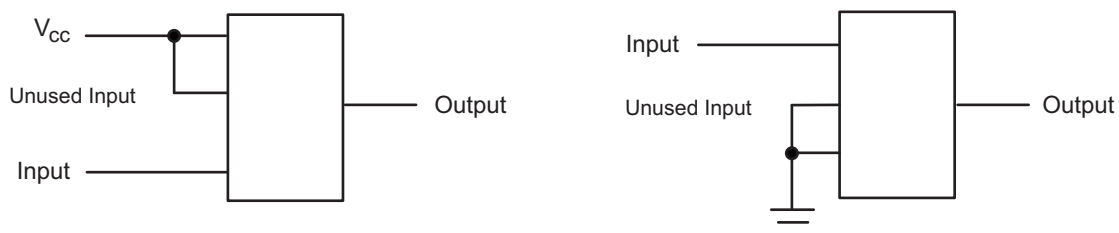


Figure 7. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC132	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74HC132	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89845022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 89845022A SNJ54HC 132FK	<a href="#">Samples</a>
5962-8984502CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8984502CA SNJ54HC132J	<a href="#">Samples</a>
5962-8984502DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8984502DA SNJ54HC132W	<a href="#">Samples</a>
5962-8984502VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8984502VC A SNV54HC132J	<a href="#">Samples</a>
5962-8984502VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8984502VD A SNV54HC132W	<a href="#">Samples</a>
SN54HC132J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC132J	<a href="#">Samples</a>
SN74HC132D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC132DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC132DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC132N	<a href="#">Samples</a>
SN74HC132NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC132N	<a href="#">Samples</a>
SN74HC132NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC132PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SN74HC132PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC132	<a href="#">Samples</a>
SNJ54HC132FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 89845022A SNJ54HC 132FK	<a href="#">Samples</a>
SNJ54HC132J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8984502CA	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54HC132J	
SNJ54HC132W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8984502DA SNJ54HC132W	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC132, SN54HC132-SP, SN74HC132 :**

- Catalog: [SN74HC132](#), [SN54HC132](#)
- Automotive: [SN74HC132-Q1](#), [SN74HC132-Q1](#)
- Military: [SN54HC132](#)
- Space: [SN54HC132-SP](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC132DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC132DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC132DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC132DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC132PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC132PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**

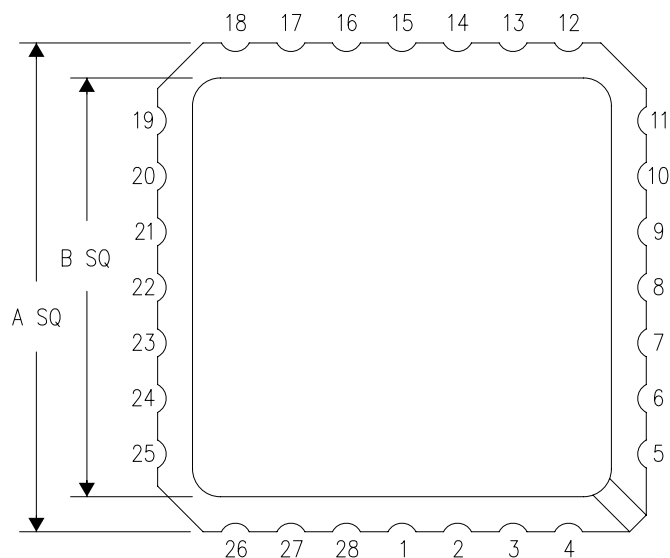

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC132DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74HC132DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC132DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC132DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HC132PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC132PWT	TSSOP	PW	14	250	367.0	367.0	35.0

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)