SRAM 1 MEG x 1 SRAM

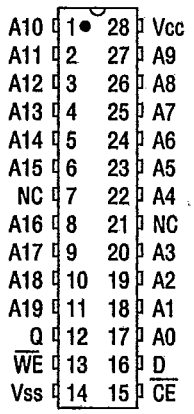
FEATURES

- High speed: 25, 35, and 45ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

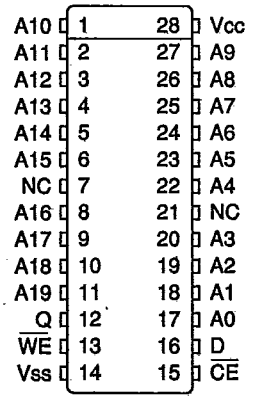
OPTIONS	MARKING
• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (400 mil)	None
Ceramic DIP (400mil)	C
Plastic SOJ (400 mil)	DJ
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

28L/400 DIP
(A-10)



28L/400 SOJ
(E-9)



GENERAL DESCRIPTION

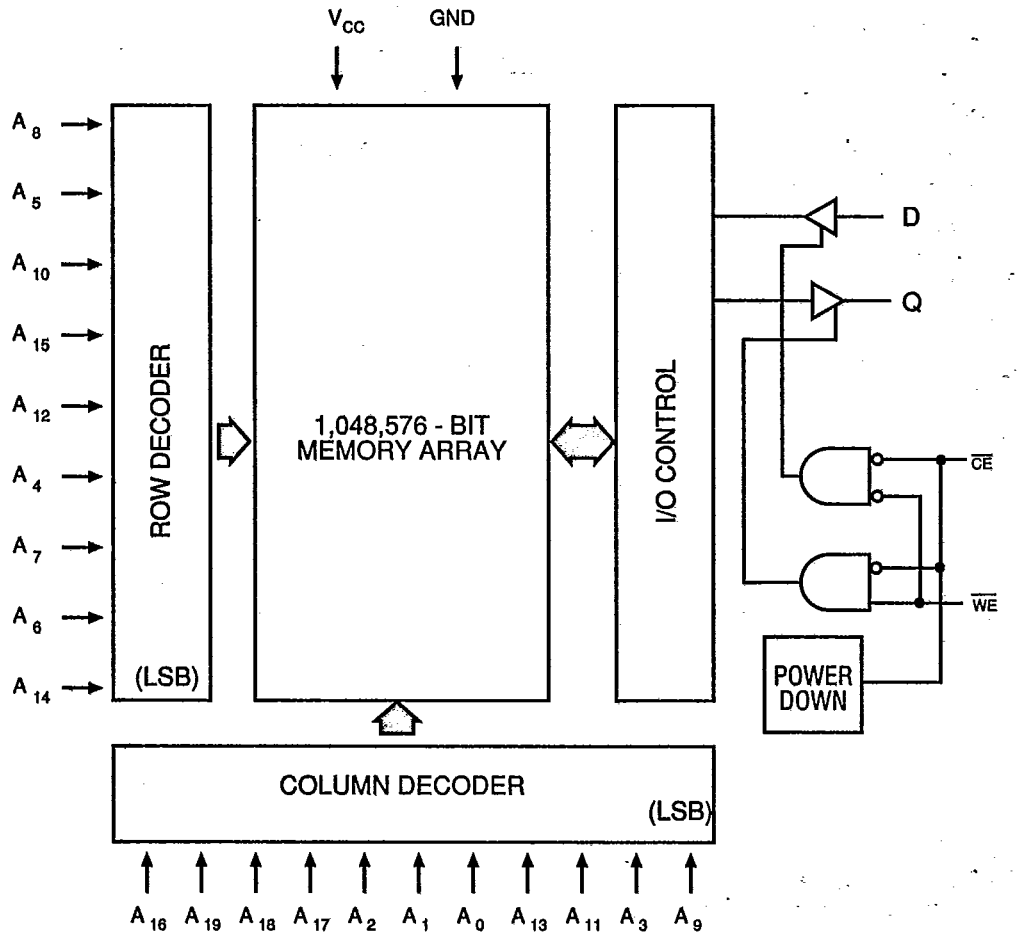
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A6 and A14) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; Vcc = MAX f = MAX = 1/ ^tRC, Outputs Open	Icc		120	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; Vcc = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}		30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; Vcc = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}		7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		8	pF	4
Output Capacitance	Vcc = 5V	Co		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; Vcc = 5V ± 10%)

DESCRIPTION		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	25		35		45		ns	
Address access time	^tAA		25		35		45	ns	
Chip Enable access time	^tACE		25		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip Disable to power-down time	^tPD		25		35		45	ns	
WRITE Cycle									
WRITE cycle time	^tWC	25		35		45		ns	
Chip Enable to end of write	^tCW	15		20		25		ns	
Address valid to end of write	^tAW	15		20		25		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
Write pulse width	^tWP	15		20		25		ns	
Data setup time	^tDS	10		15		20		ns	
Data hold time	^tDH	0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	0		0		0		ns	
Write Enable to output in High-Z	^tHZWE	0	10	0	15	0	18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

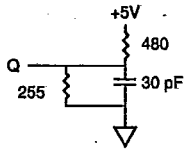


Fig. 1 OUTPUT LOAD EQUIVALENT

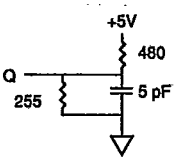


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

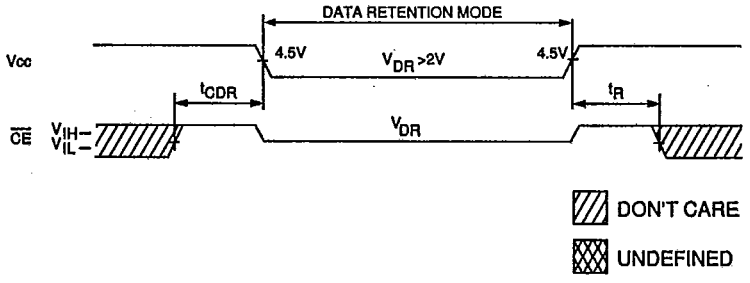
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enable held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-171.

FAST SRAM

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

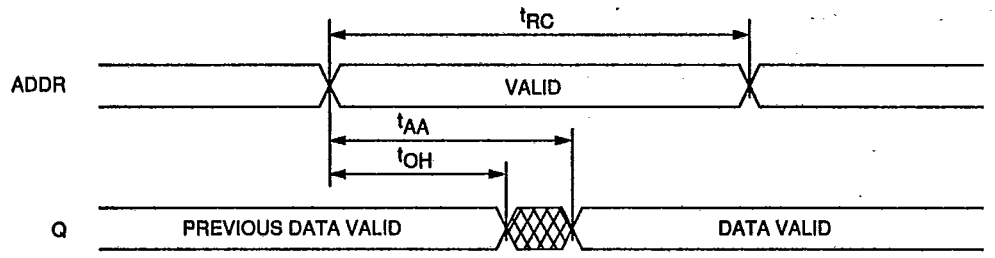
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	Vcc = 2v	I_{CCDR}		95	500	µA	
		Vcc = 3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

LOW Vcc DATA RETENTION WAVEFORM

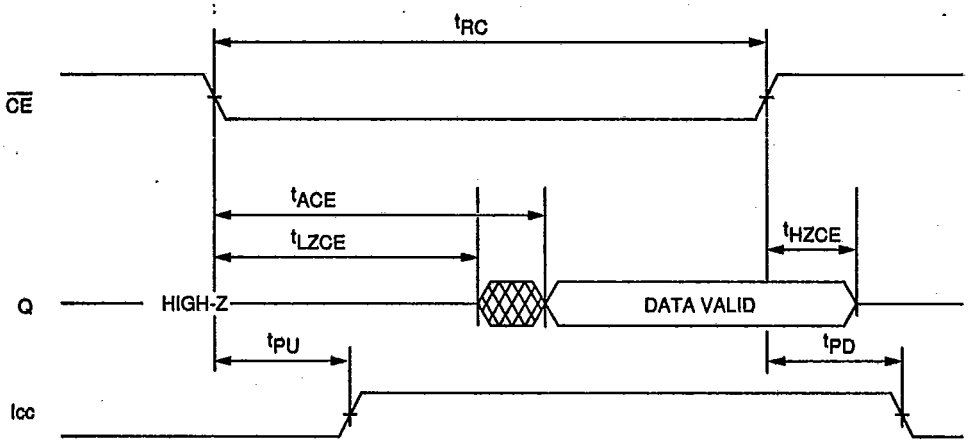


FAST SRAM

READ CYCLE NO. 1 [8, 9]

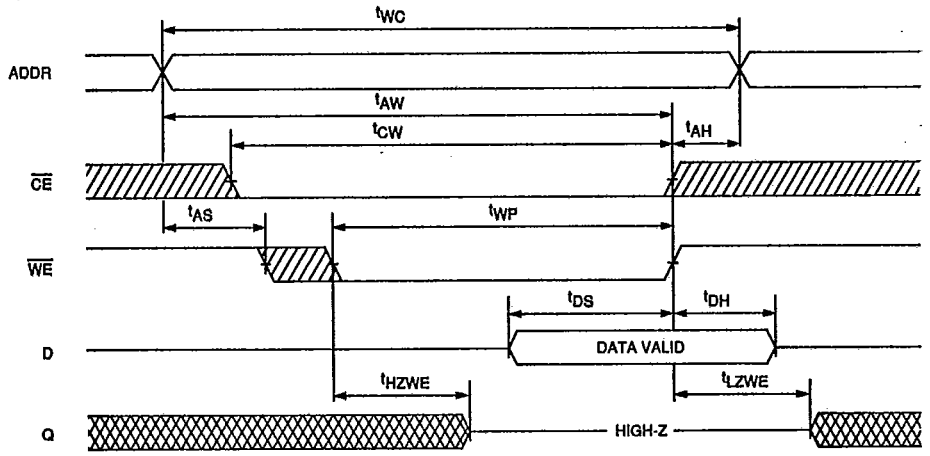


READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1

(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2

(Chip Enable Controlled) [12]