pFLASH
Superior Endurance and Performance

Pm39LV512 / Pm39LV010 / Pm39LV020 / Pm39LV040

512 Kbit / 1Mbit / 2Mbit / 4Mbit 3.0 Volt-only CMOS Flash Memory

FEATURES

• Single Power Supply Operation
- Low voltage range: 2.7 V - 3.6 V

• Memory Organization
- Pm39LV512: 64K x 8 (512 Kbit)
- Pm39LV010: 128K x 8 (1 Mbit)
- Pm39LV020: 256K x 8 (2 Mbit)
- Pm39LV040: 512K x 8 (4 Mbit)

• High Performance Read
- 55/70 ns access time

• Cost Effective Sector/Block Architecture
- Uniform 4 Kbyte sectors
- Uniform 64 Kbyte blocks (sector group - except Pm39LV512)

• Data# Polling and Toggle Bit Features

• Hardware Data Protection

• Automatic Erase and Byte Program
- Build-in automatic program verification
- Typical 16 µs/byte programming time
- Typical 55 ms sector/block/chip erase time

• Low Power Consumption
- Typical 4 mA active read current
- Typical 8 mA program/erase current
- Typical 0.1 µA CMOS standby current

• High Product Endurance
- Guarantee 100,000 program/erase cycles per single sector (preliminary)
- Minimum 20 years data retention

• Industrial Standard Pin-out and Packaging
- 32-pin (8 mm x 14 mm) VSOP
- 32-pin PLCC
- Optional lead-free (Pb-free) package

GENERAL DESCRIPTION

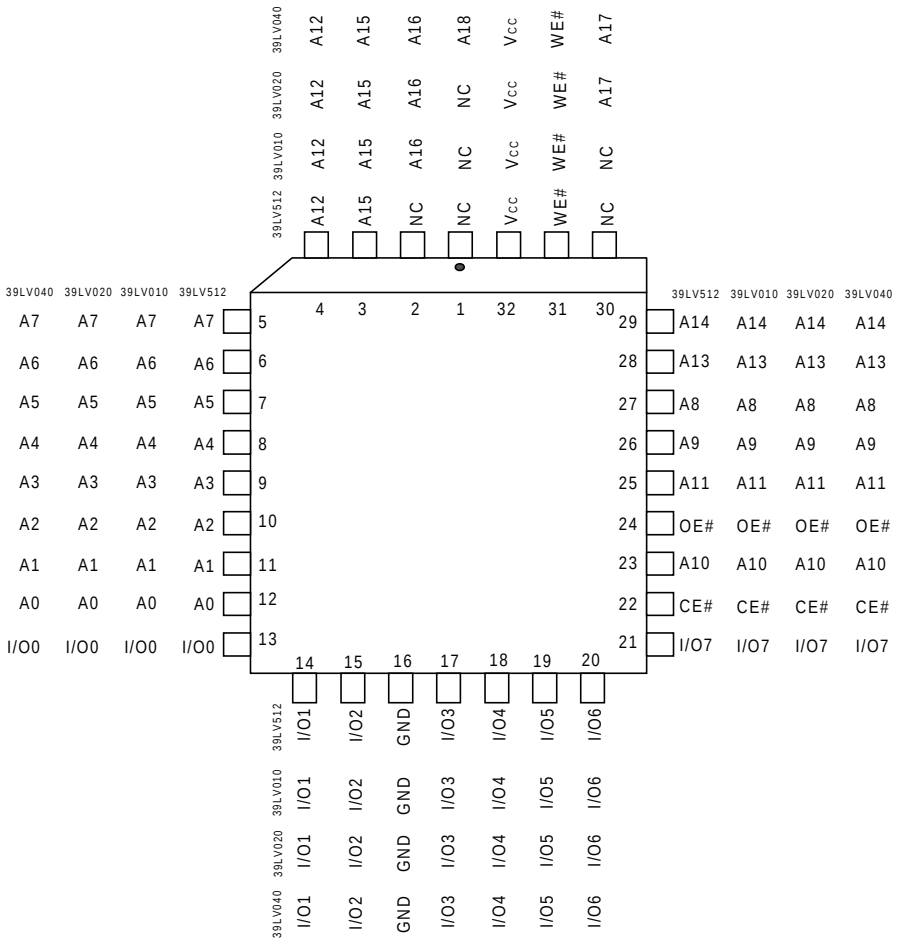
The Pm39LV512/010/020/040 are 512 Kbit/1 Mbit/2 Mbit/4 Mbit 3.0 Volt-only Flash Memories. These devices are designed to use a single low voltage, range from 2.7 Volt to 3.6 Volt, power supply to perform read, erase and program operations. The 12.0 Volt V_{PP} power supply for program and erase operations are not required. The devices can be programmed in standard EPROM programmers as well.

The memory array of Pm39LV512 is divided into uniform 4 Kbyte sectors for data or code storage. The memory arrays of Pm39LV010/020/040 are divided into uniform 4 Kbyte sectors or uniform 64 Kbyte blocks (sector group - consists of sixteen adjacent sectors). The sector or block erase feature allows users to flexibly erase a memory area as small as 4 Kbyte or as large as 64 Kbyte by one single erase operation without affecting the data in others. The chip erase feature allows the whole memory array to be erased in one single erase operation. The devices can be programmed on a byte-by-byte basis after performing the erase operation.

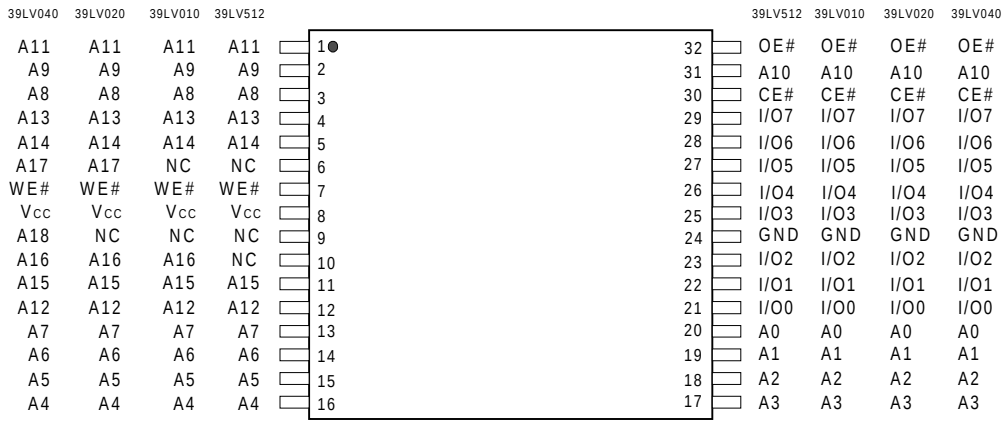
The devices have a standard microprocessor interface as well as a JEDEC standard pin-out/command set. The program operation is executed by issuing the program command code into command register. The internal control logic automatically handles the programming voltage ramp-up and timing. The erase operation is executed by issuing the chip erase, block, or sector erase command code into command register. The internal control logic automatically handles the erase voltage ramp-up and timing. The preprogramming on the array which has not been programmed is not required before an erase operation. The devices offer Data# Polling and Toggle Bit functions, the progress or completion of program and erase operations can be detected by reading the Data# Polling on I/O7 or the Toggle Bit on I/O6.

The Pm39LV512/010/020/040 are manufactured on pFLASH™'s advanced nonvolatile CMOS technology. The devices are offered in 32-pin VSOP and PLCC packages with 70 ns access time.

CONNECTION DIAGRAMS

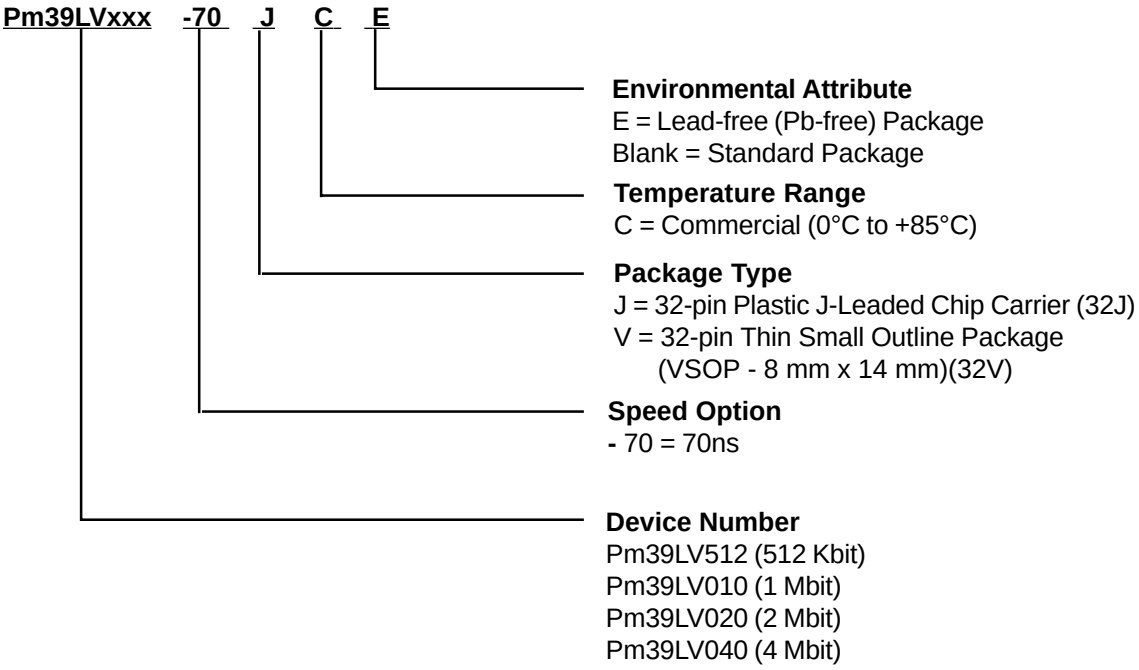


32-Pin PLCC



32-Pin VSOP

PRODUCT ORDERING INFORMATION



Part Number	t_{ACC} (ns)	Package	Temperature Range
Pm39LV512-70JCE	70	32J	Commercial (0ºC to +85ºC)
Pm39LV512-70JC			
Pm39LV512-70VCE		32V	
Pm39LV512-70VC			
Pm39LV010-70JCE	70	32J	
Pm39LV010-70JC			
Pm39LV010-70VCE		32V	
Pm39LV010-70VC			
Pm39LV020-70JCE	70	32J	
Pm39LV020-70JC			
Pm39LV020-70VCE		32V	
Pm39LV020-70VC			
Pm39LV040-70JCE	70	32J	
Pm39LV040-70JC			
Pm39LV040-70VCE		32V	
Pm39LV040-70VC			

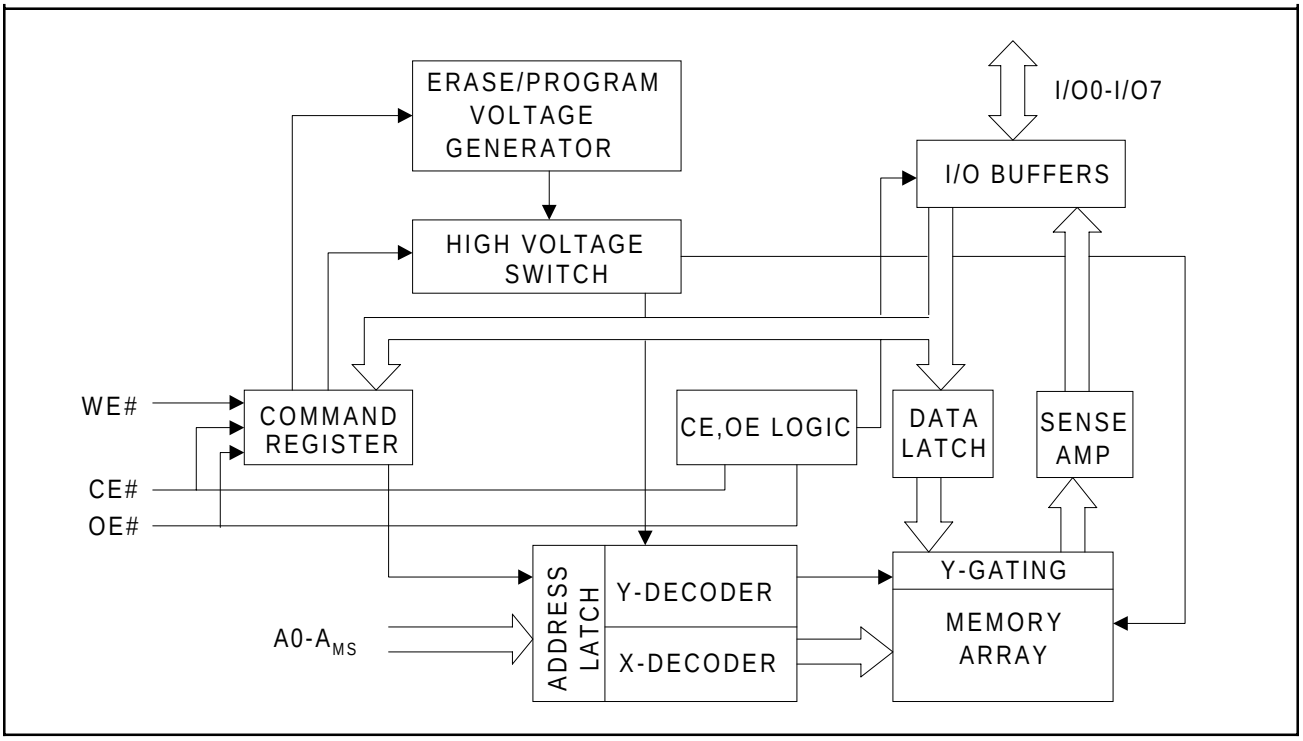
PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
A0 - A_{MS}(1)	INPUT	Address Inputs: For memory addresses input. Addresses are internally latched on the falling edge of WE# during a write cycle.
CE#	INPUT	Chip Enable: CE# goes low activates the device's internal circuitries for device operation. CE# goes high deselects the device and switches into standby mode to reduce the power consumption.
WE#	INPUT	Write Enable: Activate the device for write operation. WE# is active low.
OE#	INPUT	Output Enable: Control the device's output buffers during a read cycle. OE# is active low.
I/O0 - I/O7	INPUT/ OUTPUT	Data Inputs/Outputs: Input command/data during a write cycle or output data during a read cycle. The I/O pins float to tri-state when OE# are disabled.
V_{CC}		Device Power Supply
GND		Ground
NC		No Connection

Note:

1. A_{MS} is the most significant address where A_{MS} = A15 for Pm39LV512, A16 for Pm39LV010, A17 for Pm39LV020, and A18 for Pm39LV040.

BLOCK DIAGRAM



DEVICE OPERATION

READ OPERATION

The access of Pm39LV512/010/020/040 are similar to EPROM. To read data, three control functions must be satisfied:

• CE# is the chip enable and should be pulled low (V_{IL}).

• OE# is the output enable and should be pulled low (V_{IL}).

• WE# is the write enable and should remains high (V_{IH}).

PRODUCT IDENTIFICATION

The product identification mode can be used to identify the manufacturer and the device through hardware or software read ID operation. See Table 1 for pFLASH™ Manufacturer ID and Device ID. The hardware ID mode is activated by applying a 12.0 Volt on A9 pin, typically used by an external programmer for selecting the right programming algorithm for the devices. Refer to Table 2 for Bus Operation Modes. The software ID mode is activated by a three-bus-cycle command. See Table 3 for Software Command Definition.

BYTE PROGRAMMING

The programming is a four-bus-cycle operation and the data is programmed into the devices (to a logical “0”) on a byte-by-byte basis. See Table 3 for Software Command Definition. A program operation is activated by writing the three-byte command sequence followed by program address and one byte of program data into the devices. The addresses are latched on the falling edge of WE# or CE# whichever occurs later, and the data are latched on the rising edge of WE# or CE# whichever occurs first. The internal control logic automatically handles the internal programming voltages and timing.

A data “0” can not be programmed back to a “1”. Only erase operation can convert the “0”s to “1”s. The Data# Polling on I/O7 or Toggle Bit on I/O6 can be used to detect the progress or completion of a program cycle.

DEVICE OPERATION (CONTINUED)

CHIP ERASE

The entire memory array can be erased through a chip erase operation. Pre-programs the devices are not required prior to a chip erase operation. Chip erase starts immediately after a six-bus-cycle chip erase command sequence. All commands will be ignored once the chip erase operation has started. The devices will return to standby mode after the completion of chip erase.

SECTOR AND BLOCK ERASE

The memory array of Pm39LV512/010/020/040 are organized into uniform 4 Kbyte sectors. A sector erase operation allows to erase any individual sector without affecting the data in others. The memory array of Pm39LV010/020/040, excluding Pm39LV512, are also organized into uniform 64 Kbyte blocks (sector group - consists of sixteen adjacent sectors). A block erase operation allows to erase any individual block. The sector or block erase operation is similar to chip erase.

I/O7 DATA# POLLING

The Pm39LV512/010/020/040 provide a Data# Polling feature to indicate the progress or completion of a program and erase cycles. During a program cycle, an attempt to read the devices will result in the complement of the last loaded data on I/O7. Once the program operation is completed, the true data of the last loaded data is valid on all outputs. During a sector, block, or chip erase cycle, an attempt to read the device will result a “0” on I/O7. After the erase operation is completed, an attempt to read the device will result a “1” on I/O7.

I/O6 TOGGLE BIT

The Pm39LV512/010/020/040 also provide a Toggle Bit feature to detect the progress or completion of a program and erase cycles. During a program or erase cycle, an attempt to read data from the device will result a toggling between “1” and “0” on I/O6. When the program or erase operation is complete, I/O6 will stop toggling and valid data will be read. Toggle bit may be accessed at any time during a program or erase cycle.

HARDWARE DATA PROTECTION

Hardware data protection protects the devices from unintentional erase or program operation. It is performed in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8 V (typical), the write operation is inhibited. (b) Write inhibit: holding any of the signal OE# low, CE# high, or WE# high inhibits a write cycle. (c) Noise filter: pulses of less than 5 ns (typical) on the WE# or CE# input will not initiate a write operation.

Table 1. Product Identification

Product Identification	Data
Manufacturer ID	9Dh
Device ID:	
Pm39LV512	1Bh
Pm39LV010	1Ch
Pm39LV020	3Dh
Pm39LV040	3Eh

SECTOR/BLOCK ADDRESS TABLE

Memory Density				Block [1]	Block Size (Kbytes)	Sector	Sector Size (Kbytes)	Address Range
512Kbit	1 Mbit	2 Mbit	4 Mbit	Block 0 [2]	64	Sector 0	4	00000h - 00FFFh
						Sector 1	4	01000h - 01FFFh
						:	:	:
						Sector 15	4	0F000h - 0FFFFh
				Block 1	64	Sector 16	4	10000h - 10FFFh
						Sector 17	4	11000h - 11FFFh
						:	:	:
						Sector 31	4	1F000h - 1FFFFh
				Block 2	64	"	"	20000h - 2FFFFh
				Block 3	64	"	"	30000h - 3FFFFh
				Block 4	64	"	"	40000h - 4FFFFh
				Block 5	64	"	"	50000h - 5FFFFh
				Block 6	64	"	"	60000h - 6FFFFh
				Block 7	64	"	"	70000h - 7FFFFh

Notes:

1. A Block is a 64 Kbyte sector group which consists of sixteen adjecent sectors of 4 Kbyte each.
2. Block erase feature is available for Pm39LV010/020/040 only. The chip erase command should be used to erase the Block 0 for the Pm39LV512.

OPERATING MODES

Table 2. Bus Operation Modes

Mode	CE#	OE#	WE#	ADDRESS	I/O
Read	V_{IL}	V_{IL}	V_{IH}	X (1)	D_{OUT}
Write	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}
Standby	V_{IH}	X	X	X	High Z
Output Disable	X	V_{IH}	X	X	High Z
Product Identification Hardware	V_{IL}	V_{IL}	V_{IH}	A2 - A_{MS} (2) = X, A9 = V_H (3), A1 = V_{IL}, A0 = V_{IL}	Manufacturer ID
				A2 - A_{MS} (2) = X, A9 = V_H (3), A1 = V_{IL}, A0 = V_{IH}	Device ID

Notes:
1. X can be V_{IL}, V_{IH} or addresses.
2. A_{MS} = Most significant address;
   A_{MS} = A15 for Pm39LV512, A16 for Pm39LV010,
   A17 for Pm39LV020, and A18 for Pm39LV040.
3. V_H = 12.0 V ± 0.5 V.

COMMAND DEFINITION

Table 3. Software Command Definition

Command Sequence	Bus Cycle	1st Bus Cycle Addr Data	2nd Bus Cycle Addr Data	3rd Bus Cycle Addr Data	4th Bus Cycle Addr Data	5th Bus Cylce Addr Data	6th Bus Cycle Addr Data
Read	1	Addr D_{OUT}					
Chip Erase	6	555h AAh	2AAh 55h	555h 80h	555h AAh	2AAh 55h	555h 10h
Sector Erase	6	555h AAh	2AAh 55h	555h 80h	555h AAh	2AAh 55h	SA (1) 30h
Block Erase	6	555h AAh	2AAh 55h	555h 80h	555h AAh	2AAh 55h	BA (2) 50h
Byte Program	4	555h AAh	2AAh 55h	555h A0h	Addr D_{IN}		
Product ID Entry	3	555h AAh	2AAh 55h	555h 90h			
Product ID Exit (3)	3	555h AAh	2AAh 55h	555h F0h			
Product ID Exit (3)	1	XXXh F0h					

Notes:
1. SA = Sector address of the sector to be erased.
2. BA = Block address of the block to be erased.
3. Either one of the Product ID Exit command can be used.

DEVICE OPERATIONS FLOWCHARTS

AUTOMATIC PROGRAMMING

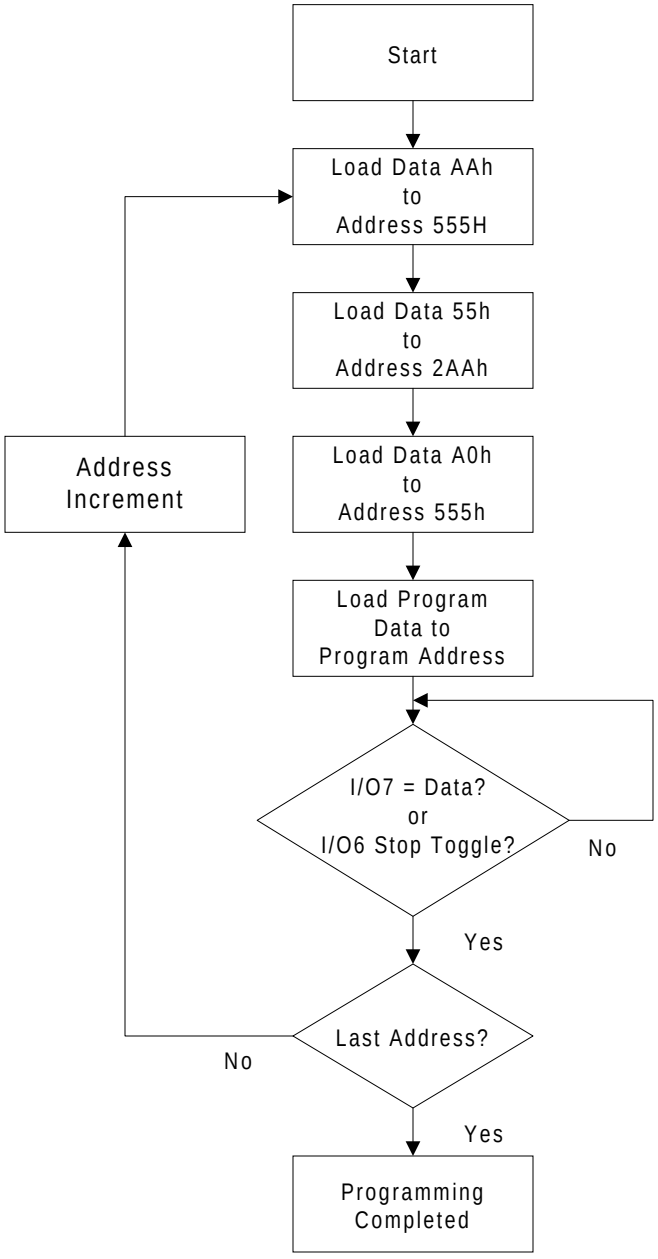
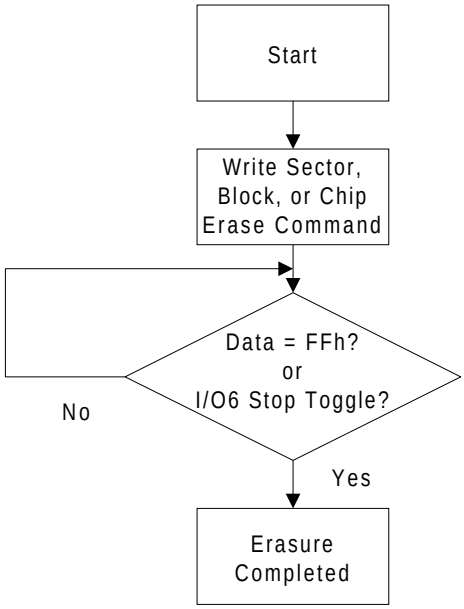


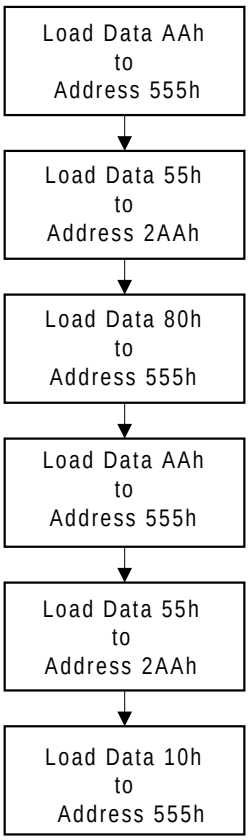
Chart 1. Automatic Programming Flowchart

DEVICE OPERATIONS FLOWCHARTS (CONTINUED)

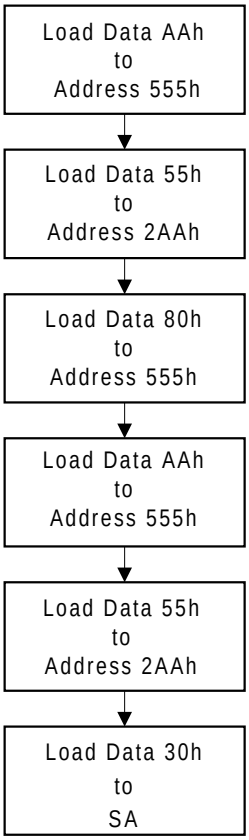
AUTOMATIC ERASE



CHIP ERASE COMMAND



SECTOR ERASE COMMAND



BLOCK ERASE COMMAND

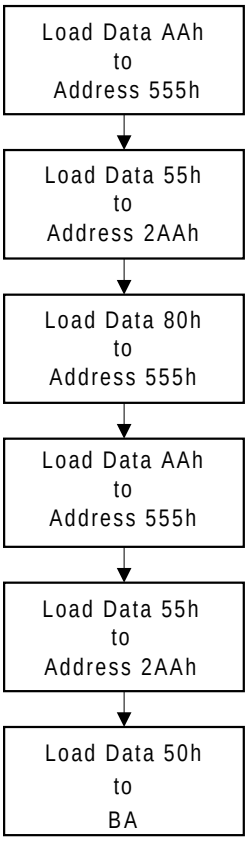
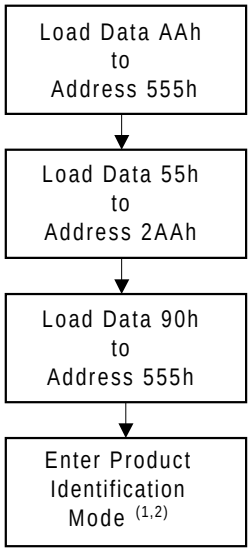


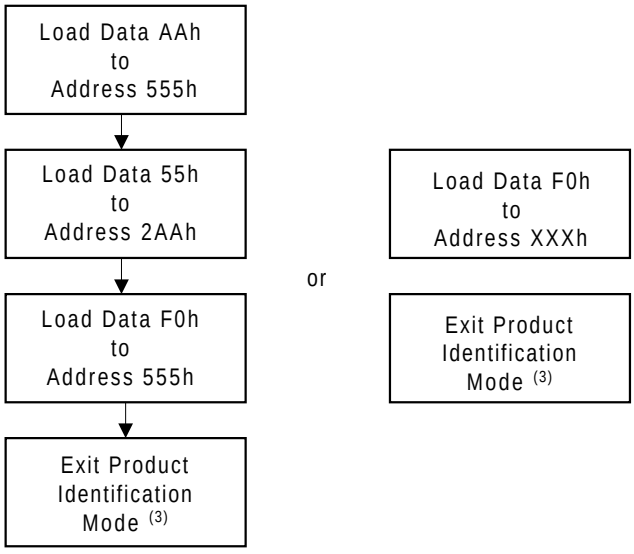
Chart 2. Automatic Erase Flowchart

DEVICE OPERATIONS FLOWCHARTS (CONTINUED)

SOFTWARE PRODUCT IDENTIFICATION ENTRY



SOFTWARE PRODUCT IDENTIFICATION EXIT



Notes:
1. The device will enter Product Identification mode after excuting the Product ID Entry command.
2. Under Product Identification mode, the Manufacturer ID and Device ID of devices can be read at address X0000h and X0001h where X = Don't Care.
3. The device returns to standby operation.

Chart 3. Software Product Identification Entry/Exit Flowchart

ABSOLUTE MAXIMUM RATINGS (1)

Temperature Under Bias		-65°C to +125°C
Storage Temperature		-65°C to +125°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins except A9 pin(2)		-0.5 V to V_{CC} + 0.5 V
Input Voltage with Respect to Ground on A9 pin(3)		-0.5 V to +13.0 V
All Output Voltage with Respect to Ground		-0.5 V to V_{CC} + 0.5 V
V_{CC} (2)		-0.5 V to +6.0 V

Notes:
1. Stresses under those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device or any other conditions under those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affected device reliability.
2. Maximum DC voltage on input or I/O pins are V_{CC} + 0.5 V. During voltage transitioning period, input or I/O pins may overshoot to V_{CC} + 2.0 V for a period of time up to 20 ns. Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitioning period, input or I/O pins may undershoot GND to -2.0 V for a period of time up to 20 ns.
3. Maximum DC voltage on A9 pin is +13.0 V. During voltage transitioning period, A9 pin may overshoot to +14.0 V for a period of time up to 20 ns. Minimum DC voltage on A9 pin is -0.5 V. During voltage transitioning period, A9 pin may undershoot GND to -2.0 V for a period of time up to 20 ns.

DC AND AC OPERATING RANGE

Part Number	**Pm39LV512/010/020/040**
Operating Temperature	0°C to +85°C
Vcc Power Supply	2.7 V - 3.6 V

DC CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN}= 0 V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$= 0 V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	CE#, OE# = V_{CC} ?0.3 V		0.1	5	µA
I_{SB2}	V_{CC} Standby Current TTL	CE# = V_{IH} to V_{CC}		0.05	3	mA
I_{CC1}	V_{CC} Active Read Current	f = 5 MHz; I_{OUT}= 0 mA		4	15	mA
I_{CC2}(1)	V_{CC} Program/Erase Current			8	20	mA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL}= 2.1 mA; V_{CC}= V_{CC} min			0.45	V
V_{OH}	Output High Voltage	I_{OH}= -100 µA; V_{CC}= V_{CC} min	V_{CC} - 0.2			V

Note: 1. Characterized but not 100% tested.

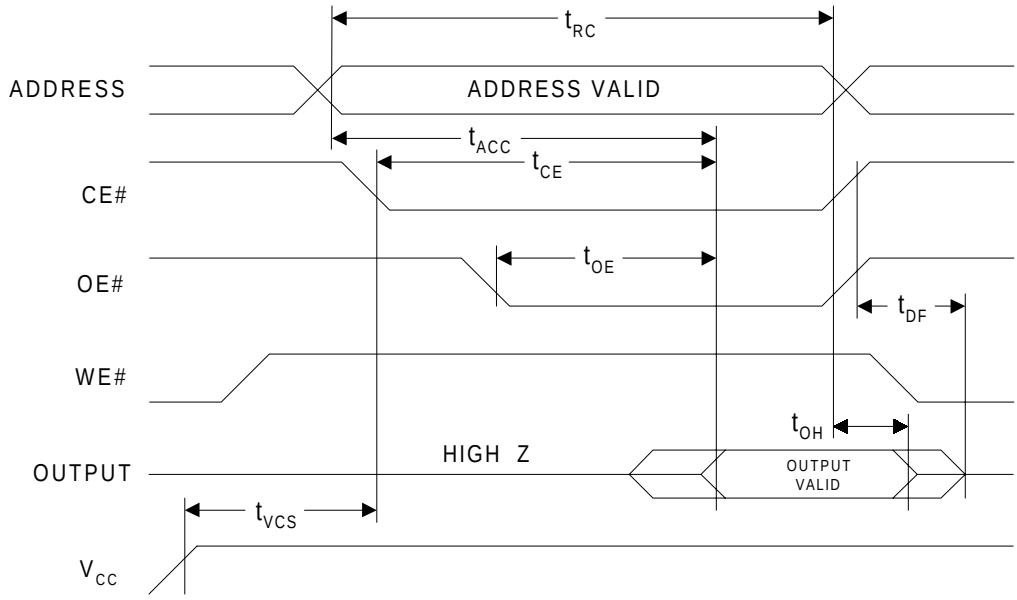
AC CHARACTERISTICS

READ OPERATIONS CHARACTERISTICS

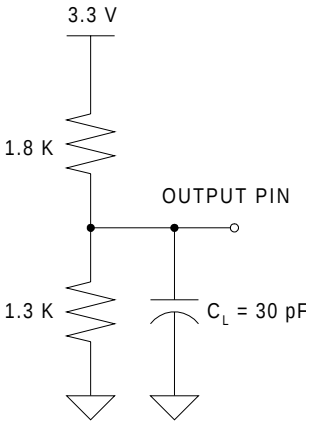
Symbol	Parameter	Pm39LV512-55 Pm39LV010-55 Pm39LV020-55 Pm39LV040-55		Pm39LV512-70 Pm39LV010-70 Pm39LV020-70 Pm39LV040-70		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	55		70		ns
t_{ACC}	Address to Output Delay		55		70	ns
t_{CE}	CE# to Output Delay		55		70	ns
t_{OE}	OE# to Output Delay		30		35	ns
t_{DF}	CE# or OE# to Output High Z	0	15	0	25	ns
t_{OH}	Output Hold from OE#, CE# or Address, whichever occured first	0		0		ns
t_{VCS}	V_{CC} Set-up Time	50		50		µs

AC CHARACTERISTICS (CONTINUED)

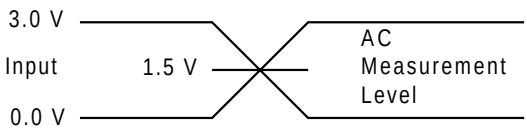
READ OPERATIONS AC WAVEFORMS



OUTPUT TEST LOAD



INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



PIN CAPACITANCE (f = 1 MHz, T = 25°C)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

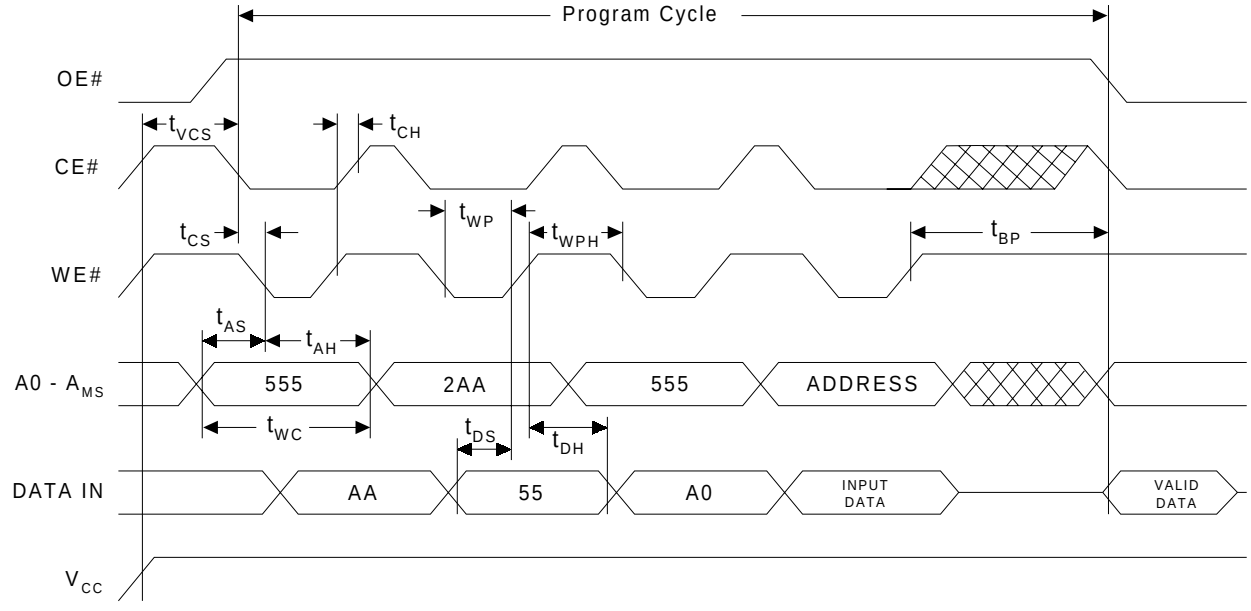
Note: These parameters are characterized but not 100% tested.

AC CHARACTERISTICS (CONTINUED)

WRITE (PROGRAM/ERASE) OPERATIONS CHARACTERISTICS

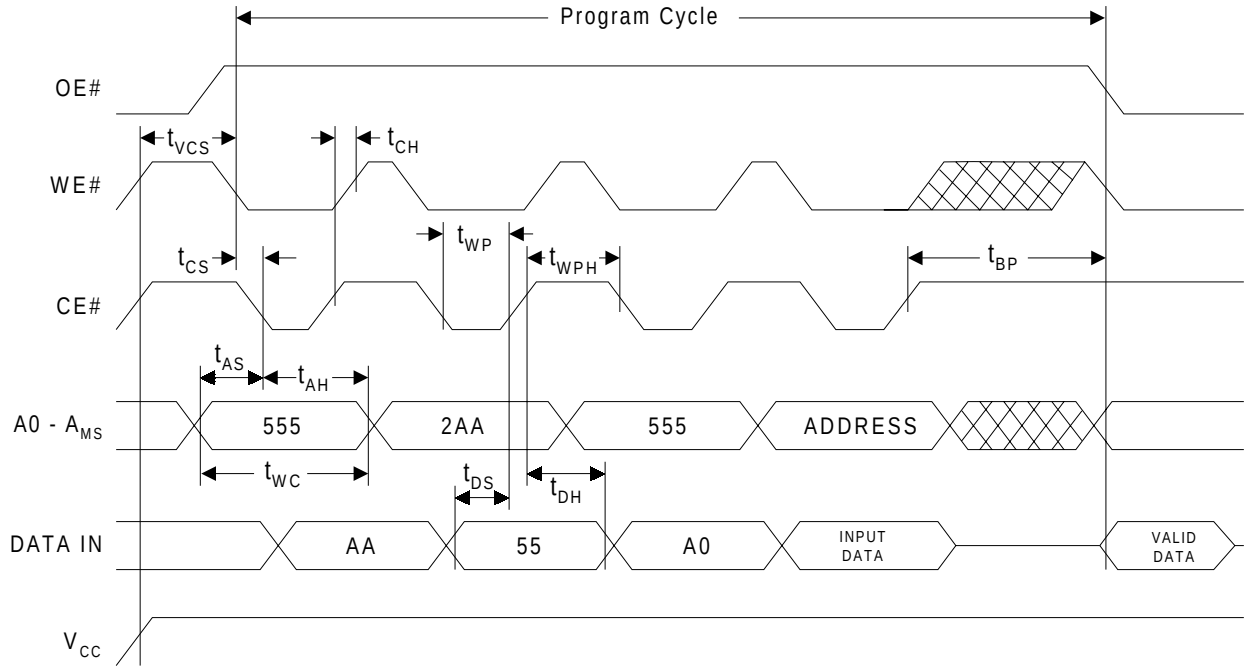
Symbol	Parameter	Pm39LV512-55 Pm39LV010-55 Pm39LV020-55 Pm39LV040-55		Pm39LV512-70 Pm39LV010-70 Pm39LV020-70 Pm39LV040-70		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	55		70		ns
t_{AS}	Address Set-up Time	0		0		ns
t_{AH}	Address Hold Time	30		30		ns
t_{CS}	CE# and WE# Set-up Time	0		0		ns
t_{CH}	CE# and WE# Hold Time	0		0		ns
t_{OEH}	OE# High Hold Time	10		10		ns
t_{DS}	Data Set-up Time	40		40		ns
t_{DH}	Data Hold Time	0		0		ns
t_{WP}	Write Pulse Width	35		35		ns
t_{WPH}	Write Pulse Width High	20		20		ns
t_{BP}	Byte Programming Time		20		20	µs
t_{EC}	Chip or Block Erase Time		100		100	ms
t_{VCS}	V_{CC} Set-up Time	50		50		µs

PROGRAM OPERATIONS AC WAVEFORMS - WE# CONTROLLED

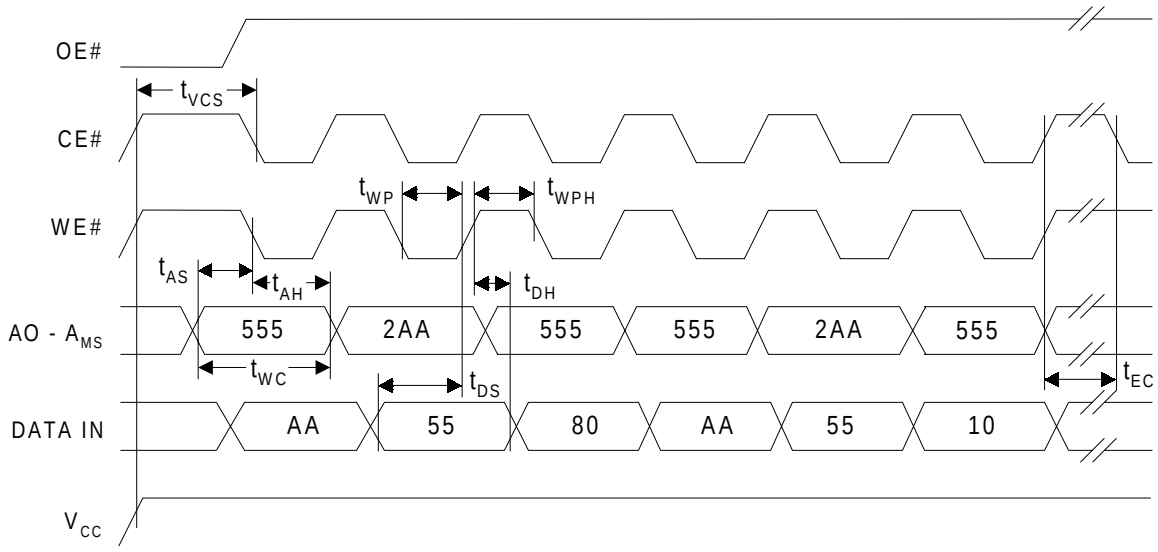


AC CHARACTERISTICS (CONTINUED)

PROGRAM OPERATIONS AC WAVEFORMS - CE# CONTROLLED

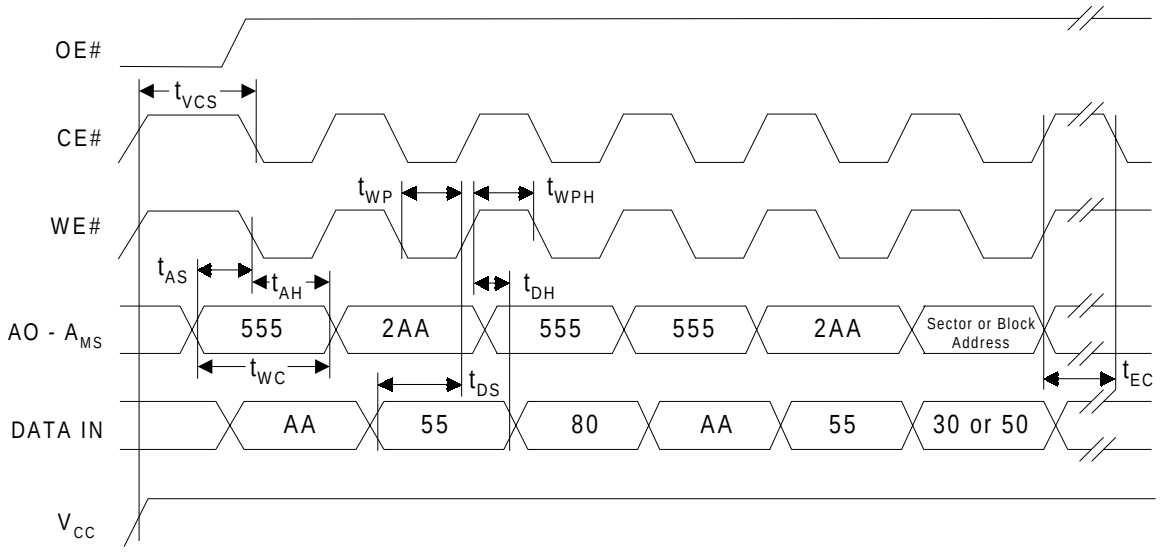


CHIP ERASE OPERATIONS AC WAVEFORMS

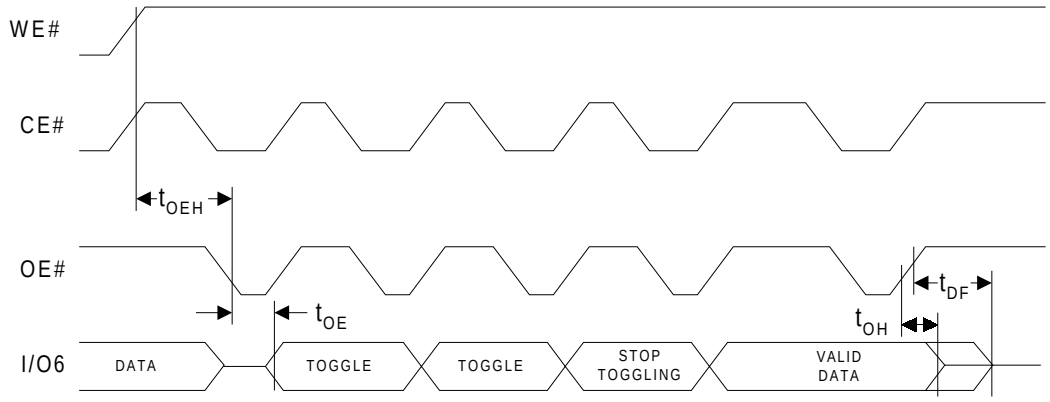


AC CHARACTERISTICS (CONTINUED)

SECTOR OR BLOCK ERASE OPERATIONS AC WAVEFORMS



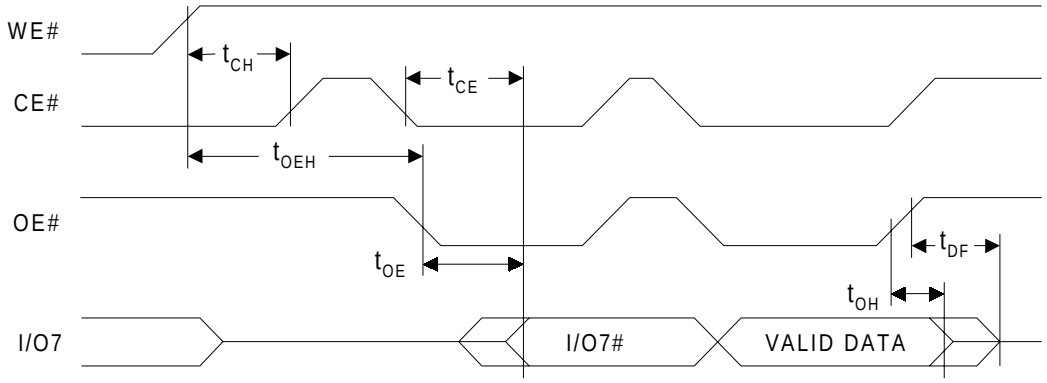
TOGGLE BIT AC WAVEFORMS



Note: Toggling CE#, OE#, or both OE# and CE# will operate Toggle Bit.

AC CHARACTERISTICS (CONTINUED)

DATA# POLLING AC WAVEFORMS



Note: Toggling CE#, OE#, or both OE# and CE# will operate Data# Polling.

PROGRAM/ERASE PERFORMANCE

Parameter	Unit	Typ	Max	Remarks
Sector Erase Time	ms	55	100	From writing erase command to erase completion
Block Erase Time	ms	55	100	From writing erase command to erase completion
Chip Erase Time	ms	55	100	From writing erase command to erase completion
Byte Programming Time	µs	16	20	Excludes the time of four-cycle program command execution

Note: These parameters are characterized but not 100% tested.

RELIABILITY CHARACTERISTICS (1)

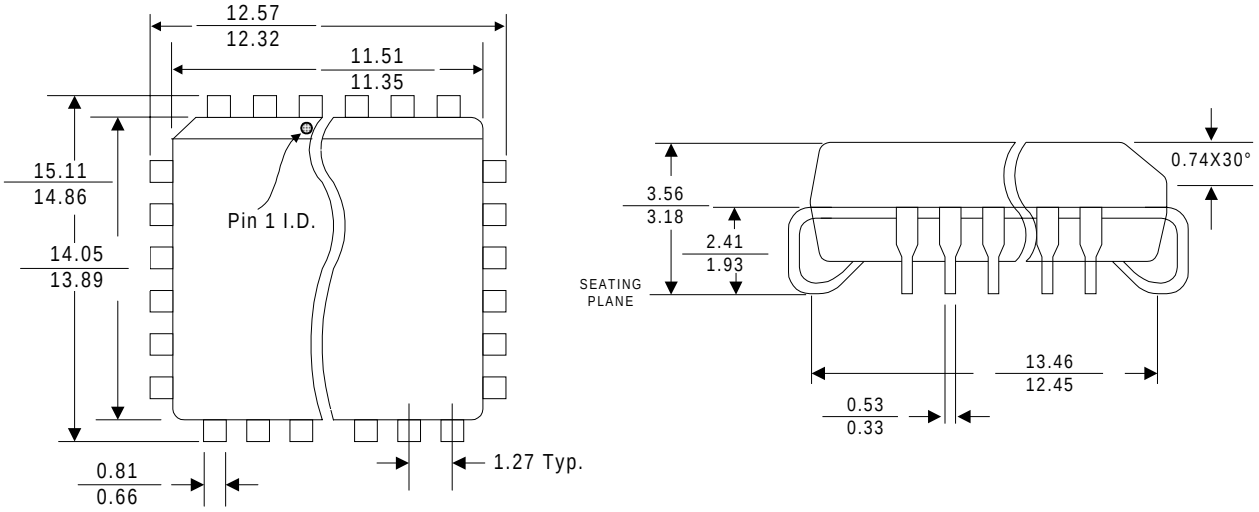
Parameter	Min	Typ	Unit	Test Method
Endurance	100,000 (2)		Cycles	JEDEC Standard A117
Data Retention	20		Years	JEDEC Standard A103
ESD - Human Body Model	2,000		Volts	JEDEC Standard A114
ESD - Machine Model	200		Volts	JEDEC Standard A115
Latch-Up	100 + I_{CC1}		mA	JEDEC Standard 78

Note: 1. These parameters are characterized but not 100% tested.
2. Preliminary specification only and will be formalized after cycling qualification test.

PACKAGE TYPE INFORMATION

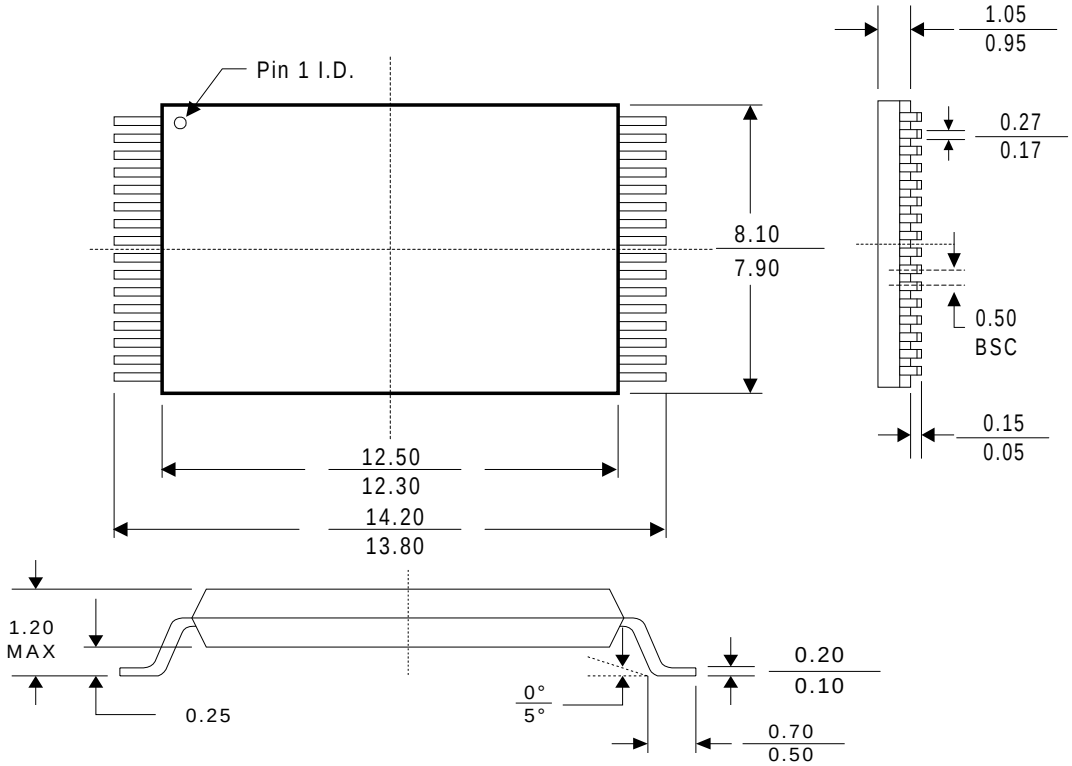
32J

32-Pin Plastic Leaded Chip Carrier Dimensions in Inches (Millimeters)



32V

32-Pin Thin Small Outline Package (VSOP - 8 mm x 14 mm)(measure in millimeters)



REVISION HISTORY

Date	Revision No.	Description of Changes	Page No.
May, 2003	1.0	Preliminary Information	All
September, 2003	1.1	Updated program description and formal release	5
December, 2003	1.2	Added Lead-free package option	1, 3, 12
		Upgraded guranteed program/erase cycles from 50,000 to 100,000 (preliminary)	1, 18
		Revised output test load as 30 pF for all speed	14
		Revised package dimension information	19
March, 2004	1.3	Extend the operation range of temperature	All
June, 2005	1.4	Improve tBP (max) from 30us to 20us	15, 18
March, 2006	1.5	Change Logo and company name	All
April, 2006	1.6	Correct logo for some description	3, 5