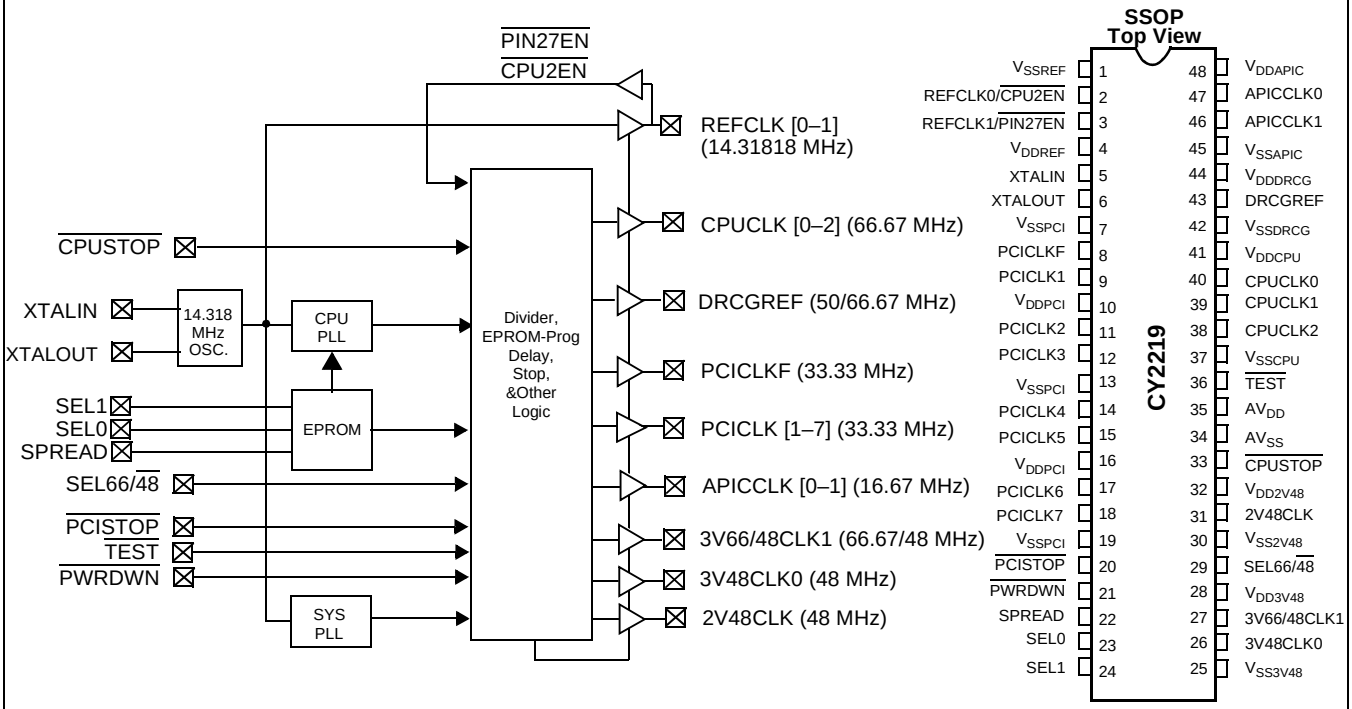
CY2219

Spread Spectrum Frequency Timing Generator for Integrated CPU

Features	Benefits
• **Mixed 2.5V and 3.3V operation**	Supports Intel® Timna processors with integrated graphics and memory controllers
• **Multiple output clocks at different frequencies** — **Three CPU clocks at 66 MHz** — **Eight PCI clocks at 33 MHz, 1 free-running** — **One DRCG reference clock at 50 or 66 MHz** — **Two synchronous APIC clocks at 16.67 MHz** — **One 3.3V clock selectable between 66 or 48 MHz** — **One 3.3V and one 2.5V clock at 48 MHz** — **Two reference clocks at 14.318 MHz**	Single-chip main motherboard clock generator — Support for CPU and chipset — Support for multiple PCI slots and chipset — Drives one main memory clock generator, including DRCG (134S) — Supports USB frequencies and I/O chip
• **Spread Spectrum clocking** — **31 kHz modulation frequency** — **EPROM programmable percentage of spreading. Default is –0.6%, which is recommended by Intel®**	Enables reduction of EMI
• **Two Frequency Select inputs**	Supports up to four CPU clock frequencies
• **Low skew and low jitter outputs**	Meet-tight system timing requirements at high frequency
• **OE and Test Mode support**	Enables ATE and “bed of nails” testing
• **48-pin SSOP package**	Widely available, standard package enables lower cost

Logic Block Diagram



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Pin Summary[1]

Name	Pins	Description
V_{SSREF}	1	3.3V Reference ground
V_{DDREF}	4	3.3V Reference voltage supply
V_{SSPCI}	7, 13, 19	3.3V PCI ground
V_{DDPCI}	10, 16	3.3V PCI voltage supply
V_{SS3V48}	25	3.3V 66/48M ground
V_{DD3V48}	28	3.3V 66/48M voltage supply
V_{SS2V48}	30	2.5V 48M ground
V_{DD2V48}	32	2.5V 48M voltage supply
V_{SSCPU}	37	2.5V CPU ground
V_{DDCPU}	41	2.5V CPU voltage supply
V_{SSDRCG}	42	2.5V DRCG ground
V_{DDDRCG}	44	2.5V DRCG voltage supply
V_{SSAPIC}	45	2.5V APIC ground
V_{DDAPIC}	48	2.5V APIC voltage supply
AV_{SS}	34	Analog ground for PLL and Core
AV_{DD}	35	Analog voltage supply for PLL and Core
XTALIN[1]	5	Reference crystal input
XTALOUT[1]	6	Reference crystal feedback
CPUCLK [0–2]	38, 39, 40	CPU clock outputs
APIC[0-1]	46, 47	APIC clock output
PCICLK [1–7]	9, 11, 12, 14, 15, 17, 18	PCI clock outputs, synchronously running at 33.33 MHz
PCICLKF	8	Free running PCI clock
DRCGREF	43	DRCG clock output, drive memory clock generator
3V48CLK0	26	3.3V 48-MHz clock
3V66/48CLK1	27	3.3V 48-/66.67-MHz clock selectable by pin 29, enabled by pin 3
2V48CLK	31	2.5V 48-MHz clock
REFCLK0/$\overline{\text{CPU2EN}}$	2	Reference clock output, 14.318 MHz; Latched input with internal pull-up; HIGH = CPUCLK2 three-stated (no external component required); LOW = CPUCLK2 running (external 10k or smaller resistor from Pin 2 to board ground required)
REFCLK1/$\overline{\text{PIN27EN}}$	3	Reference clock output, 14.318 MHz; Latched input with internal pull-up; HIGH = 3V66/48CLK1 three-stated (no external component required); LOW = 3V66/48CLK1 running (external 10k or smaller resistor from Pin 3 to board ground required)
CPUSTOP	33	Active LOW input, disables CPU clocks when asserted
PCISTOP	20	Active LOW input, disables PCI clocks when asserted
PWRDWN	21	Active LOW input, powers down part when asserted
TEST	36	Active LOW input, enables vendor test mode when asserted; (HIGH = NORMAL MODE, LOW = VENDOR TEST MODE)
SPREAD	22	Active HIGH input, enables spread spectrum when asserted
SEL1	24	CPU frequency select input (See Function Table)
SEL0	23	CPU frequency select input (See Function Table)
SEL66/$\overline{48}$	29	3V66/48CLK1 frequency select input; (HIGH = 66.67 MHz, LOW = 48 MHz)

Note:
1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF. For crystals with different C_{LOAD}, please refer to the appnote, “Crystal Oscillator Topics.”

Function Table[2]

SEL66/48	SEL1	SEL0	CPUCLK (MHz)	DRCGREF (MHz)	3V66/48CLK (MHz)	PCICLK (MHz)	2/3V48CLK (MHz)	REFCLK (MHz)	APICCLK (MHz)
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	0	1	66.67	50	48	33.33	48	14.318	16.67
0	1	0	TCLK/3	TCLK/4	TCLK/2	TCLK/6	TCLK/2	TCLK	TCLK/12
0	1	1	66.67	66.67	48	33.33	48	14.318	16.67
1	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	1	66.67	50	66.67	33.33	48	14.318	16.67
1	1	0	TCLK/3	TCLK/4	TCLK/3	TCLK/6	TCLK/2	TCLK	TCLK/12
1	1	1	66.67	66.67	66.67	33.33	48	14.318	16.67

Actual Clock Frequency Values

Target Frequency (MHz)	Actual Frequency (MHz)	PPM
14.31818	14.31818	0
16.67	16.506	–8741
33.33	33.042	–8741
50.0	49.716	–8741
66.67	66.084	–8741
48.0	48.008	167

Clock Enable Configuration

PWRDWN	CPUSTOP	PCISTOP	CPU2	CPU1 CPU0	DRCG	3V66/ 48	PCI	PCIF	3V48 2V48	APIC	REF	XTAL	VCO
0	X	X	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	0	0	LOW	LOW	ON	ON	LOW	ON	ON	ON	ON	ON	ON
1	0	1	LOW	LOW	ON	ON	ON	ON	ON	ON	ON	ON	ON
1	1	0	ON	ON	ON	ON	LOW	ON	ON	ON	ON	ON	ON
1	1	1	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON

PIN27EN (latched at power up)	CPU2EN (latched at power up)	CPU2	3V66/48
0	0	ON	ON
0	1	ON	Hi-Z
1	0	Hi-Z	ON
1	1	Hi-Z	Hi-Z

Clock Driver Impedances

Buffer Name	V_{DD} Range	Buffer Type	Minimum (Ω)	Typical (Ω)	Maximum (Ω)
CPU,DRCG,APIC,2V48	2.375–2.625	Type 1	13.5	29	45
REF, 3V48, 3V66/48	3.135–3.465	Type 3	20	40	60
PCI	3.135–3.465	Type 5	12	30	55

2. TCLK is a test clock driven in on the XTALIN input in test mode.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5 to +7.0V

Input Voltage ..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ..... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Core VDD Minimum Ramp Rate ..... 0.06 V/ms

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2000V

Operating Conditions Over which Electrical Parameters are Guaranteed

Parameter	Description	Min	Max	Unit
V_{DDREF}, V_{DDPCI}, AV_{DD}, V_{DD3V48}, V_{DDUSB}	3.3V Supply Voltages	3.135	3.465	V
V_{DDCPU}, V_{DDDRCG}, V_{DDAPIC}, V_{DD2V48}	2.5V Supply Voltages	2.375	2.625	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on: CPU, DRCG, APIC, 2V48, 3V48, 3V66/48, REF PCI	 10 10	 20 30	 pF pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min	Max	Unit
V_{IH}	High-level Input Voltage	Except XIN and SEL0. Threshold voltage for XIN = $V_{DD}/2$		2.0		V
V_{IL}	Low-level Input Voltage	Except XIN and SEL0. Threshold voltage for XIN = $V_{DD}/2$			0.8	V
V_{IHSEL0}	High-level Input Voltage			70%		V_{DD}
V_{ILSEL0}	Low-level Input Voltage				30%	V_{DD}
V_{OH}	High-level Output Voltage	CPU, DRCG, APIC, 2V48	I_{OH} = –1 mA	2.0		V
		PCI, 3V66/48, 3V48, REF	I_{OH} = –1 mA	2.4		
V_{OL}	Low-level Output Voltage	CPU, DRCG, APIC, 2V48	I_{OL} = 1 mA		0.4	V
		PCI, 3V66/48, 3V48, REF	I_{OL} = 1 mA		0.4	
I_{IH}	Input High Current	$0 \le V_{IN} \le V_{DD}$			10	µA
I_{IL}	Input Low Current	$0 \le V_{IN} \le V_{DD}$			10	µA
I_{OH}	High-level Output Current	CPU, DRCG, APIC, 2V48	V_{OH} = 2.0V	–12	–59	mA
		3V48, 3V66/48, REF	V_{OH} = 2.4V	–16	–63	
		PCI	V_{OH} = 2.4V	–15	–100	
I_{OL}	Low-level Output Current	CPU, DRCG, APIC, 2V48	V_{OL} = 0.4V	12	40	mA
		3V48, 3V66/48, REF	V_{OL} = 0.4V	9	27	
		PCI	V_{OL} = 0.4V	10	38	
I_{OZ}	Output Leakage Current	Three-state			10	µA
I_{DD2}	2.5V Power Supply Current	AV_{DD}/V_{DD33} = 3.465V, V_{DD25} = 2.625V			50	mA
I_{DD3}	3.3V Power Supply Current	AV_{DD}/V_{DD33} = 3.465V, V_{DD25} = 2.625V			135	mA
I_{DDPD2}	2.5V Shutdown Current	AV_{DD}/V_{DD33} = 3.465V, V_{DD25} = 2.625V			100	µA
I_{DDPD3}	3.3V Shutdown Current	AV_{DD}/V_{DDQ3} = 3.465V, V_{DD25} = 2.625V			200	µA

Switching Characteristics[3] Over the Operating Range

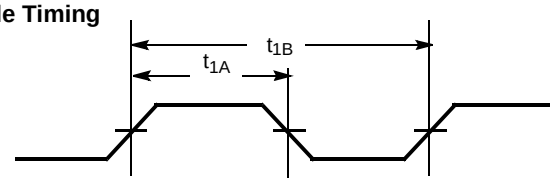
Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_1	All	Output Duty Cycle[4]	t_{1A}/t_{1B}	45	55	%
t_2	CPU	Rising Edge Rate	Between 0.8V and 1.8V	1.0	4.0	V/ns
	DRCG, APIC, 2V48	Rising Edge Rate	Between 0.4V and 2.0V	1.0	4.0	V/ns
	3V66/48, 3V48, REF	Rising Edge Rate	Between 0.4V and 2.4V	0.5	2.0	V/ns
	PCI	Rising Edge Rate	Between 0.8V and 2.2V	1.0	4.0	V/ns
t_3	CPU	Falling Edge Rate	Between 1.8V and 0.8V	1.0	4.0	V/ns
	DRCG, APIC, 2V48	Falling Edge Rate	Between 2.0V and 0.4V	1.0	4.0	V/ns
	3V66/48, 3V48, REF	Falling Edge Rate	Between 2.4V and 0.4V	0.5	2.0	V/ns
	PCI	Falling Edge Rate	Between 2.2V and 0.8V	1.0	4.0	V/ns
t_4	CPU	CPU-CPU Skew	Measured at 1.25V		175	ps
t_5	APIC	APIC-APIC Skew	Measured at 1.25V		250	ps
t_6	PCI	PCI-PCI Skew	Measured at 1.5V		500	ps
t_7	CPU, PCI	CPU-PCI Group Offset	CPU leads. Measured at 1.5V	1.5	3.5	ns
t_8	CPU, APIC	CPU-APIC Group Offset	CPU leads. Measured at 1.25V	1.5	3.5	ns
	CPU	Cycle-Cycle Clock Jitter			250	ps
	DRCG	Cycle-Cycle Clock Jitter	Measured at 66 MHz		250	ps
	2V48	Cycle-Cycle Clock Jitter			250	ps
	3V66/3V48	Cycle-Cycle Clock Jitter	Configured as 48 MHz output		500	ps
	3V66/3V48	Cycle-Cycle Clock Jitter	Configured as 66 MHz output		550	ps
	PCI	Cycle-Cycle Clock Jitter			500	ps
	APIC	Cycle-Cycle Clock Jitter			500	ps
	REF	Cycle-Cycle Clock Jitter			1000	ps
	All Outputs	Settle Time	Clock stabilization from power-up		3	ms

Notes:

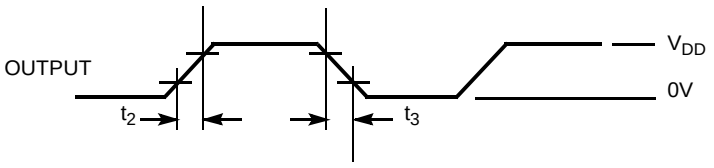
3. All parameters specified with loaded outputs.
4. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.

Switching Waveforms

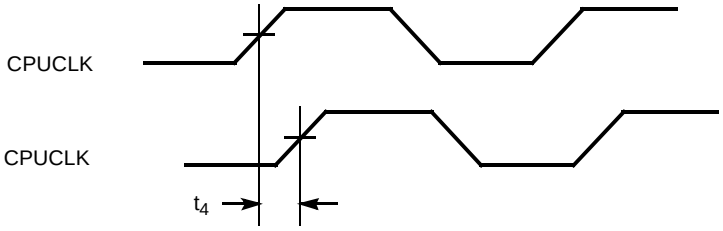
Duty Cycle Timing



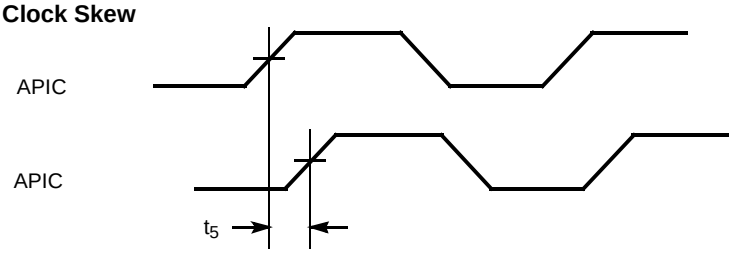
All Outputs Rise/Fall Time



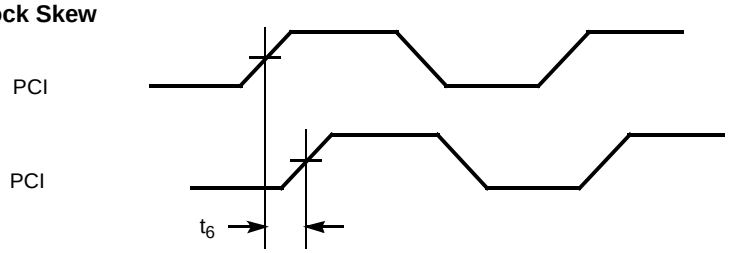
CPU-CPU Clock Skew



APIC-APIC Clock Skew

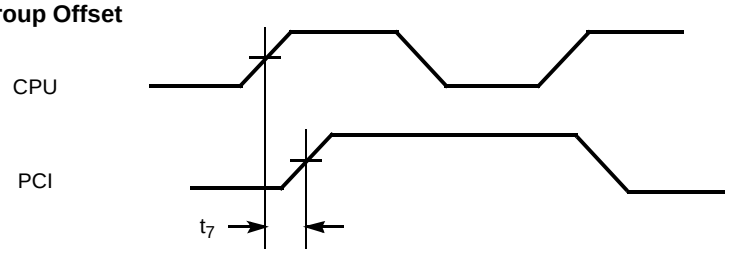


PCI-PCI Clock Skew

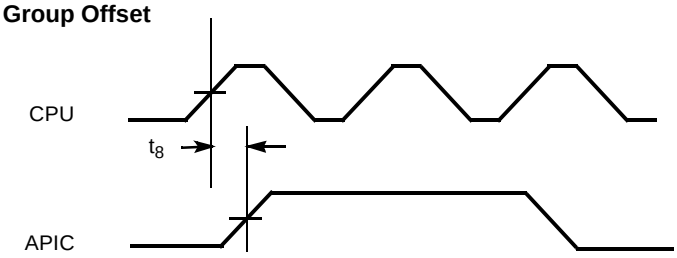


Switching Waveforms (continued)

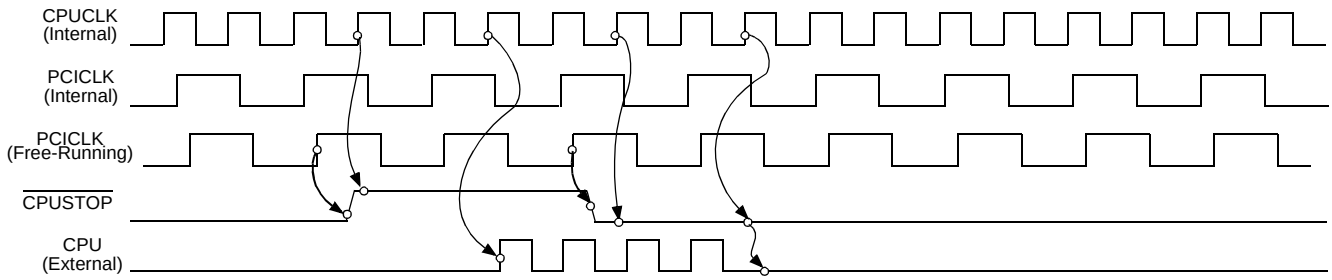
CPU-PCI Group Offset



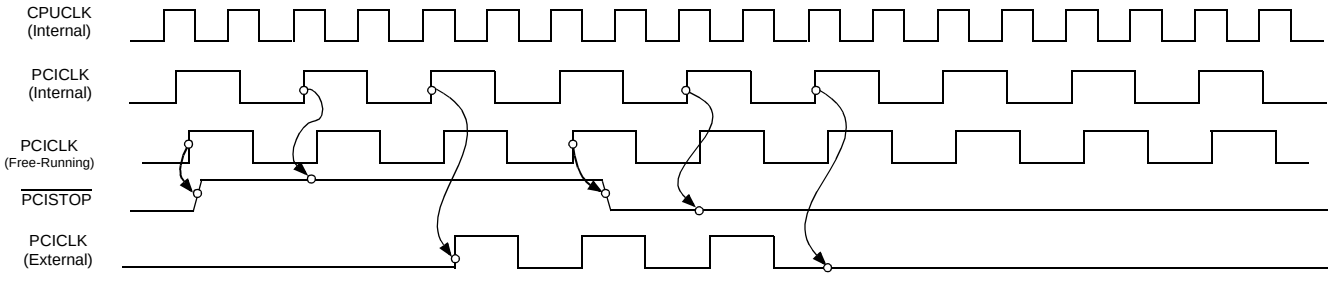
CPU-APIC Group Offset



$\overline{\text{CPUSTOP}}$ Timing [5, 6]



$\overline{\text{PCISTOP}}$ Timing

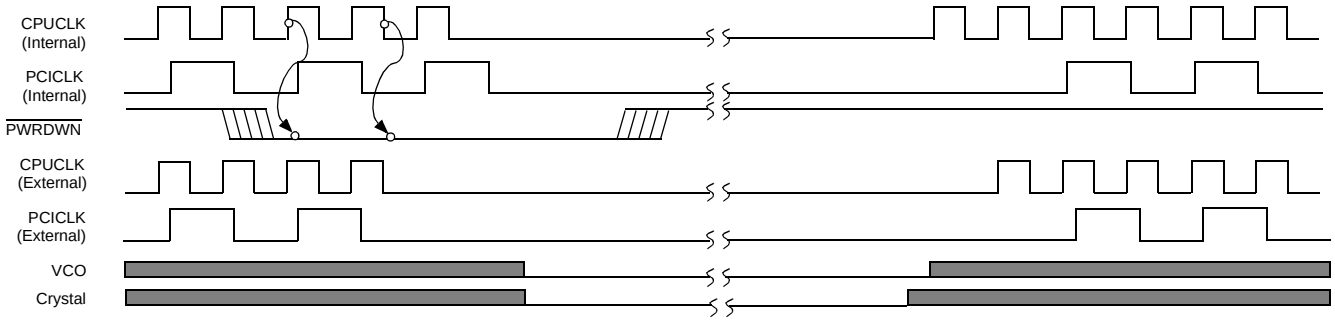


Notes:

5. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
6. CPUSTOP, PCISTOP and PWRDWN may be applied asynchronously. They are synchronized internally.

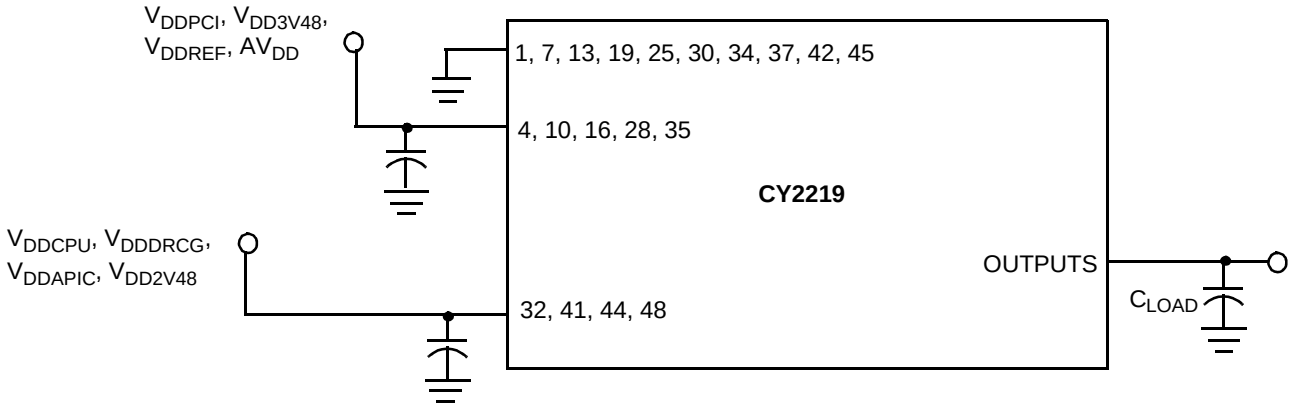
Switching Waveforms (continued)

$\overline{\text{PWRDWN}}$ Timing



Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Test Circuit



Note: Each supply pin must have an individual decoupling capacitor.

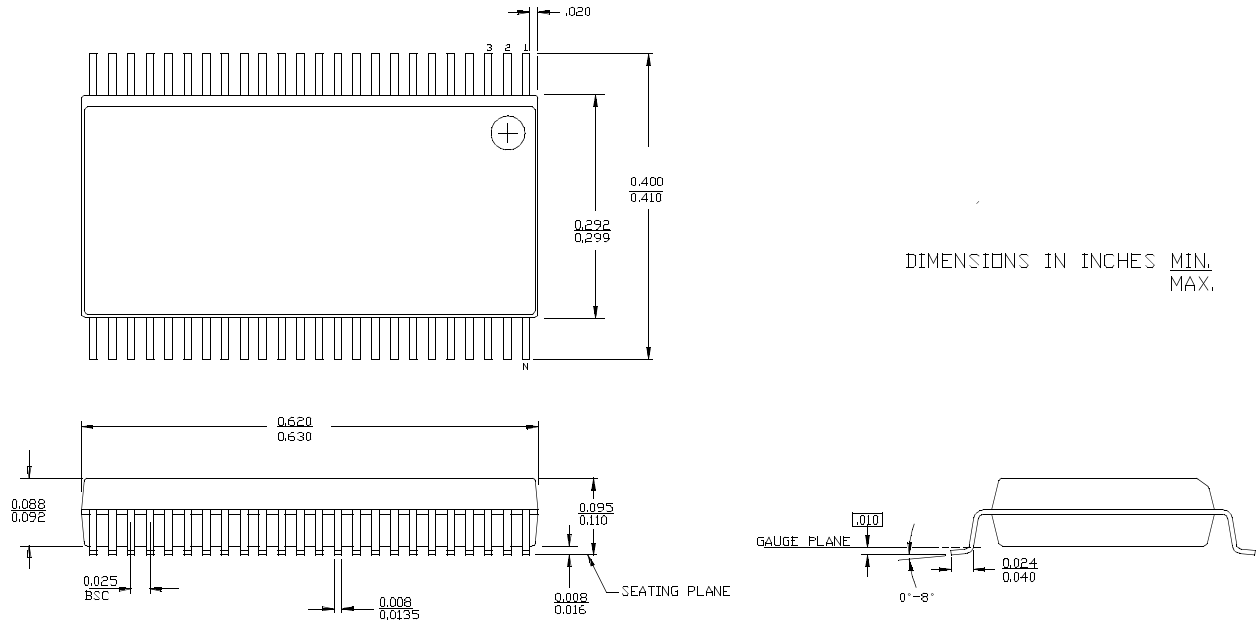
Note: All capacitors must be placed as close to the pins as is physically possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2219PVC–1	O48	48-Pin SSOP	Commercial

Package Diagram

48-Lead Shrunk Small Outline Package O48



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Document Title: CY2219 Spread Spectrum Frequency Timing Generator for Integrated CPU Document Number: 38-07213				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110346	11/11/01	SZV	Change from Spec number: 38-00863 to 38-07213