



Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BUS TRANSCEIVER/ REGISTERS

IDT54/74FCT163646/A/C

FEATURES:

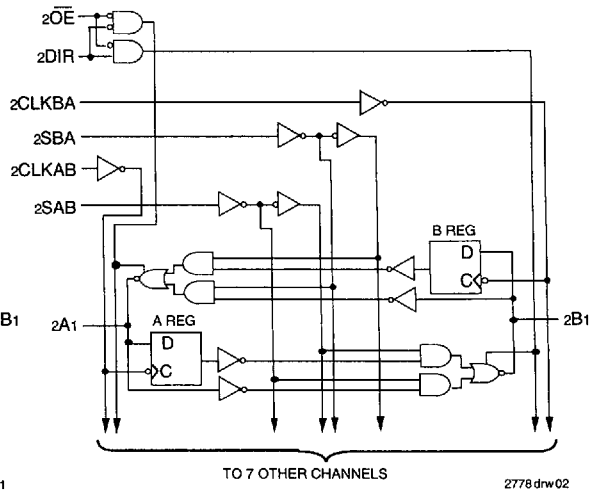
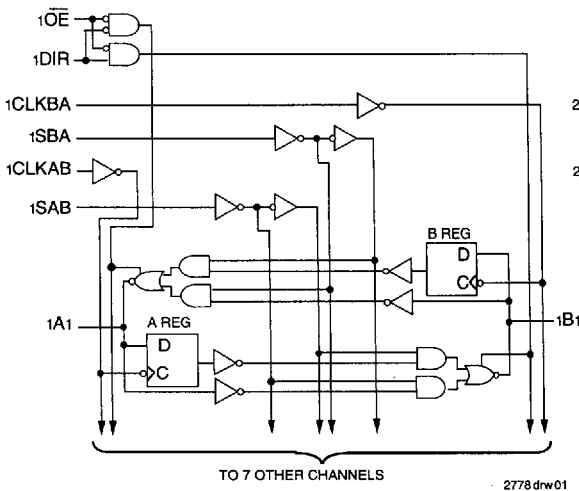
- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

The FCT163646/A/C 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (xDIR), over-riding Output Enable control (xOE) and Select lines (xSAB and xSBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the LOW-to-HIGH transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT163646/A/C have series current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times-reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 1996

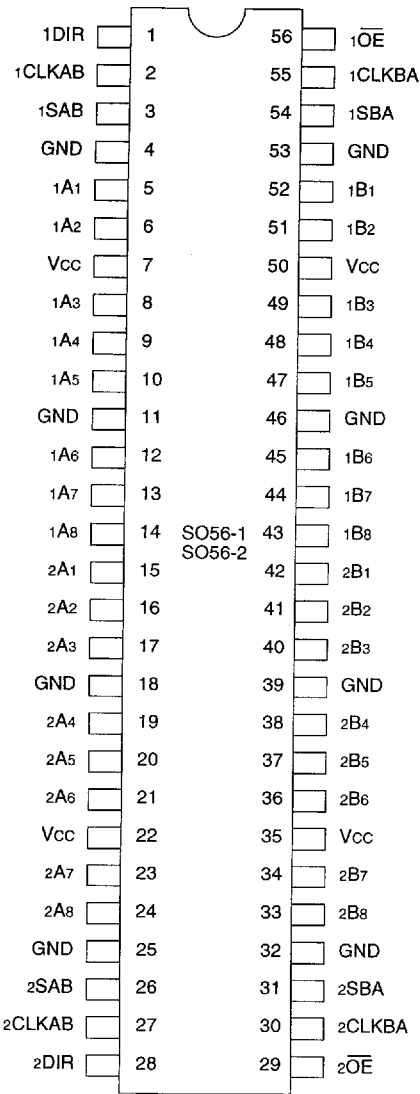
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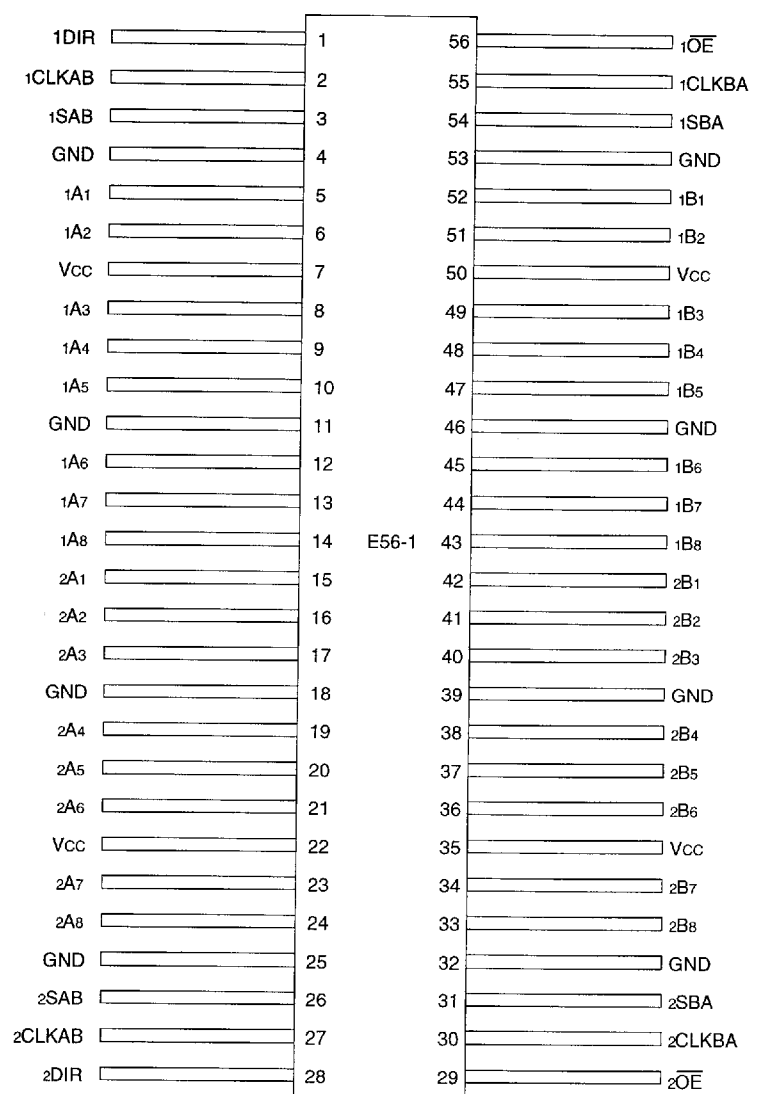
4825771 0023326 5T7

PIN CONFIGURATIONS



**SSOP
TSSOP
TOP VIEW**

2778 drw03



**CERPACK
TOP VIEW**

2778 drw04

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCAB, xCBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xDIR, xOE	Output Enable Inputs

2778 tbl 01

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6.0	pF
Ci/O	I/O Capacitance	VOUT = 0V	3.5	8.0	pF

NOTE: 2778 Ink 04

1. This parameter is measured at characterization but not tested.

FUNCTION TABLE(2)

Inputs						Data I/O(1)		Operation or Function
xOE	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

2778 tbl 02

NOTES:

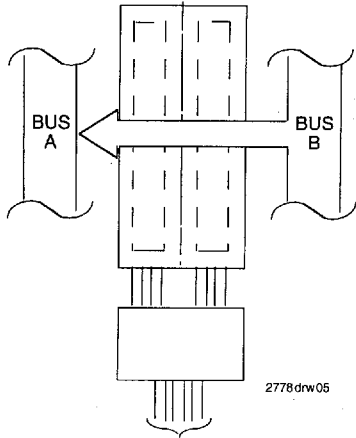
- The data output functions may be enabled or disabled by various signals at the xOE or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	-0.5 to +4.6	V
VTERM(3)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM(4)	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	-0.5 to Vcc + 0.5	V
TA	Operating Temperature	-40 to +85	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	-60 to +60	-60 to +60	mA

2778 Ink 03

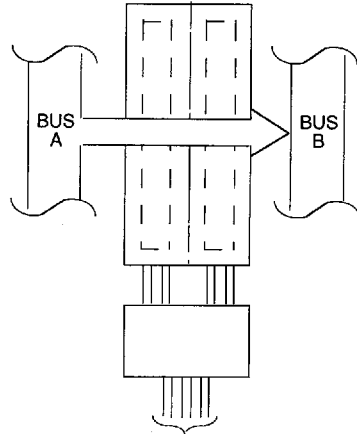
- NOTES:**
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 - Vcc terminals.
 - Input terminals.
 - Output and I/O terminals.



2778drw05

xDIR	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

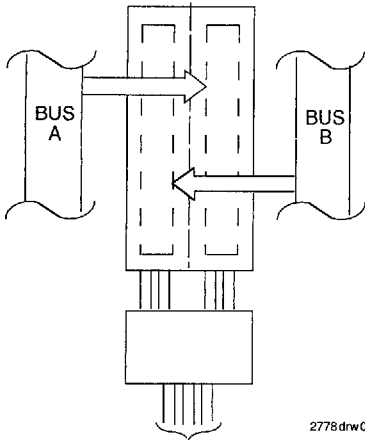
REAL-TIME TRANSFER
 BUS B TO A



2778drw06

xDIR	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

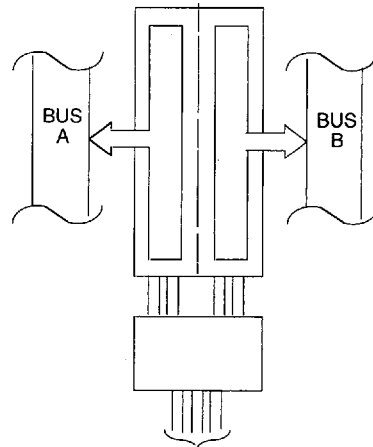
REAL-TIME TRANSFER
 BUS A TO B



2778drw07

xDIR	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

STORAGE FROM
 A AND/OR B



2778 drw 08

xDIR ⁽¹⁾	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

TRANSFER STORED
 DATA TO A AND/OR B

NOTE:

1. Cannot transfer data to A bus and B bus simultaneously.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, Vcc = 2.7V to 3.6V; Military: TA = -55°C to +125°C, Vcc = 2.7V to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
VIH	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	Vcc+0.5	
VIL	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins) ⁽⁶⁾	Vcc = Max.	VI = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins) ⁽⁶⁾		VI = Vcc	—	—	±1	
IIL	Input LOW Current (Input pins) ⁽⁶⁾		VI = GND	—	—	±1	
	Input LOW Current (I/O pins) ⁽⁶⁾		VI = GND	—	—	±1	
IOZH	High Impedance Output Current (3-State Output pins) ⁽⁶⁾	Vcc = Max.	VO = Vcc	—	—	±1	µA
			VO = GND	—	—	±1	
VIK	Clamp Diode Voltage	Vcc = Min., IIN = -18mA		—	-0.7	-1.2	V
IODH	Output HIGH Current	Vcc = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		-36	-60	-110	mA
IODL	Output LOW Current	Vcc = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		50	90	200	mA
VOH	Output HIGH Voltage	Vcc = Min. VIN = VIH or VIL	IOH = -0.1mA	Vcc-0.2	—	—	V
			IOH = -3mA	2.4	3.0	—	
		Vcc = 3.0V VIN = VIH or VIL	IOH = -6mA MIL.	2.4 ⁽⁵⁾	3.0	—	
			IOH = -8mA COM'L.	—	—	—	
VOL	Output LOW Voltage	Vcc = Min. VIN = VIH or VIL	IOL = 0.1mA	—	—	0.2	V
			IOL = 16mA	—	0.2	0.4	
			IOL = 24mA	—	0.3	0.55	
		Vcc = 3.0V VIN = VIH or VIL	IOL = 24mA	—	0.3	0.50	
IOS	Short Circuit Current ⁽⁴⁾	Vcc = Max., VO = GND ⁽³⁾		-60	-135	-240	mA
VH	Input Hysteresis	—		—	150	—	mV
ICCL ICCH ICCZ	Quiescent Power Supply Current	Vcc = Max., VIN = GND or Vcc	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = Vcc - 0.6V at rated current.
- The test limit for this parameter is ±5µA at TA = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	VCC = Max.	VIN = VCC - 0.6V ⁽³⁾	—	2.0	30	μA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	VCC = Max. Outputs Open xDIR = xOE = GND 50% Duty Cycle One Input Toggling	VIN = VCC VIN = GND	—	60	100	μA / MHz
I _C	Total Power Supply Current ⁽⁶⁾	VCC = Max. Outputs Open f _{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = xOE = GND fi = 5MHz 50% Duty Cycle One Bit Toggling	VIN = VCC VIN = GND	—	0.6	1.0	mA
			VIN = VCC - 0.6V VIN = GND	—	0.6	1.0	
		VCC = Max. Outputs Open f _{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = xOE = GND fi = 2.5MHz 50% Duty Cycle Sixteen Bits Toggling	VIN = VCC VIN = GND	—	3.0	5.0 ⁽⁵⁾	
			VIN = VCC - 0.6V VIN = GND	—	3.0	5.3 ⁽⁵⁾	

2778 tbl 06

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at VCC or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
 ΔI_{CC} = Power Supply Current for a TTL High Input
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{CP} = Number of Clock Inputs at f_{CP}
 f_i = Input Frequency
 N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽⁴⁾

Symbol	Parameter	Condition ⁽¹⁾	FCT163646				FCT163646A				FCT163646C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	5.4	—	—	ns
tPZH tPZL	Output Enable Time xDIR or xOE to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	1.5	7.8	—	—	ns
tPHZ tPLZ	Output Disable Time xDIR or xOE to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	6.3	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	1.5	5.7	—	—	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	1.5	6.2	—	—	ns
tsu	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	2.0	—	—	—	ns
th	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	—	—	ns
tw	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	—	—	ns
tSK(o)	Output Skew ⁽³⁾			—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—

2778 tbl 07

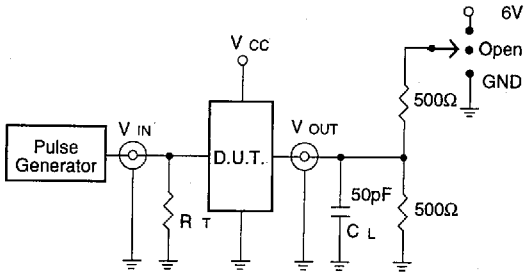
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ± 0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.



TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2778 drw 09

SWITCH POSITION

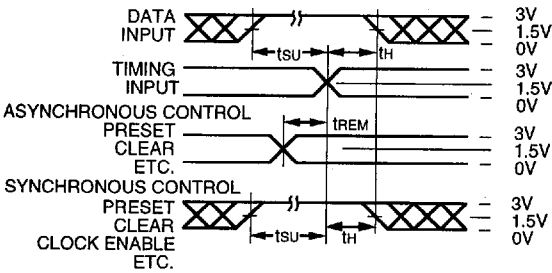
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to Z_{out} of the Pulse Generator.

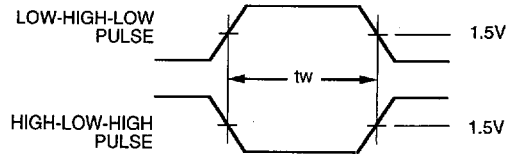
2778 Ink 08

SET-UP, HOLD AND RELEASE TIMES



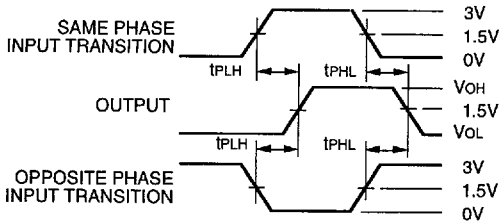
2778 drw 10

PULSE WIDTH



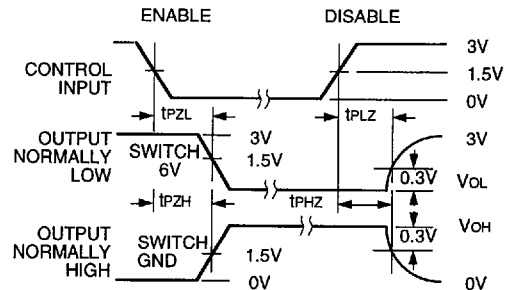
2778 drw 11

PROPAGATION DELAY



2778 drw 12

ENABLE AND DISABLE TIMES



2778 drw 13

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; th ≤ 2.5ns.
3. If Vcc is below 3V, input voltage swings should be adjusted not to exceed Vcc.

ORDERING INFORMATION

IDT	XX	FCT	XXXX	X	X	
Temp. Range		Device Type		Package	Process	
					Blank B	Commercial MIL-STD-883, Class B
					PV PA E	Shrink Small Outline Package (SO56-1) Thin Shrink Small Outline Package (SO56-2) CERPACK (E56-1)
					163646 163646A 163646C	Non-Inverting 16-Bit Transceiver/ Register
					54 74	-55°C to +125°C -40°C to +85°C

2778drw14

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