

# LOW EMI CLOCK GENERATOR

# MK1726-01A

## Description

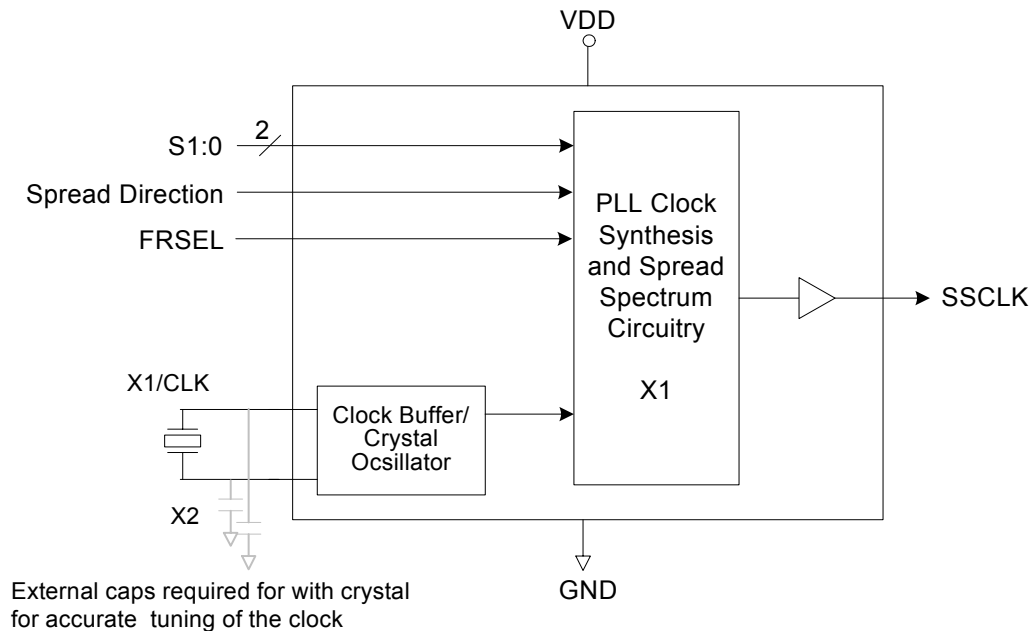
The MK1726-01A generates a low EMI output clock from a clock or crystal input. The part is designed to dither the LCD interface clock for PDAs, printers, scanners, modems, copiers, and others. Using ICS' proprietary mix of analog and digital Phase-Locked Loop (PLL) technology, the device spreads the frequency spectrum of the output, reducing the frequency amplitude peaks by several dB. The MK1726-01A offers both centered and down spread from a high-speed clock input.

ICS offers many other clocks for computers and computer peripherals. Consult us when you need to remove crystals and oscillators from your board.

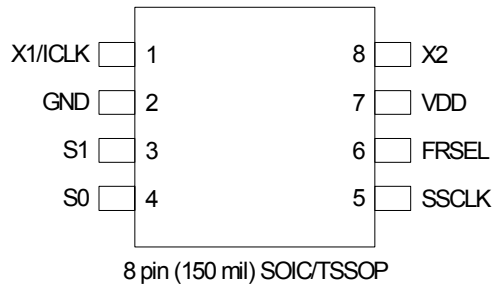
## Features

- Packaged in 8-pin SOIC/TSSOP
- Provides a spread spectrum output clock
- Supports flat panel controllers
- Accepts a clock or crystal input (provides same frequency dithered output)
- Input frequency range of 4 to 32 MHz
- Output frequency range of 4 to 32 MHz
- Center and down spread
- Peak reduction by 8 dB to 16 dB typical on 3rd through 19th odd harmonics
- Low EMI feature can be disabled
- Includes power down
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process

## Block Diagram



## Pin Assignment



## Spread Direction and Percentage Select Table

S1 Pin 3	S0 Pin 4	Spread Direction	Spread Percentage
0	0	Center	±1.4
0	M	Center	±1.1
0	1	Center	±0.6
M	0	Center	±0.5
M	M	No Spread	-
M	1	Down	-1.6
1	0	Down	-2.0
1	M	Down	-0.7
1	1	Down	-3.0

FRSEL (pin 6)	Input Freq. Range	Multiplier	Output Freq. Range
0	4.0 to 8.0 MHz	X1	4.0 to 8.0 MHz
1	8.0 to 16.0MHz	X1	8.0 to 16.0MHz
M	16.0 to 32.0MHz	X1	16.0 to 32.0MHz

0 = connect to GND  
M = unconnected (floating)  
1 = connect directly to VDD

## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	Input	Connect to a 4 to 32 MHz crystal or clock.
2	GND	Power	Connect to ground.
3	S1	Input	Function select 1 input. Selects spread amount and direction per table above. (default-internal mid-level).
4	S0	Input	Function select 0 input. Selects spread amount and direction per table above. (default-internal mid-level).
5	SSCLK	Output	Clock output with Spread spectrum
6	FRSEL	Input	Function select for input frequency range. Default to mid level "M".
7	VDD	Power	Connect to +3.3 V.
8	X2	XO	Crystal connection to a 4 to 32 MHz crystal. Leave unconnected for clock

## External Components

The MK1726-01A requires a minimum number of external components for proper operation.

### Decoupling Capacitor

A decoupling capacitor of 0.01 $\mu$ F must be connected between VDD and GND on pins 7 and 2, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

### Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50 $\Omega$  trace (a commonly used trace impedance) place a 33 $\Omega$  resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 $\Omega$ .

### Tri-level Select Pin Operation

The S1, S0 select pins are tri-level, meaning they have three separate states to make the selections shown in the table on page 2. To select the M (mid) level, the connection to these pins must be eliminated by either floating them originally, or tri-stating the GPIO pins which drive the select pins.

## PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01 $\mu$ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 33 $\Omega$  series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the MK1726-01A. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

## Crystal Information

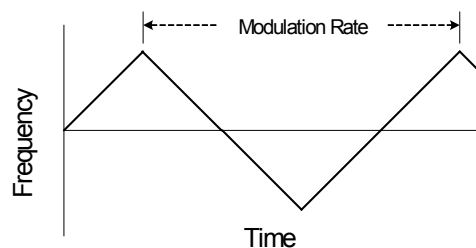
The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation,  $C_L$  is the crystal load capacitance. So, for a crystal with a 16 pF load capacitance, two 20 pF [(16-6) x 2] capacitors should be used.

## Spread Spectrum Profile

The MK1726-01A low EMI clock generator uses an optimized frequency slew rate algorithm to facilitate down stream tracking of zero delay buffers and other PLL devices. The frequency modulation amplitude is constant with variations of the input frequency.



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1726-01A. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		3.63	V

## DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V, Ambient Temperature 0 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0	3.3	3.63	V
Supply Current	IDD	No load, at 3.3 V, Fin=24 MHz		23	30	mA
		No load, at 3.3 V, Fin=12 MHz			25	mA
		No load, at 3.3 V, Fin=32 MHz			35	mA
Input High Voltage	V <sub>IH</sub>		0.85VDD	VDD	VDD	V
Input middle Voltage	V <sub>IHM</sub>		0.4VDD	0.5VDD	0.6VDD	V
Input Low Voltage	V <sub>IL</sub>		0.0	0.0	0.15VDD	V
Output High Voltage	V <sub>OH</sub>	CMOS, I <sub>OH</sub> = -4 mA	2.4			V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -6 mA	2.0			V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Low Voltage	$V_{OL}$	$I_{OL} = -4 \text{ mA}$			0.4	V
		$I_{OL} = -10 \text{ mA}$			1.2	V
Input Capacitance	$C_{IN1}$	S0, S1, FRSEL pins		4	6	pF
	$C_{IN2}$	X1, X2 pins		6	9	pF

## AC Electrical Characteristics

Unless stated otherwise,  $V_{DD} = 3.3 \text{ V}$ , Ambient Temperature 0 to  $+85^\circ \text{ C}$

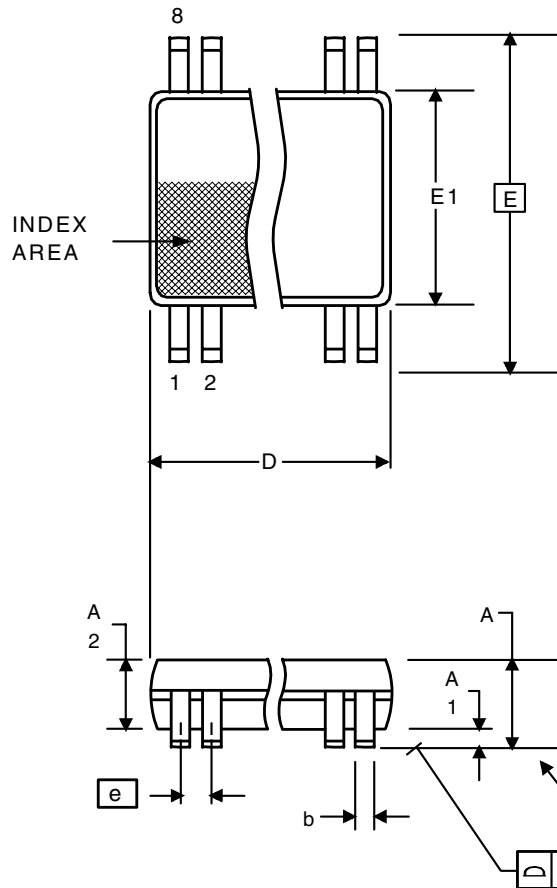
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency			4		32	MHz
Output Clock Frequency			4		32	MHz
Input Clock Duty Cycle		Time above $V_{DD}/2$	40		60	%
Output Clock Duty Cycle		Time above 1.5 V	45	50	55	%
Cycle to cycle Jitter		$F_{in}=4 \text{ MHz}$ , $F_{out}=4 \text{ MHz}$		675	800	ps
Cycle to cycle Jitter		$F_{in}=8 \text{ MHz}$ , $F_{out}=8 \text{ MHz}$		260	450	ps
Output Rise Time	$t_R$	0.4 to 2.4 V	2.4	3.2	4.0	ns
Output Fall Time	$t_F$	2.4 to 0.4 V	2.4	3.2	4.0	ns
EMI Peak Frequency Reduction				8 to 16		dB

## Thermal Characteristics

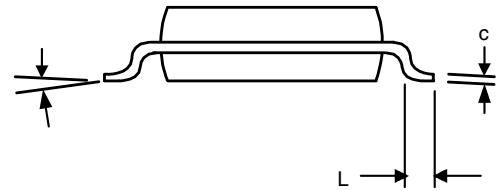
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still air		150		$^\circ\text{C/W}$
	$\theta_{JA}$	1 m/s air flow		140		$^\circ\text{C/W}$
	$\theta_{JA}$	3 m/s air flow		120		$^\circ\text{C/W}$
Thermal Resistance Junction to Case	$\theta_{JC}$			40		$^\circ\text{C/W}$

## Package Outline and Package Dimensions (8-pin TSSOP)

Package dimensions are kept current with JEDEC Publication No. 95

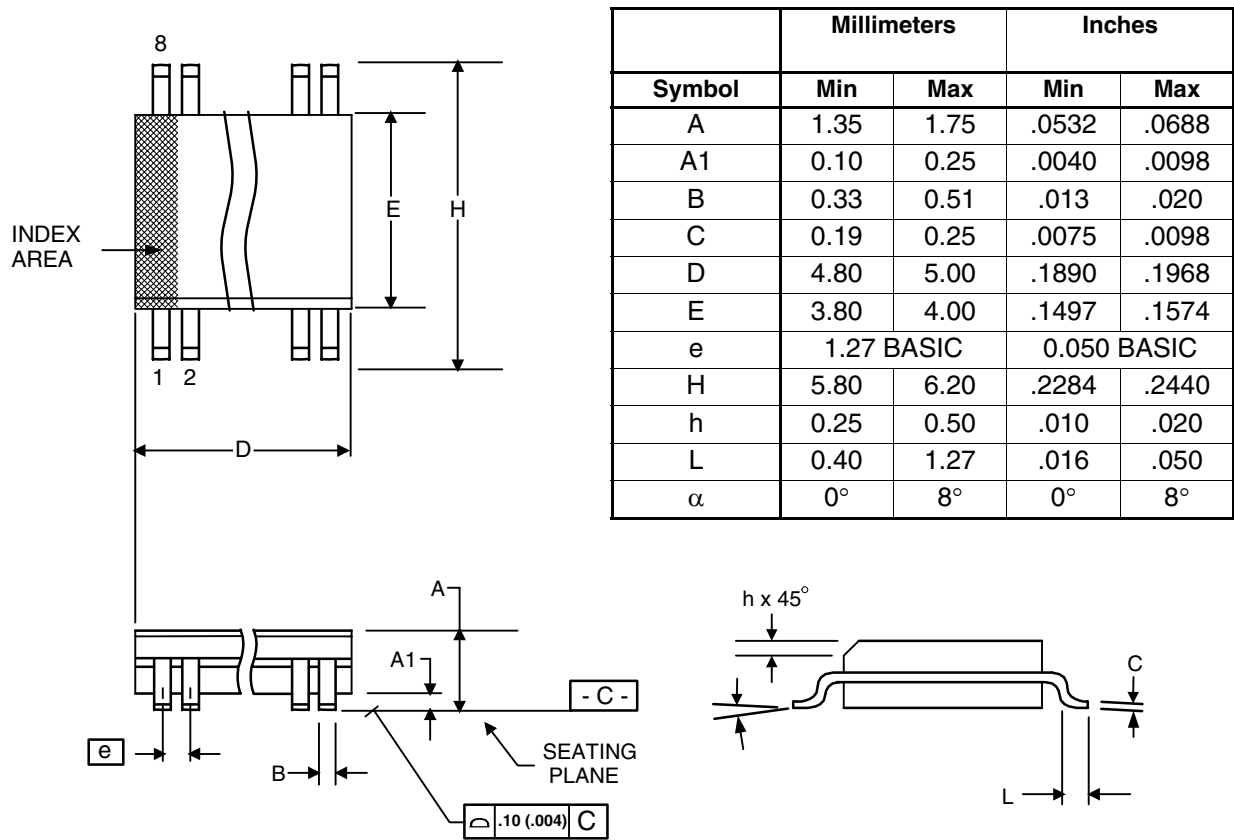


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	2.90	3.10	0.114	0.122
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
$\alpha$	0°	8°	0°	8°
aaa	-	0.10	-	0.004



## Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



## Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1726-01A	172601A	Tubes	8-pin TSSOP	0 to +85° C
MK1726-01ATR	172601A	Tape and Reel	8-pin TSSOP	0 to +85° C
MK1726-01S	172601S	Tubes	8-pin SOIC	0 to +85° C
MK1726-01STR	172601S	Tape and Reel	8-pin SOIC	0 to +85° C

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