PRELIMINARY

M5M4V18160CTP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

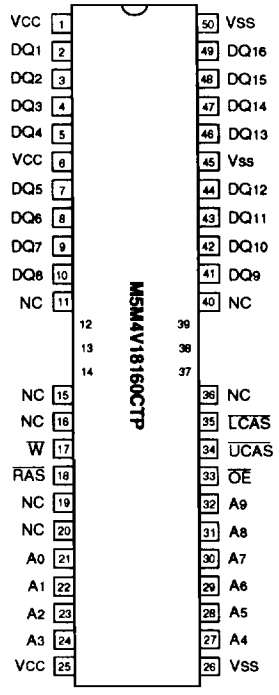
The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V18160CTP-5,-5S	50	13	25	13	90	540
M5M4V18160CTP-6,-6S	60	15	30	15	110	450
M5M4V18160CTP-7,-7S	70	20	35	20	130	390

- Standard 50 pin TSOP
- Single 3.3V ±0.3V supply
- Low stand-by power dissipation
  1.8mW (Max) ---------- CMOS Input level
- Low operating power dissipation
  M5M4V18160CTP-5,-5S ---------- 650.0mW (Max)
  M5M4V18160CTP-6,-6S ---------- 540.0mW (Max)
  M5M4V18160CTP-7,-7S ---------- 470.0mW (Max)
- Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
  * : Applicable to self refresh version (M5M4V18160CTP-5S,-6S, -7S : option) only

PIN CONFIGURATION (TOP VIEW)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_{16}	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
V_{CC}	Power supply (+3.3V)
V_{SS}	Ground (0V)

PRELIMINARY

M5M4V18160CTP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

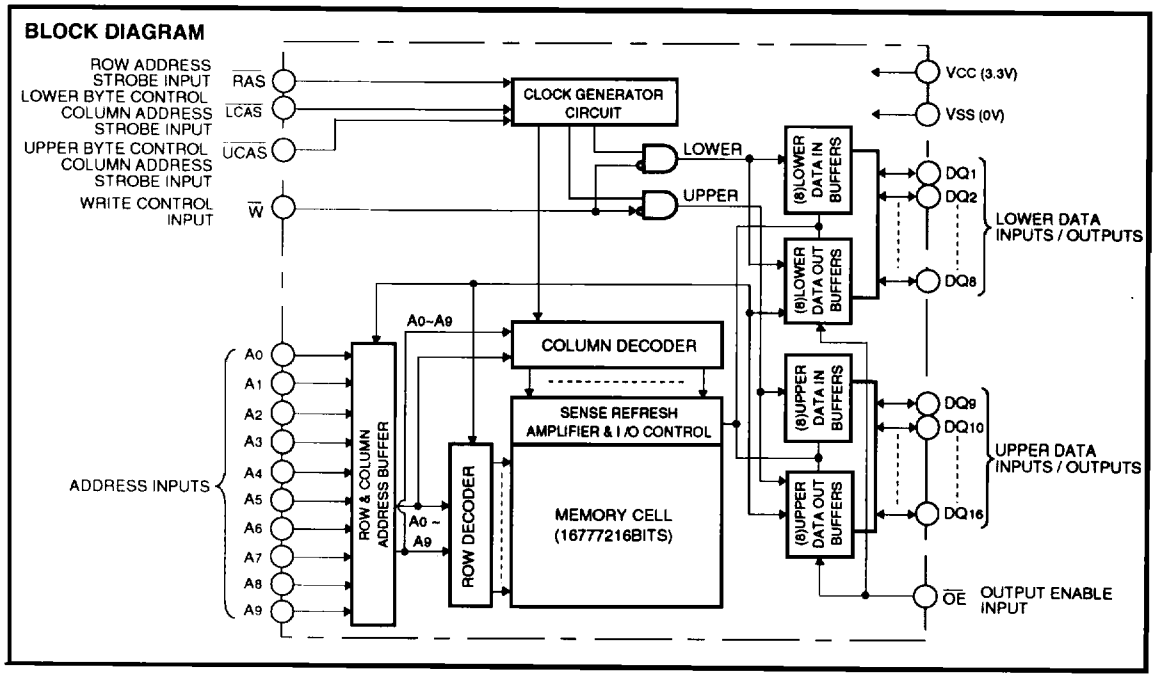
The M5M4V18160CTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PRELIMINARY

M5M4V18160CTP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
V_O	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.3V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3,4,5)	M5M4V18160C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			180	mA
		M5M4V18160C-6,-6S				150	
		M5M4V18160C-7,-7S				130	
I_{CC2}	Supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧V_{CC}-0.2V output open			0.5	
						0.15 *	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3,5)	M5M4V18160C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			180	mA
		M5M4V18160C-6,-6S				150	
		M5M4V18160C-7,-7S				130	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-page-mode (Note 3,4,5)	M5M4V18160C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M4V18160C-6,-6S				70	
		M5M4V18160C-7,-7S				65	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V18160C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			180	mA
		M5M4V18160C-6,-6S				150	
		M5M4V18160C-7,-7S				130	
$I_{CC8(AV)}$ *	Average supply current from V_{CC} Extended-refresh cycle (Note 6)	M5M4V18160C (S)	Stand-by: $\overline{RAS}$≧Vcc-0.2V $\overline{CAS}$≧Vcc-0.2V or $\overline{CAS}$≦0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}$≦0.2V or ≧V_{CC}-0.2V $\overline{OE}$≦0.2V or ≧V_{CC}-0.2V A0~A9≦0.2V or ≧V_{CC}-0.2V DQ=open, t_{RC}=125 μs, t_{RAS}=$t_{RASmin.}$~1 μs			300	μA
$I_{CC9(AV)}$ *	Average supply current from V_{CC} Self-refresh cycle	M5M4V18160C (S)	$\overline{RAS}$=$\overline{CAS}$≦0.2V			200	μA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH} .

CAPACITANCE (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Columu address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	13	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-2mA) / VOL=0.4V(IOL=2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OFF(max)}$ and $t_{OEZ\ (max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq | \pm 10\ \mu A |$) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter		Limits						Unit
			M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			16.4		16.4		16.4	ms
tREF*	Refresh cycle time			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		15		ns
tT	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.

14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tT+tASC(min).

16: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

17: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

18: Either tDZC or tDZO must be satisfied.

19: Either tCDD or tODD must be satisfied.

20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 21)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 21)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time	25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	8		10		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tWP	Write pulse width	8		10		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note 22)	131		155		180		ns
tRAS	$\overline{RAS}$ low pulse width	91	10000	105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width	54	10000	60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	91		105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	54		60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	36		40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	73		85		95		ns
tAWD	Delay time, address to $\overline{W}$ low (Note 23)	48		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tWP	Write pulse width	8		10		10		ns
tDS	Data setup time before $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{W}$ low	10		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		15		ns

Note 22: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+5tT.
23: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD(min), tAWD≧tAWD(min) and tCPWD≧ tCPWD(min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time	76		85		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note 25)	85	125000	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width (Note 26)	8	12	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	53		60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.
26: tCP(max) is specified as a reference point only.

PRELIMINARY

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M4V18160C-5,-5S		M5M4V18160C-6,-6S		M5M4V18160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

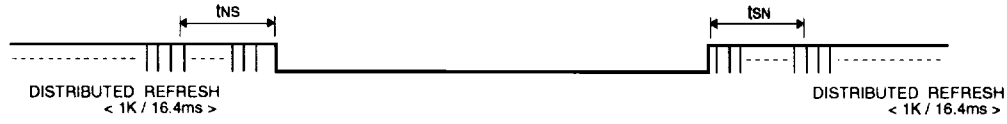
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V18160C-5S		M5M4V18160C-6S		M5M4V18160C-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	Self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
tRPS	Self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
tCHS	Self refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

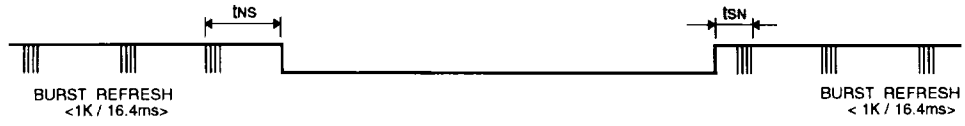
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS≦16.4ms and tSN≦16.4ms.

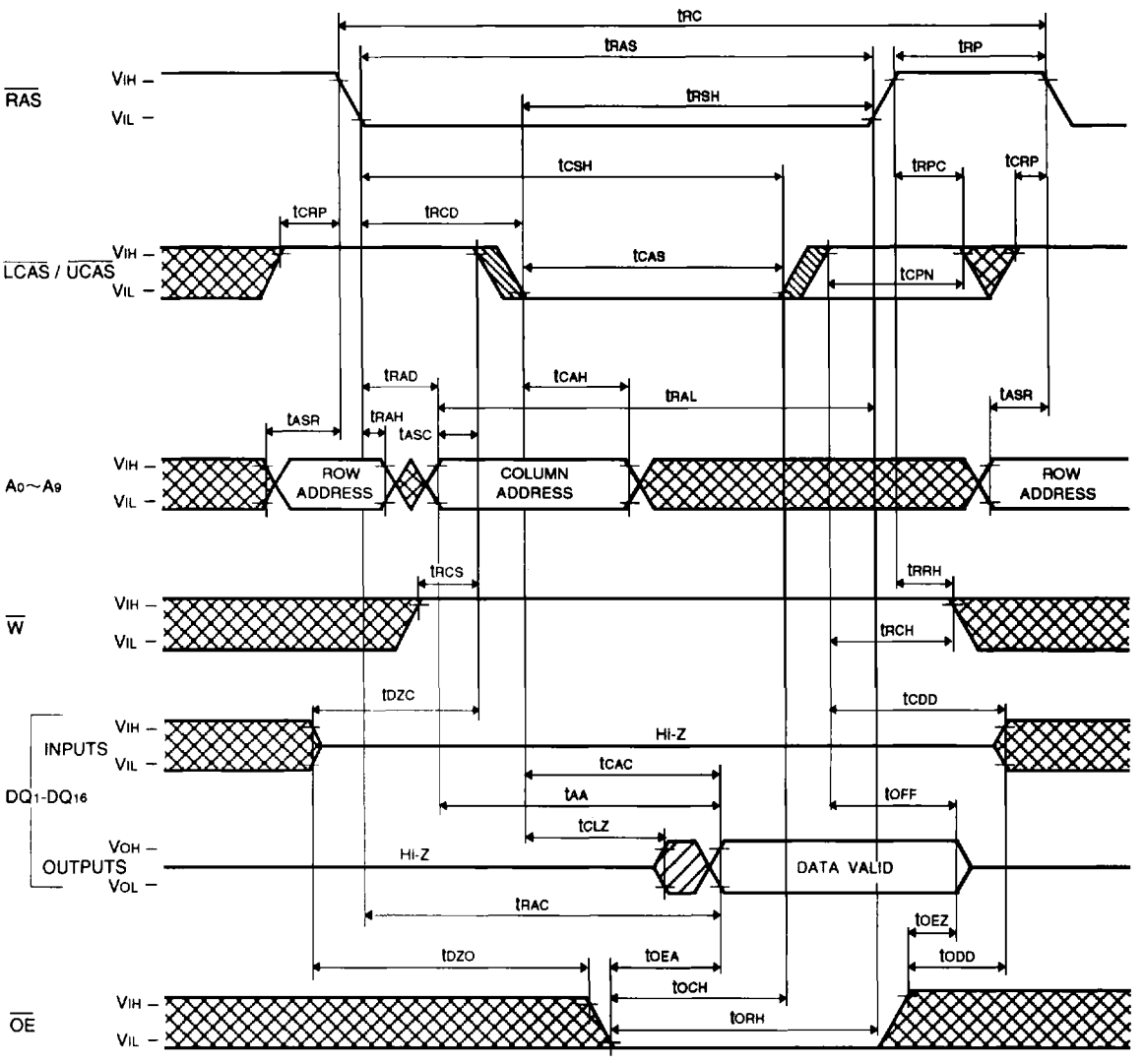


(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS +tSN≦16.4ms.



Timing Diagrams (Note 28)
Read Cycle



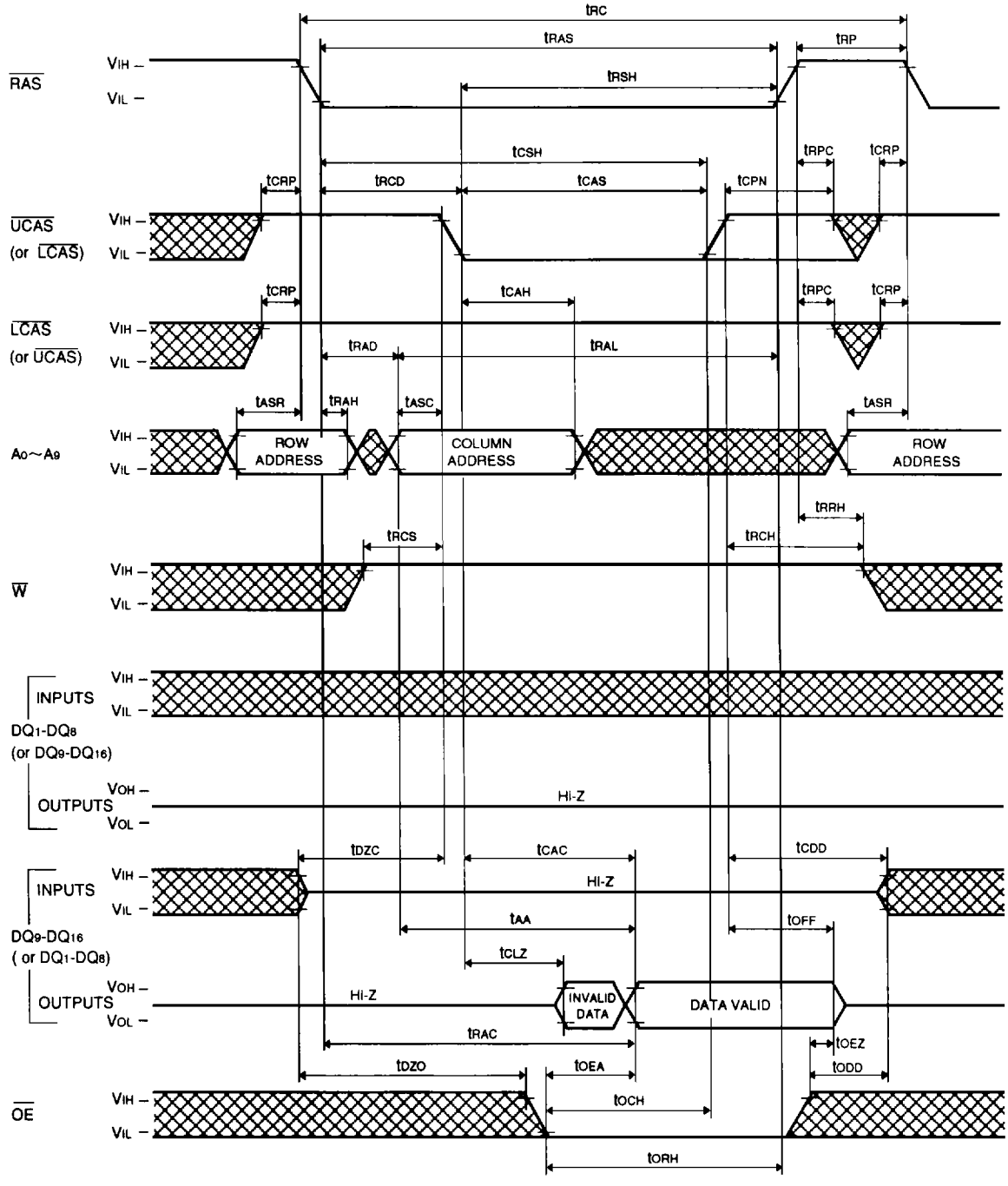
Note 28

Indicates the don't care input.
VIH(min.) ≤ VIN ≤ VIH(max) or VIL(min.) ≤ VIN ≤ VIL(max)

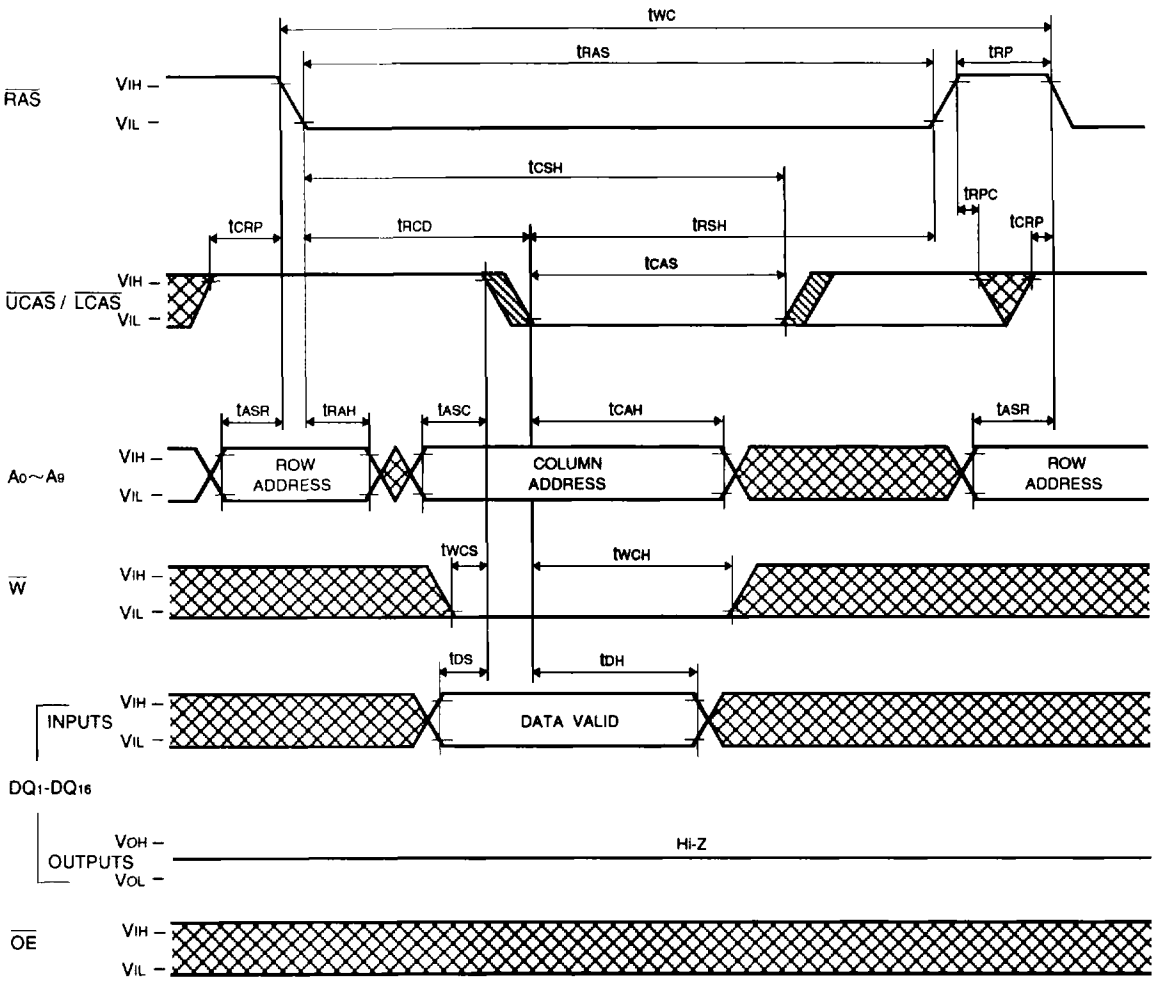
Indicates the invalid output.

Indicates the skew of the two inputs.

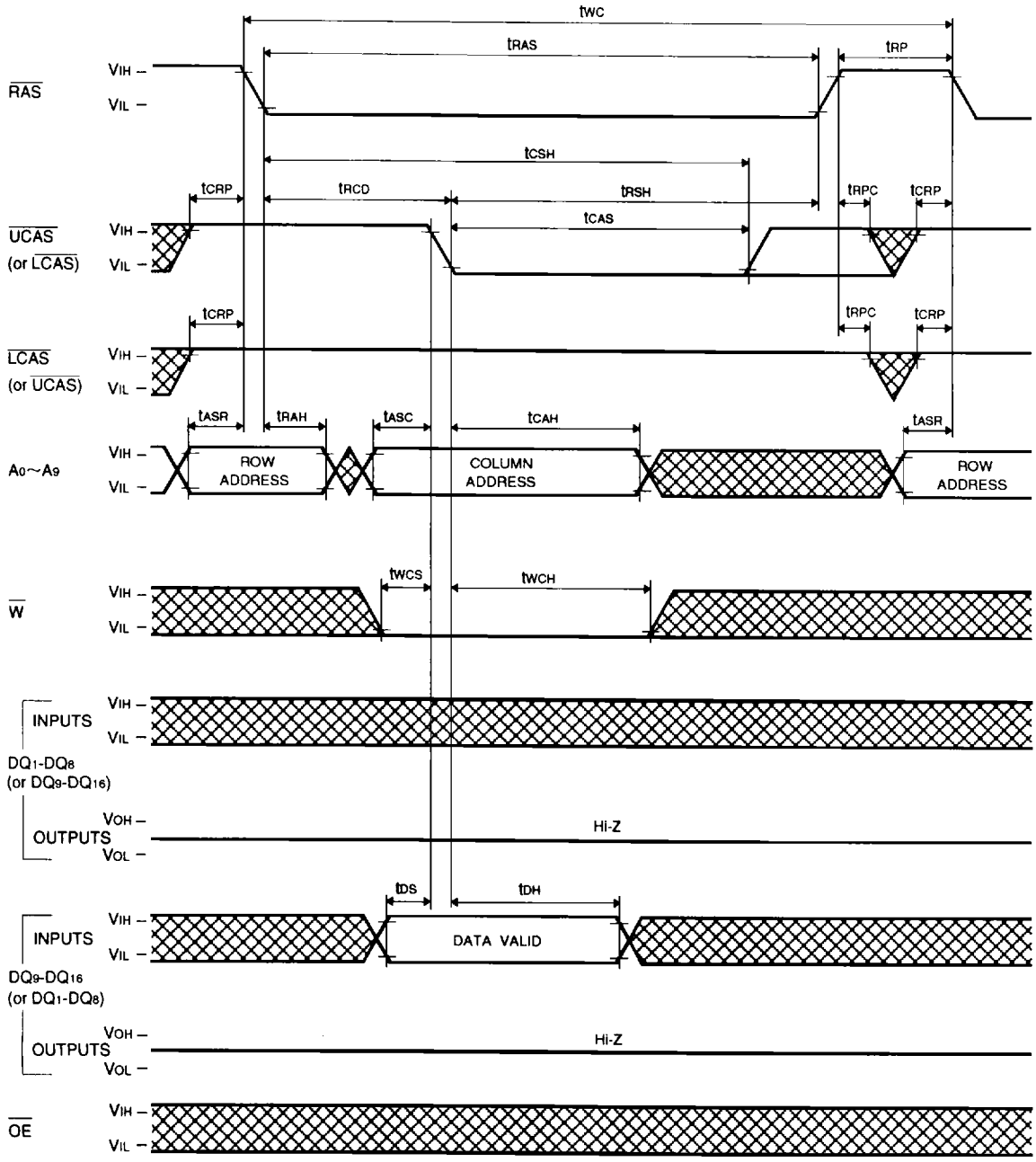
Upper / (Lower) Byte Read Cycle



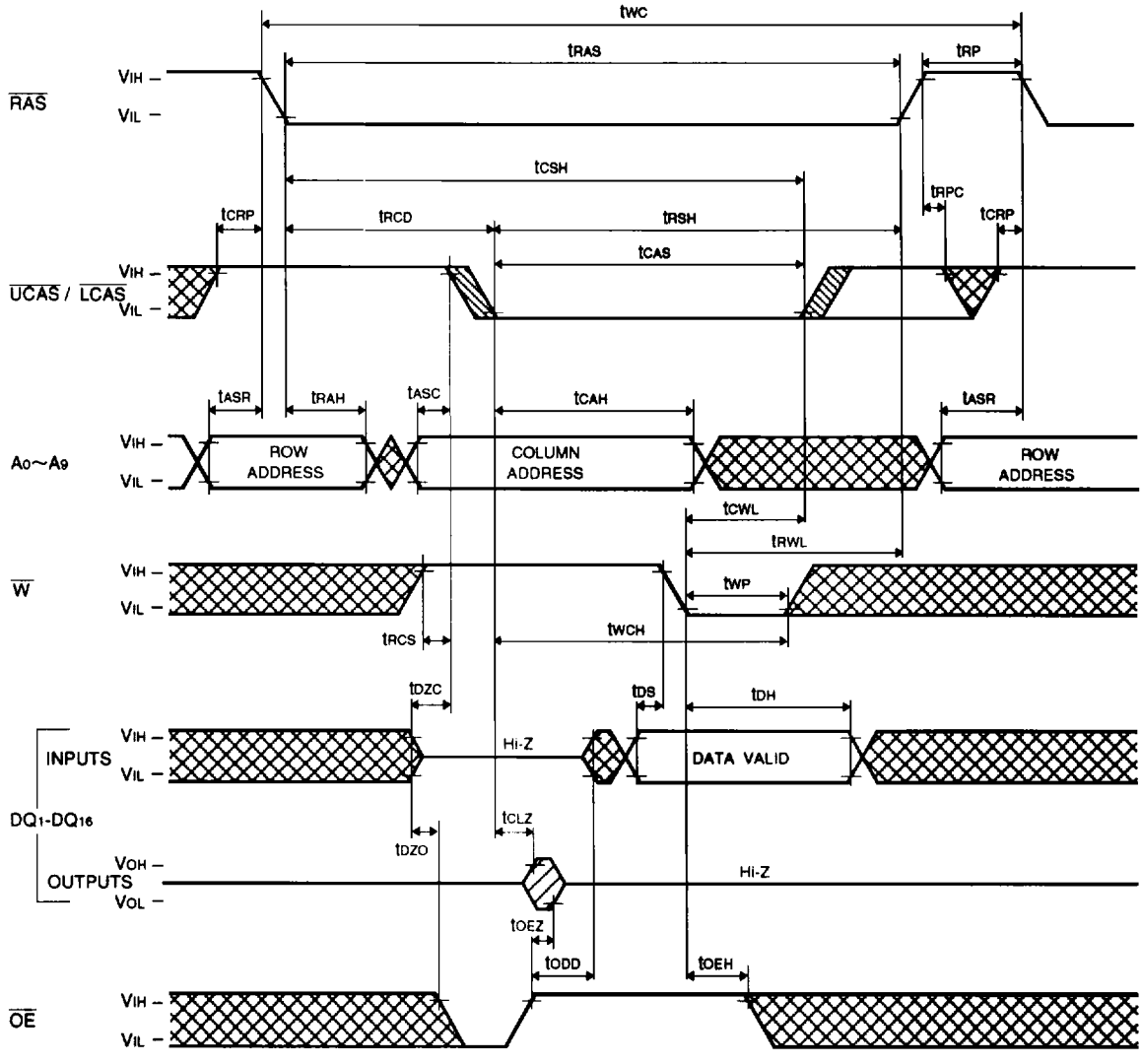
Write Cycle (Early write)



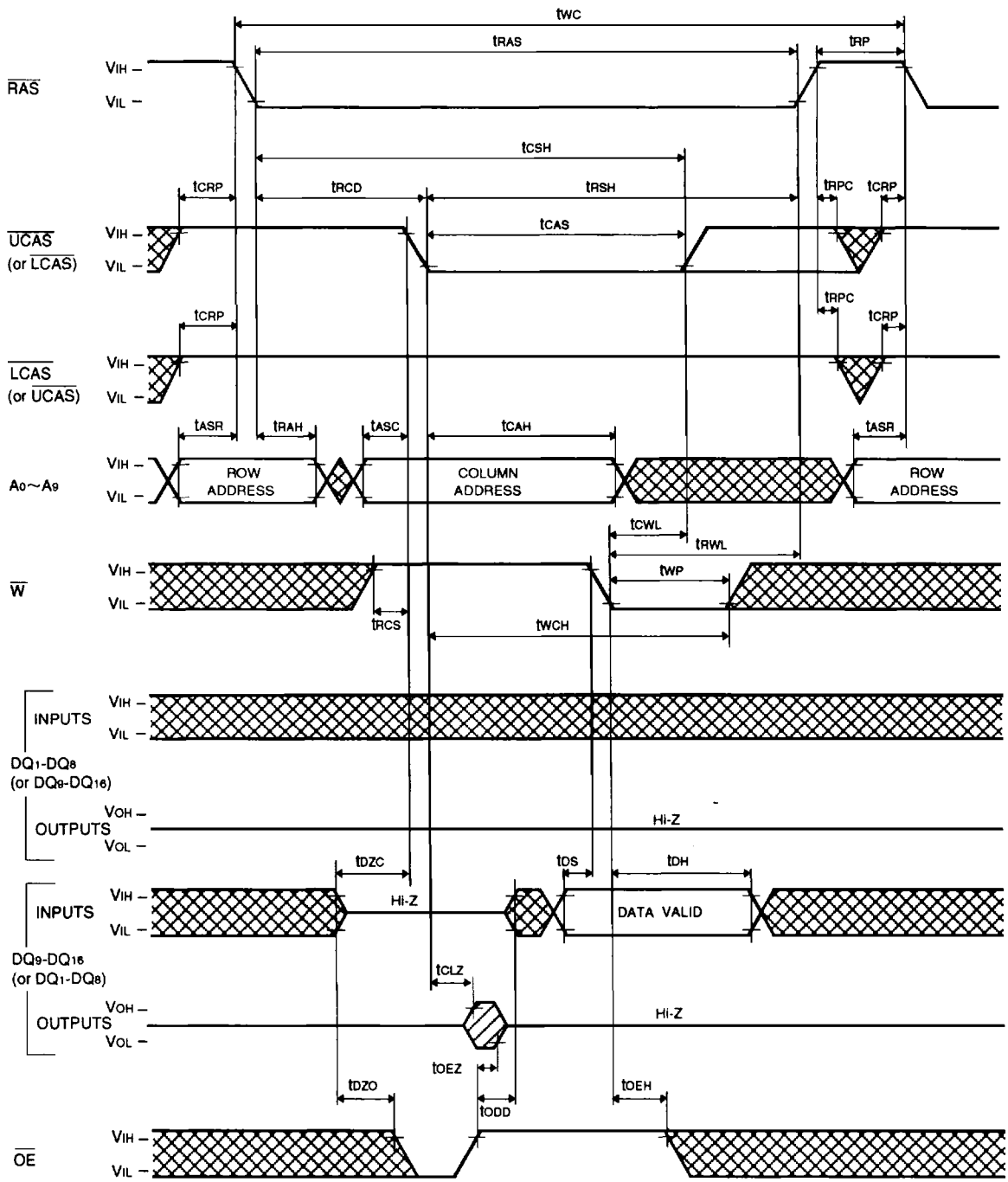
Upper / (Lower) Byte Write Cycle (Early write)



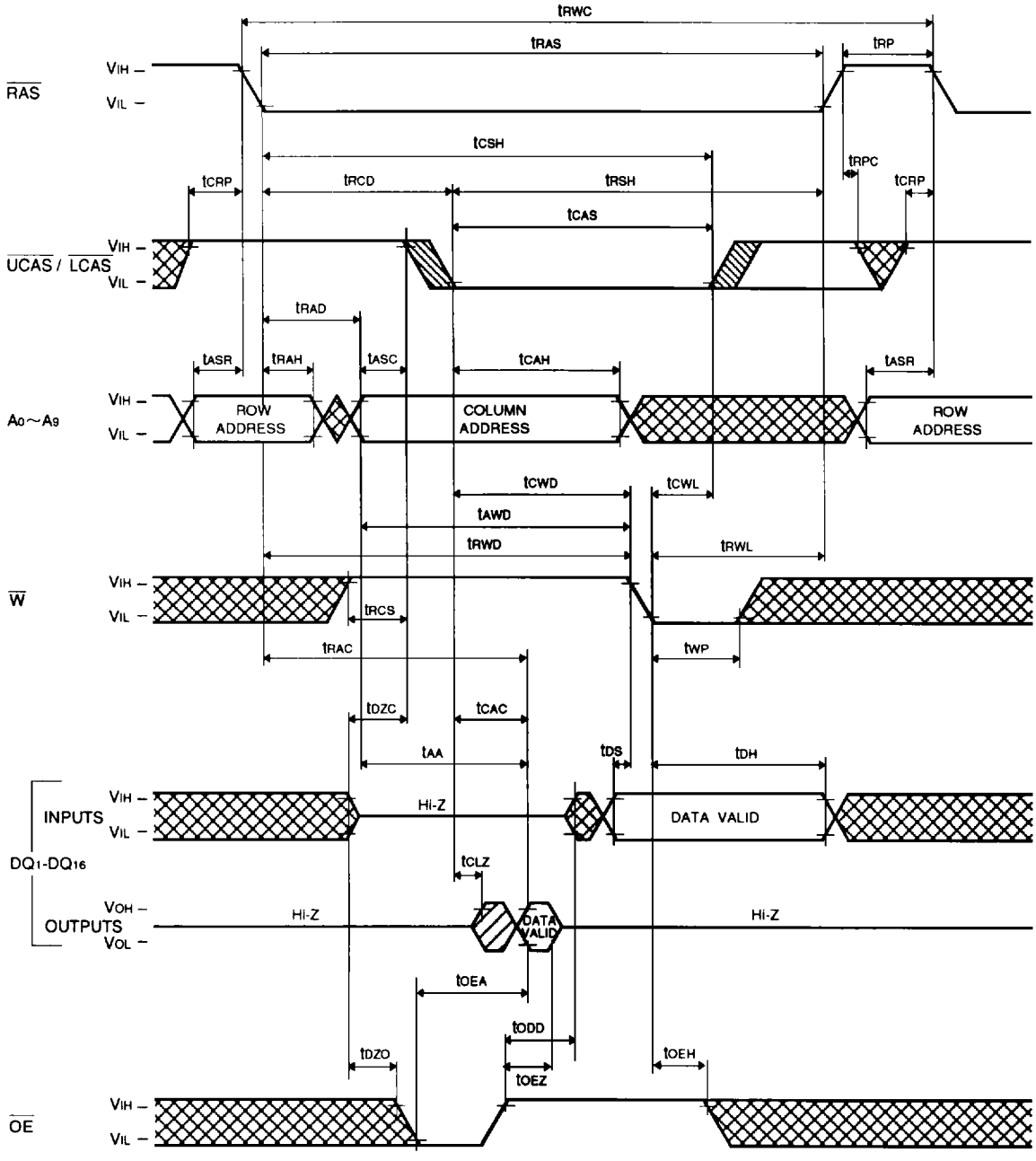
Write Cycle (Delayed write)



Upper / (Lower) Byte Write Cycle (Delayed write)

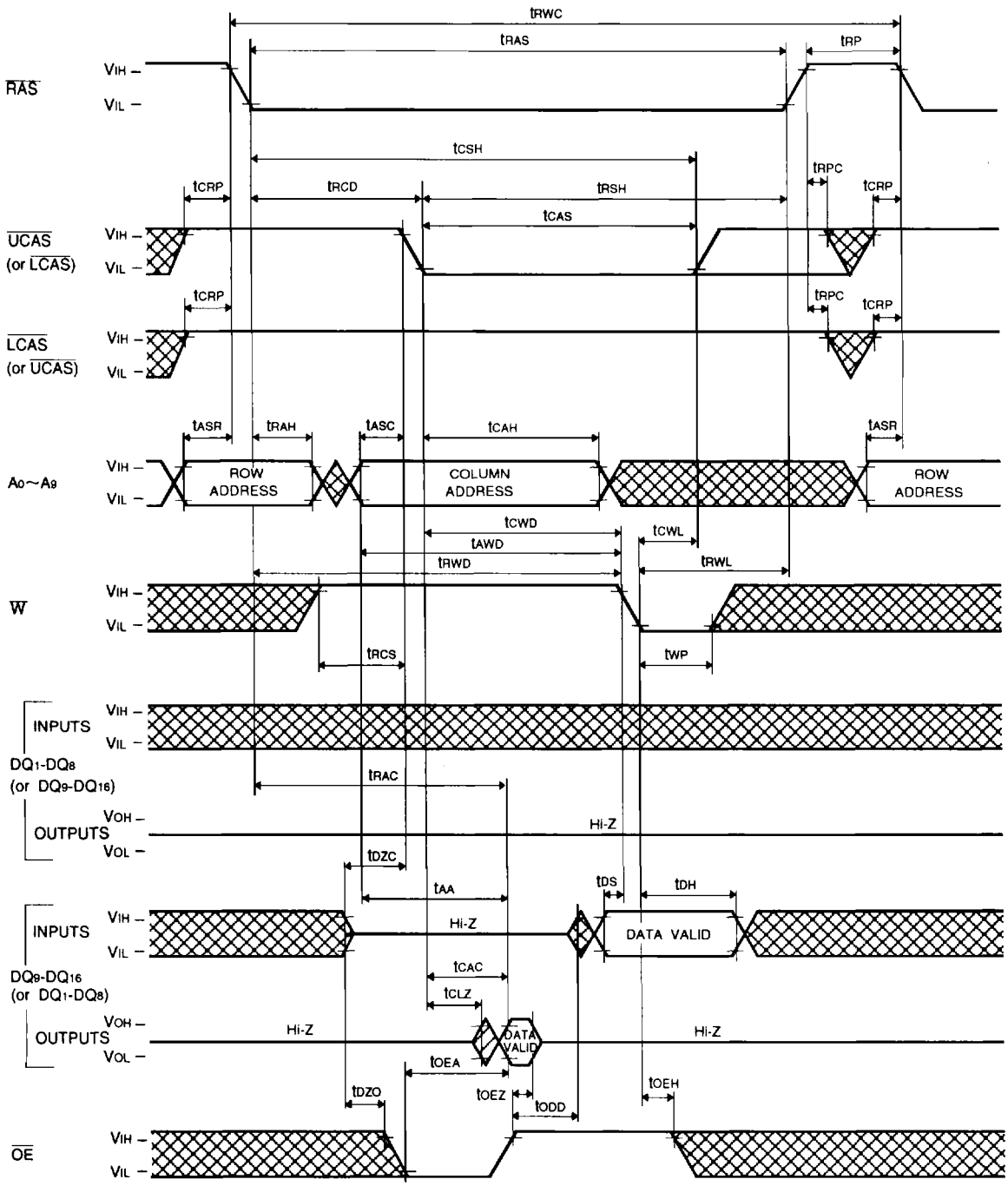


Read-Write, Read-Modify-Write Cycle

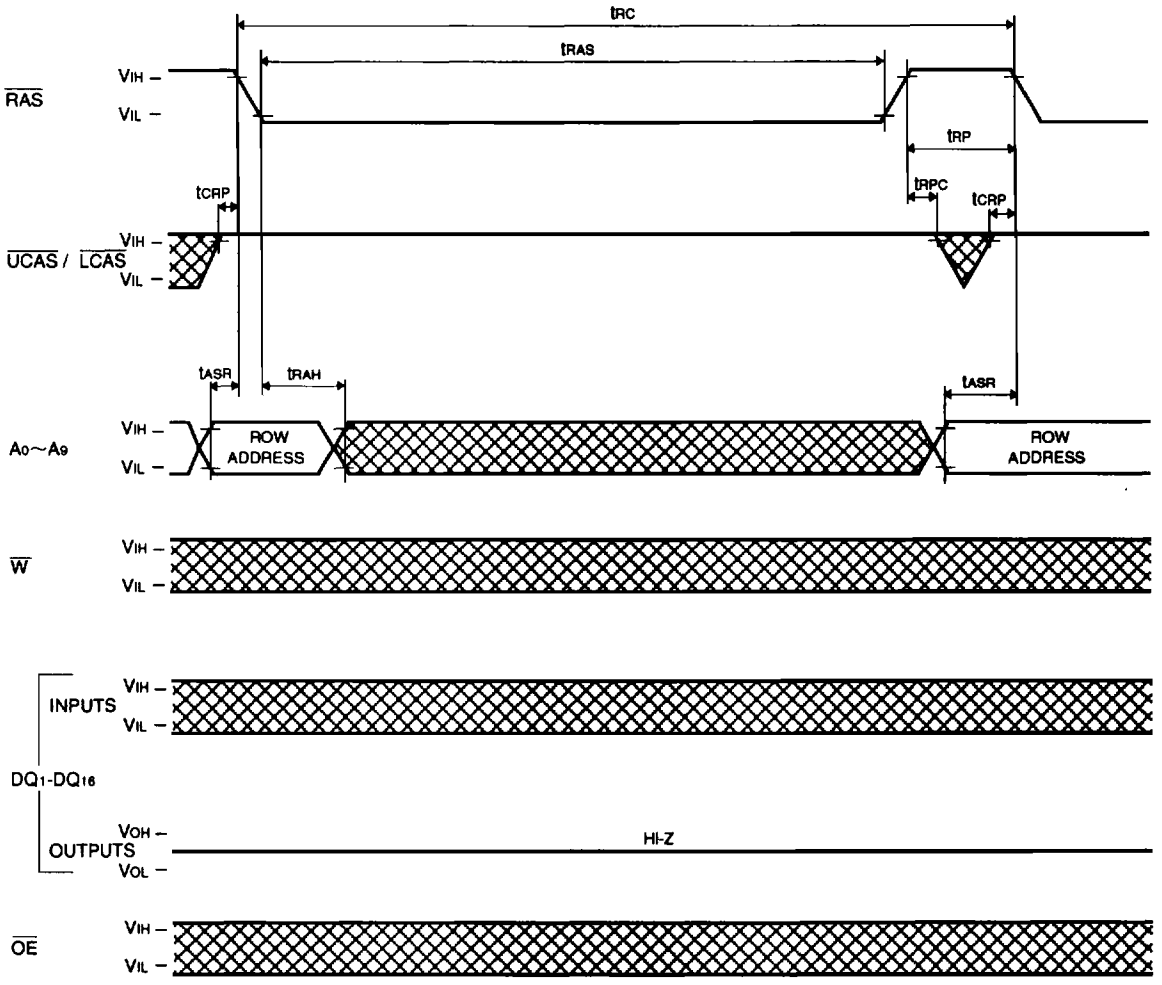


PRELIMINARY

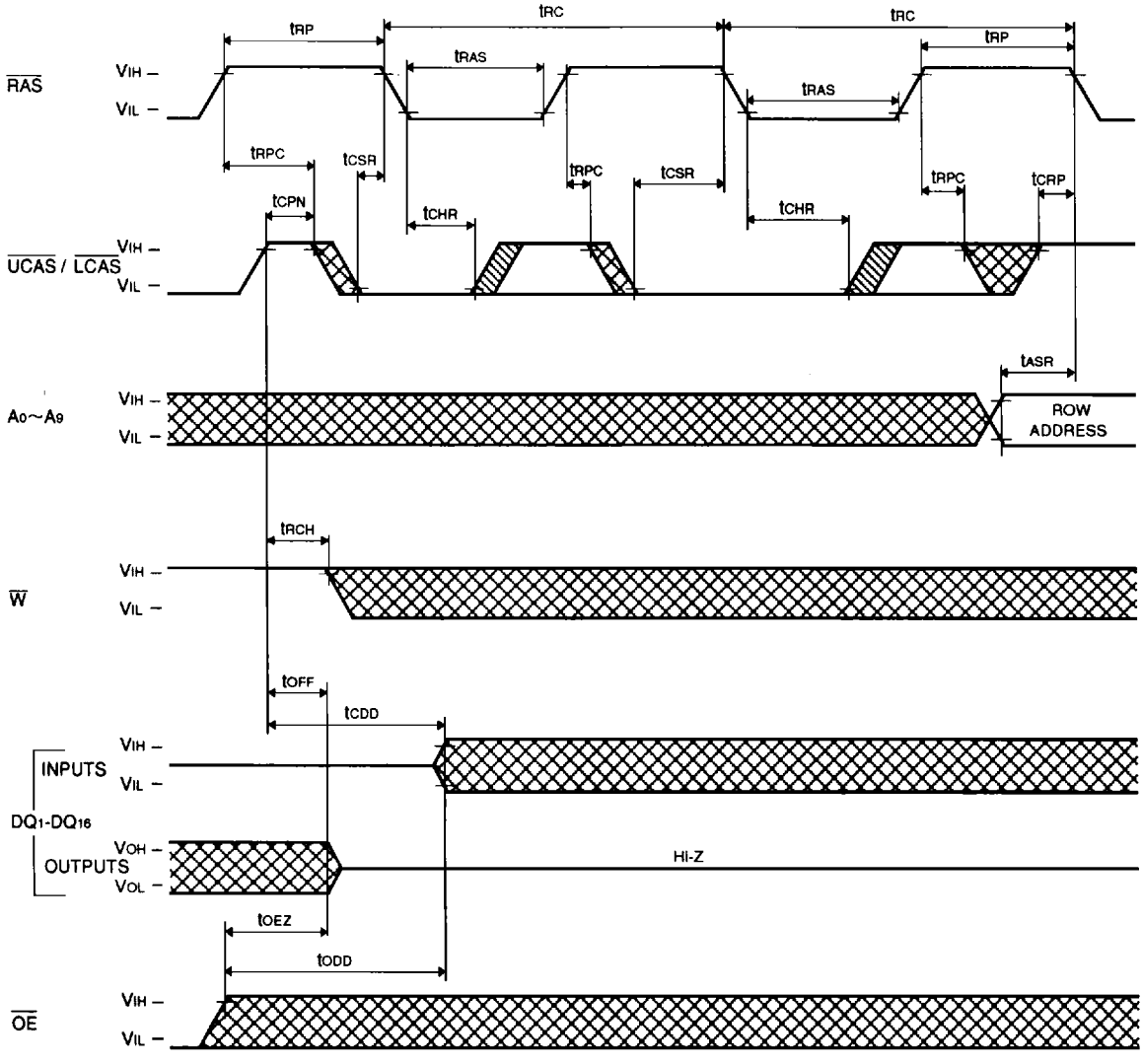
Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle



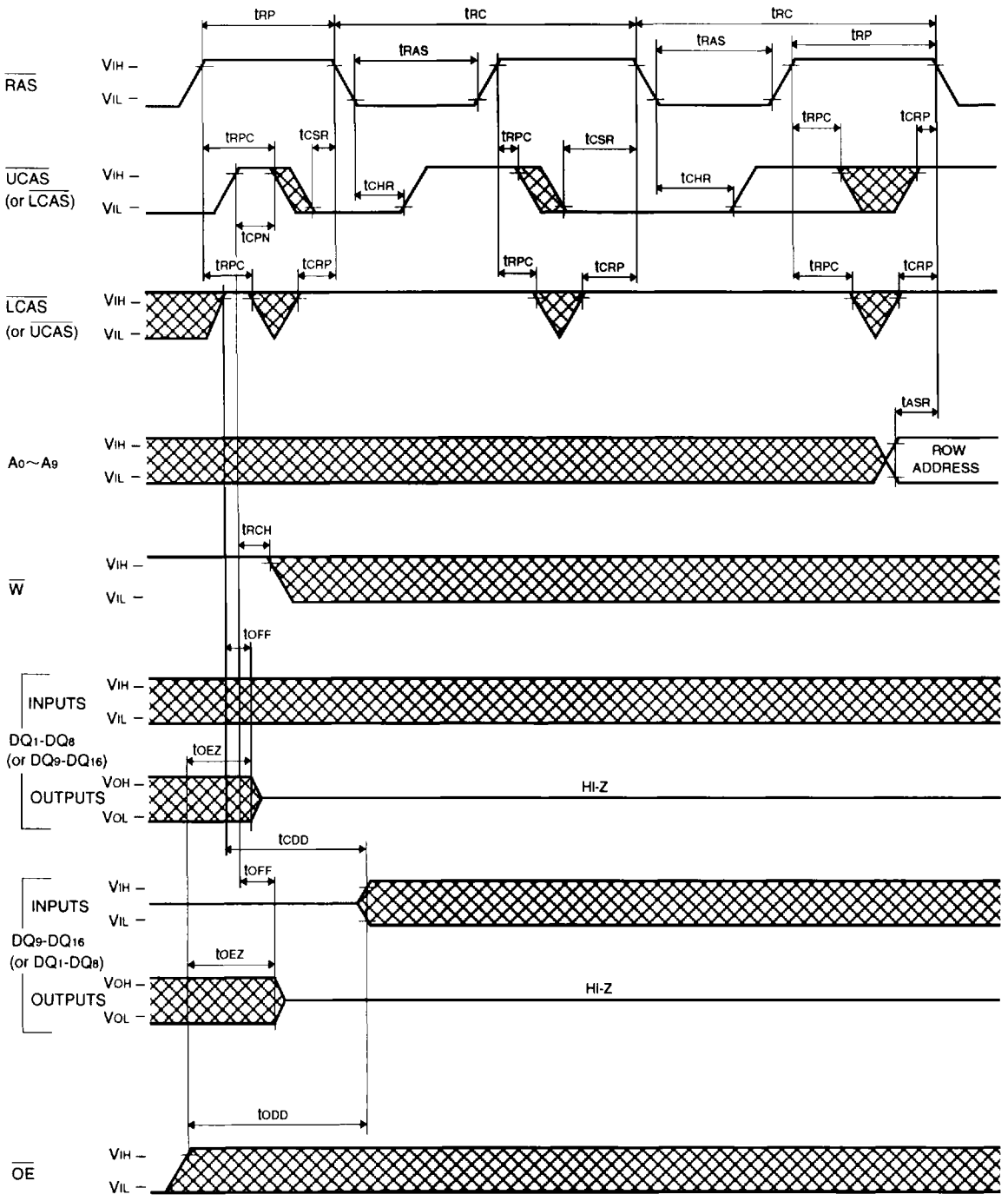
RAS-only Refresh Cycle



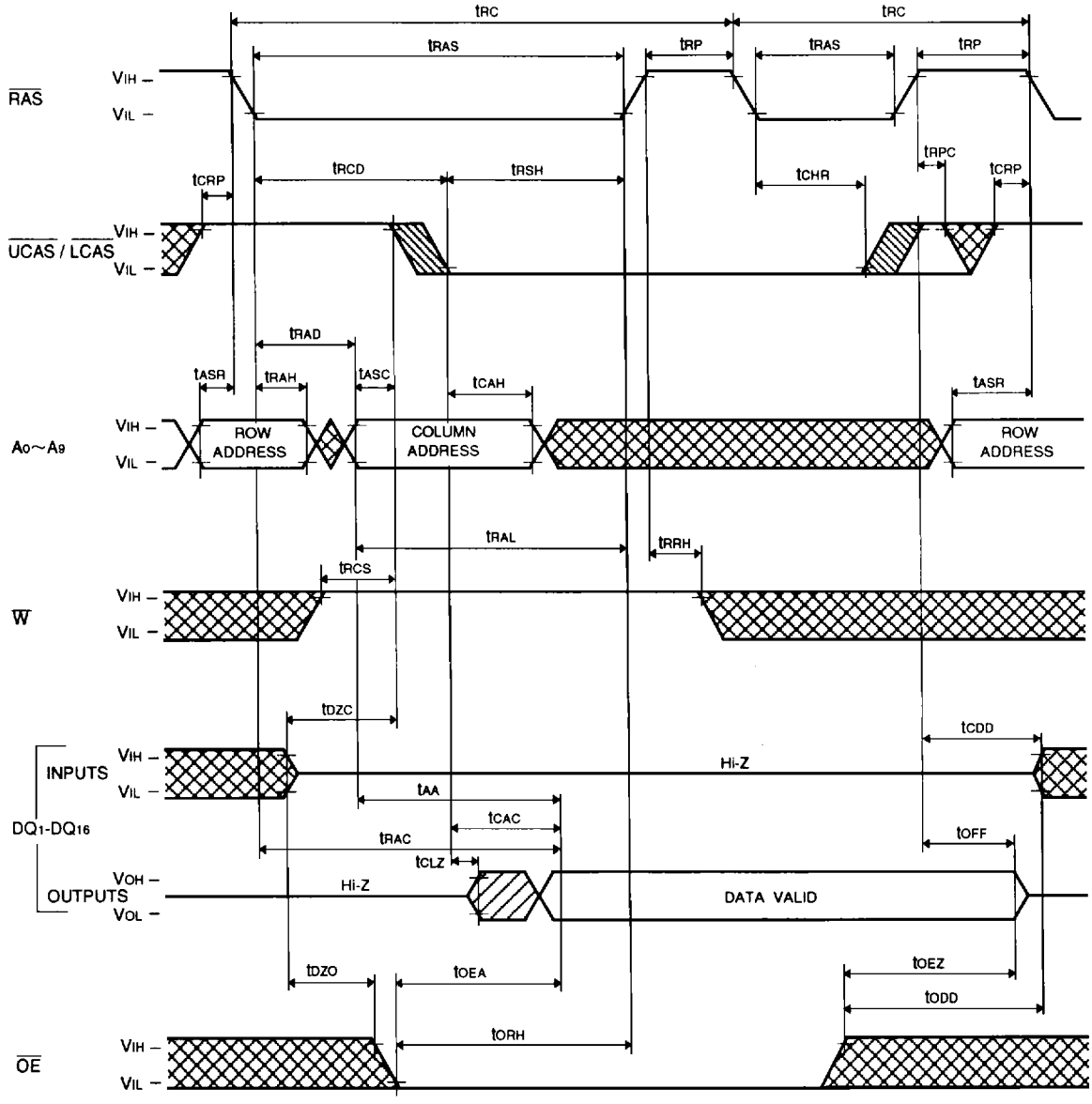
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*



Upper / (Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *

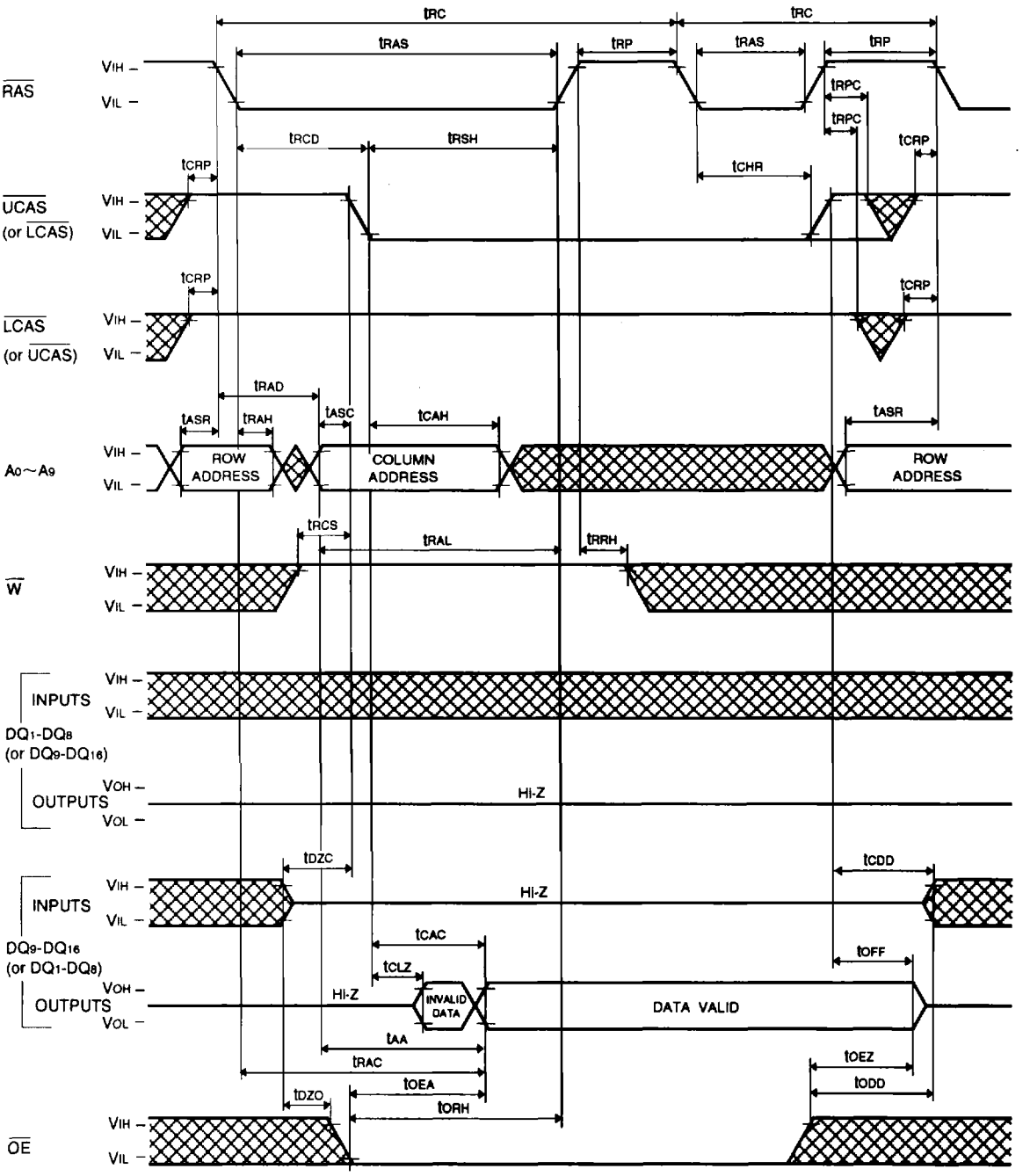


Hidden Refresh Cycle (Read) (Note 29)



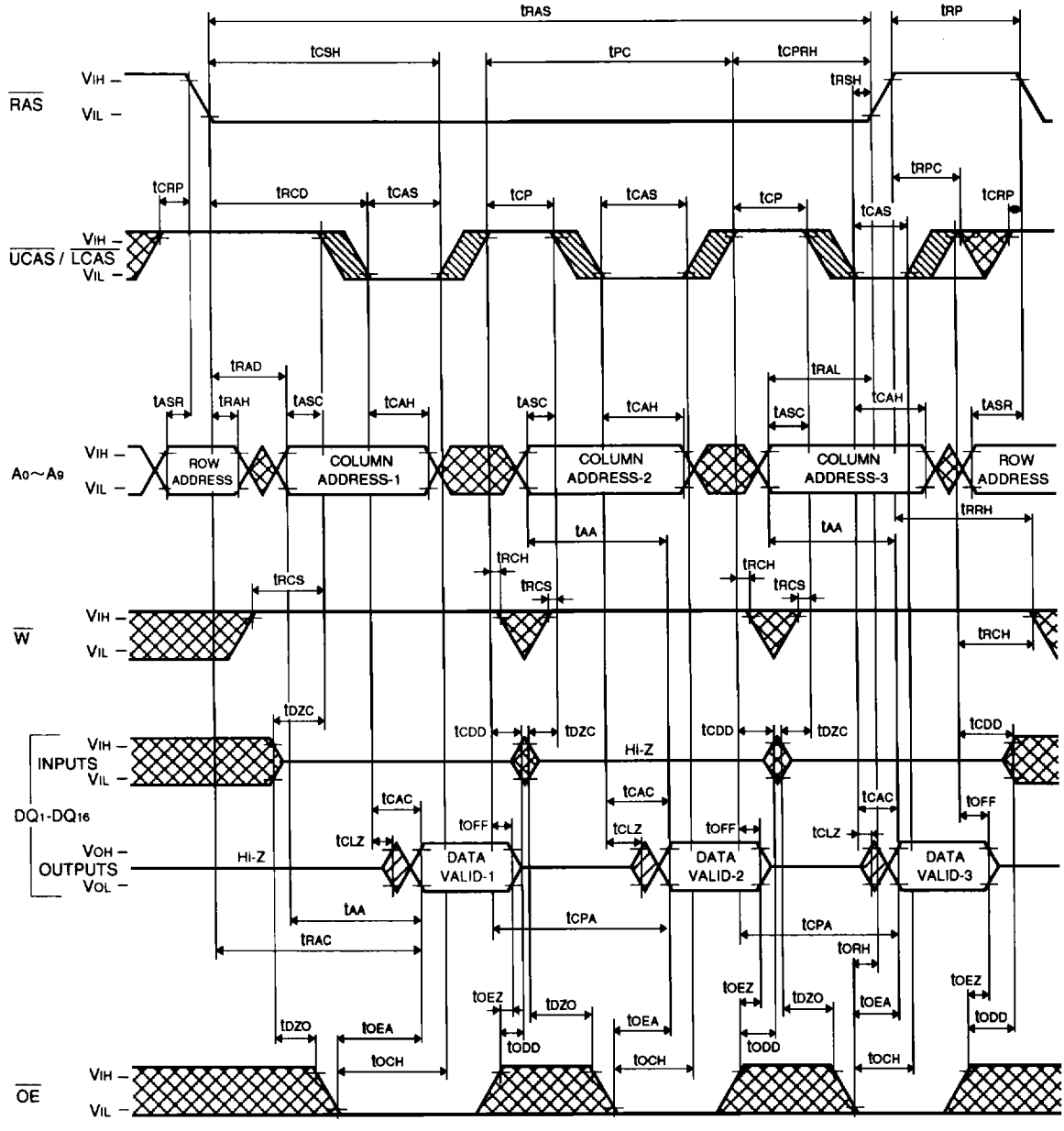
Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Upper / (Lower) Hidden Refresh Cycle (Byte Read) (Note 29)

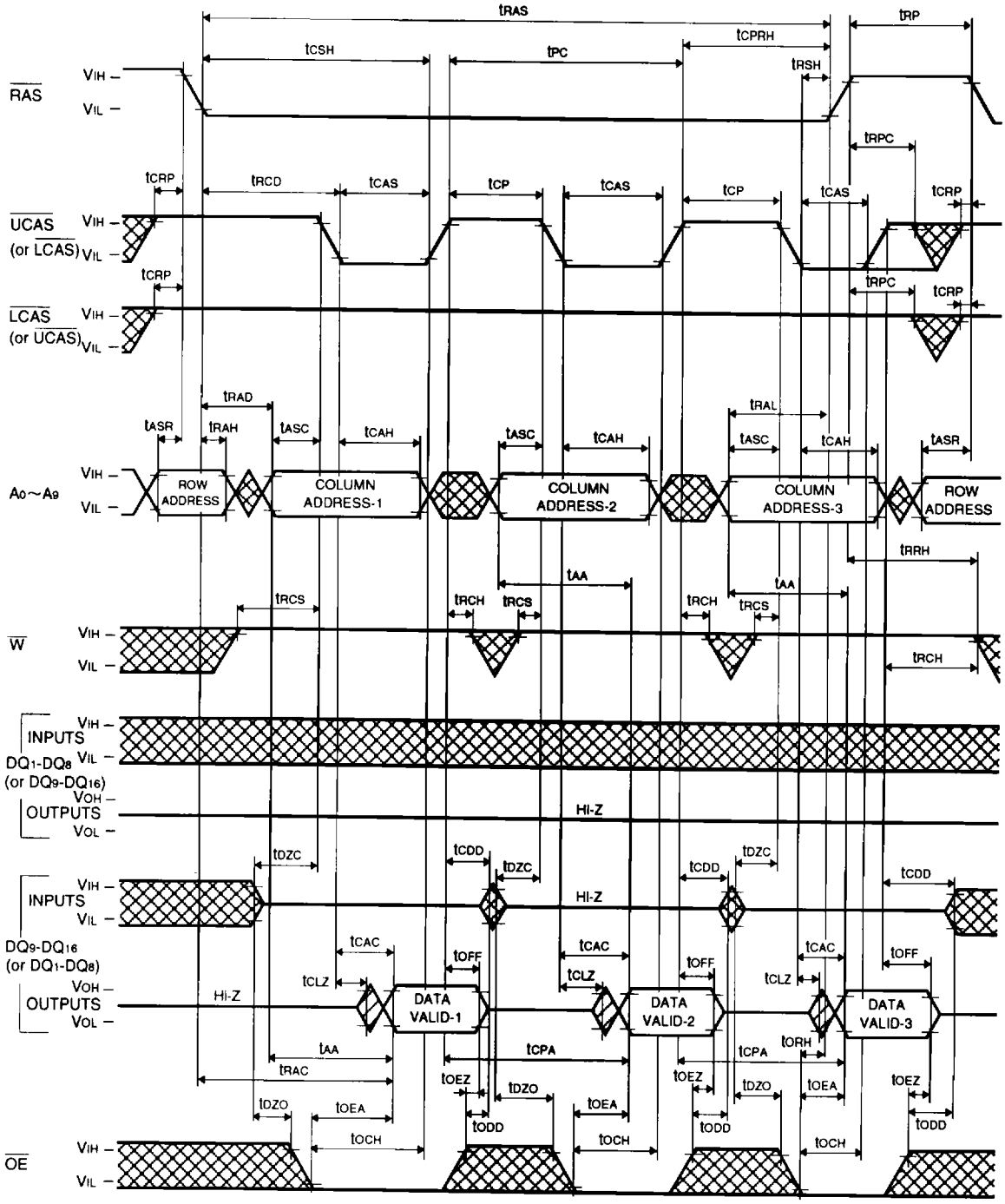


Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

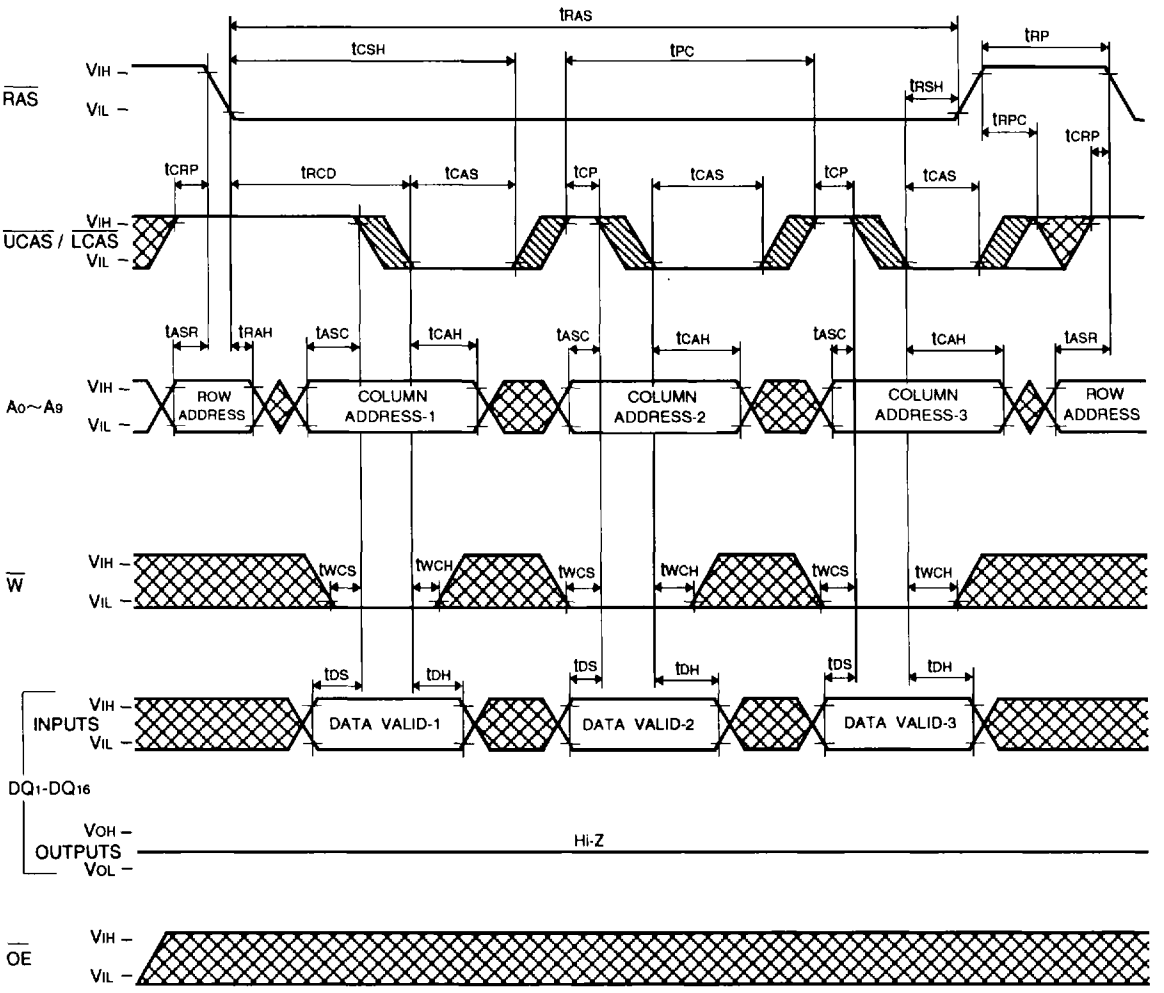
Fast Page Mode Read Cycle



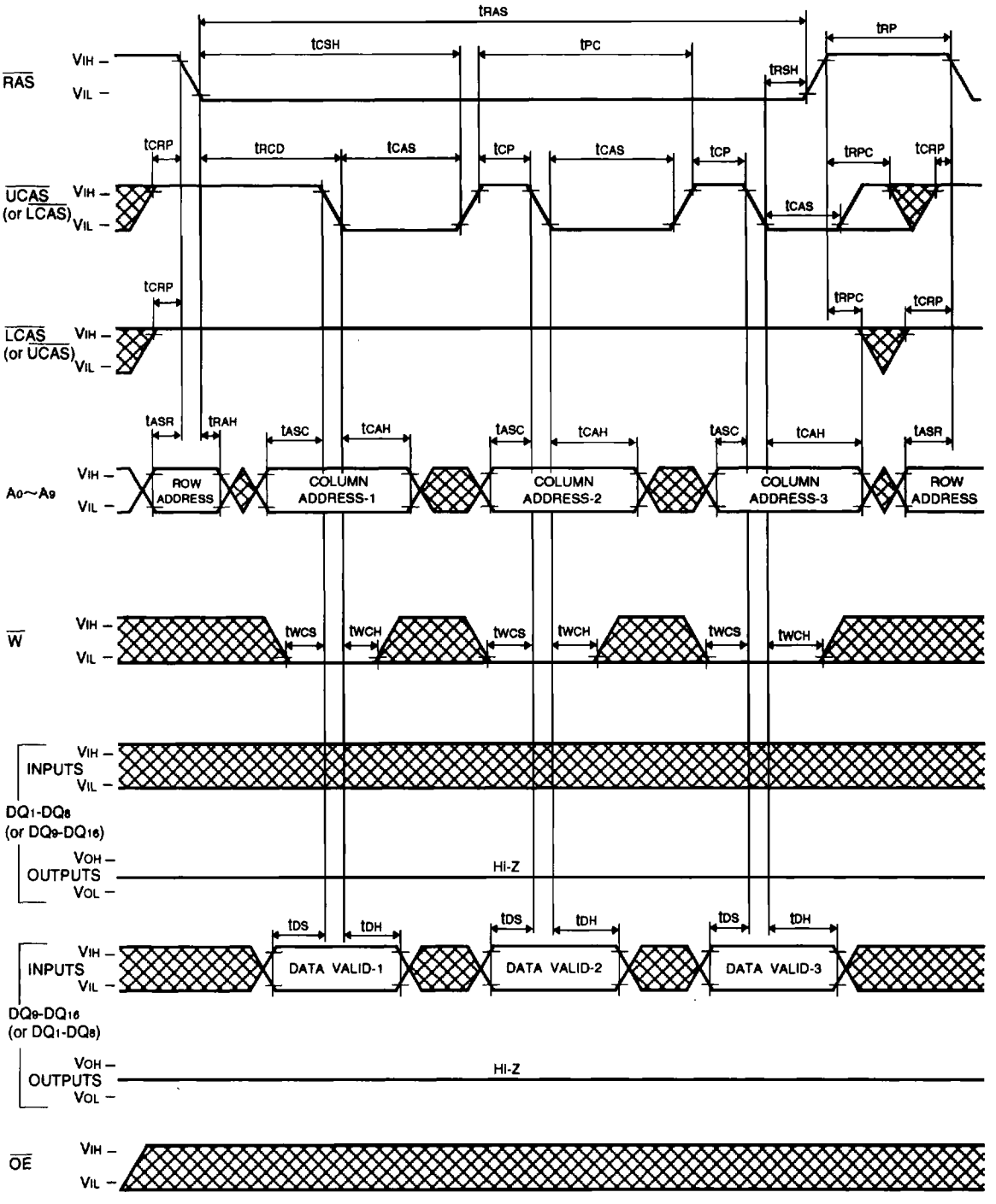
Upper / (Lower) Fast Page Mode Read Cycle



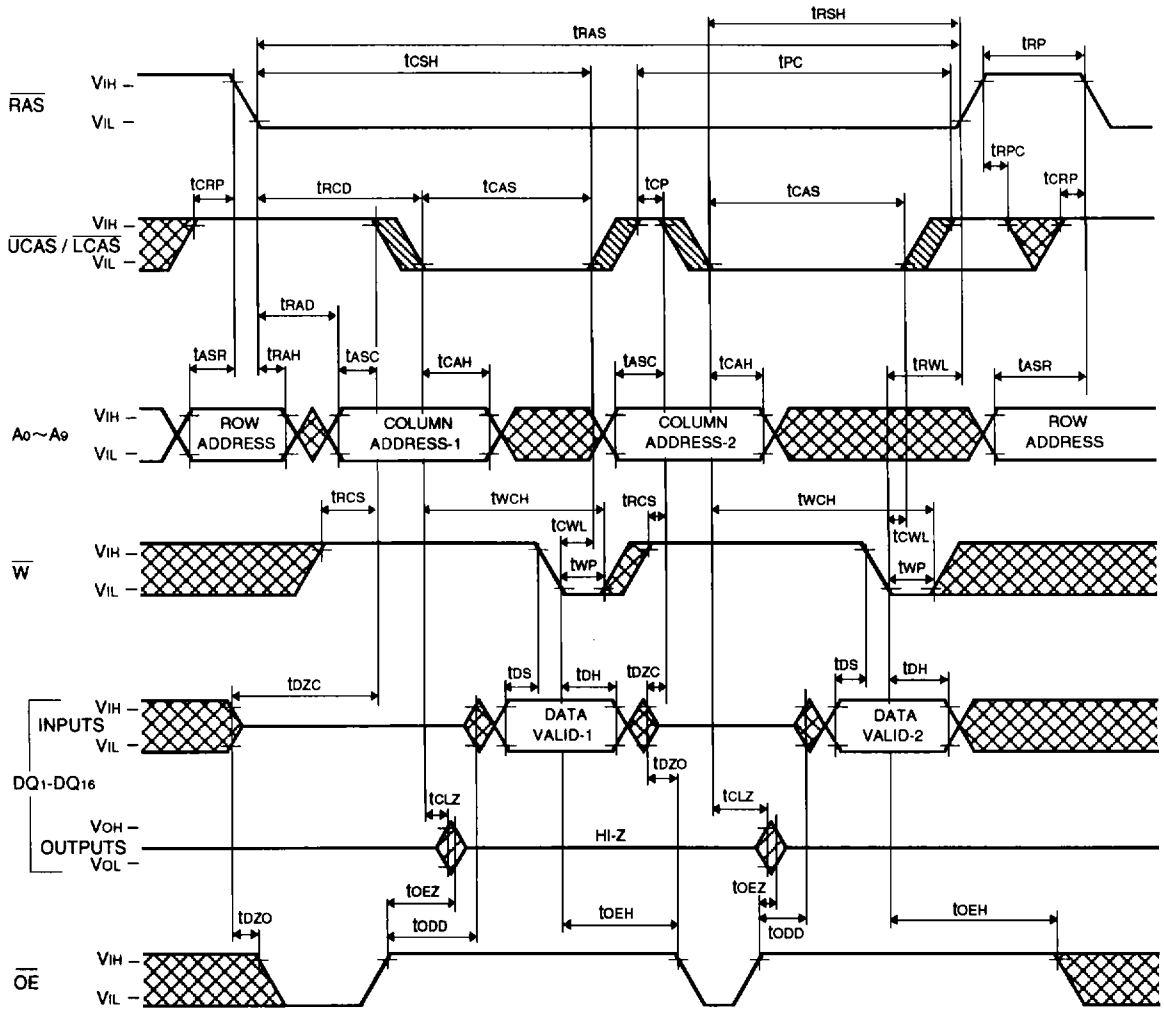
Fast Page Mode Write Cycle (Early Write)



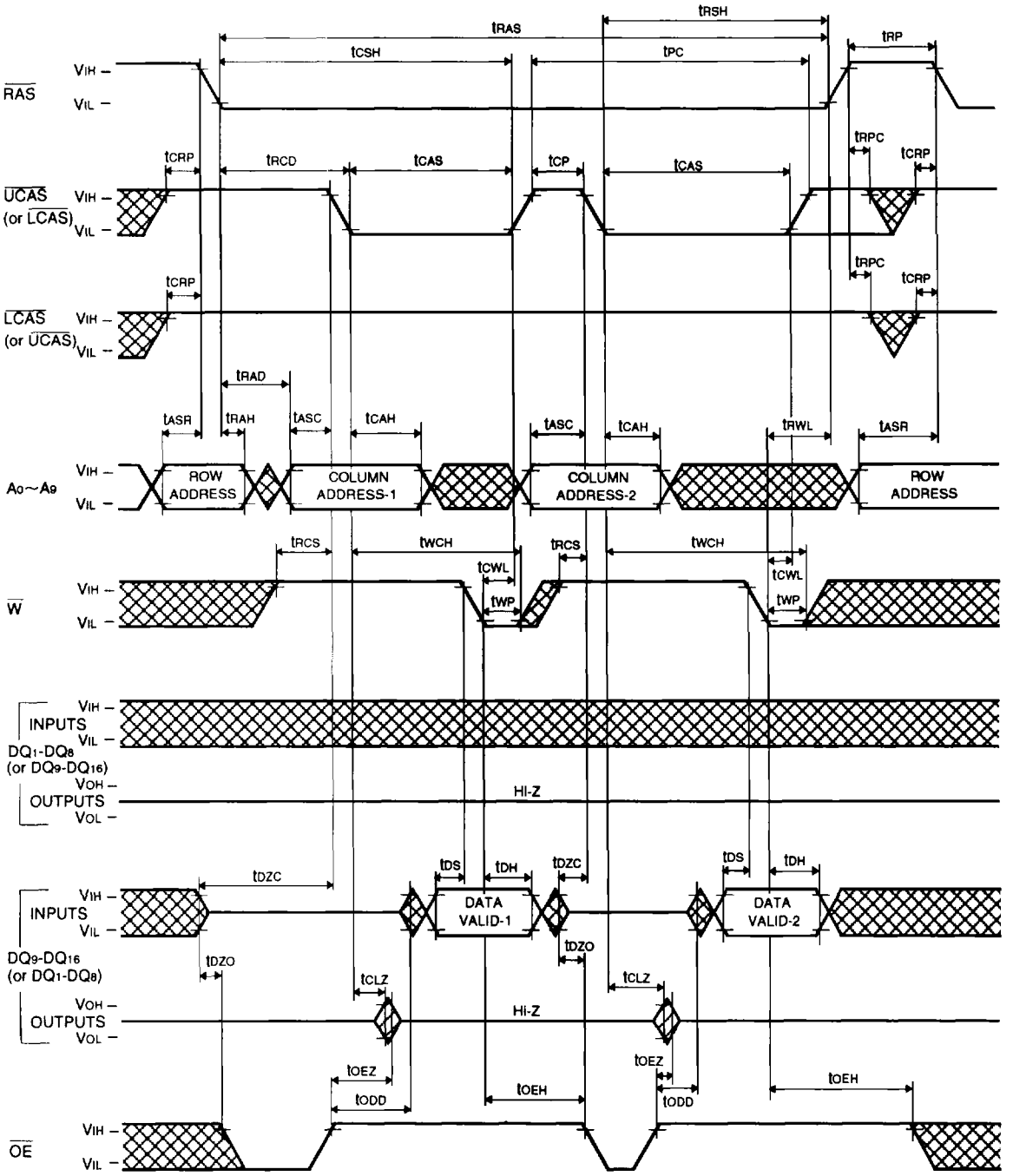
Fast Page Mode Upper / (Lower) Byte Write Cycle (Early Write)



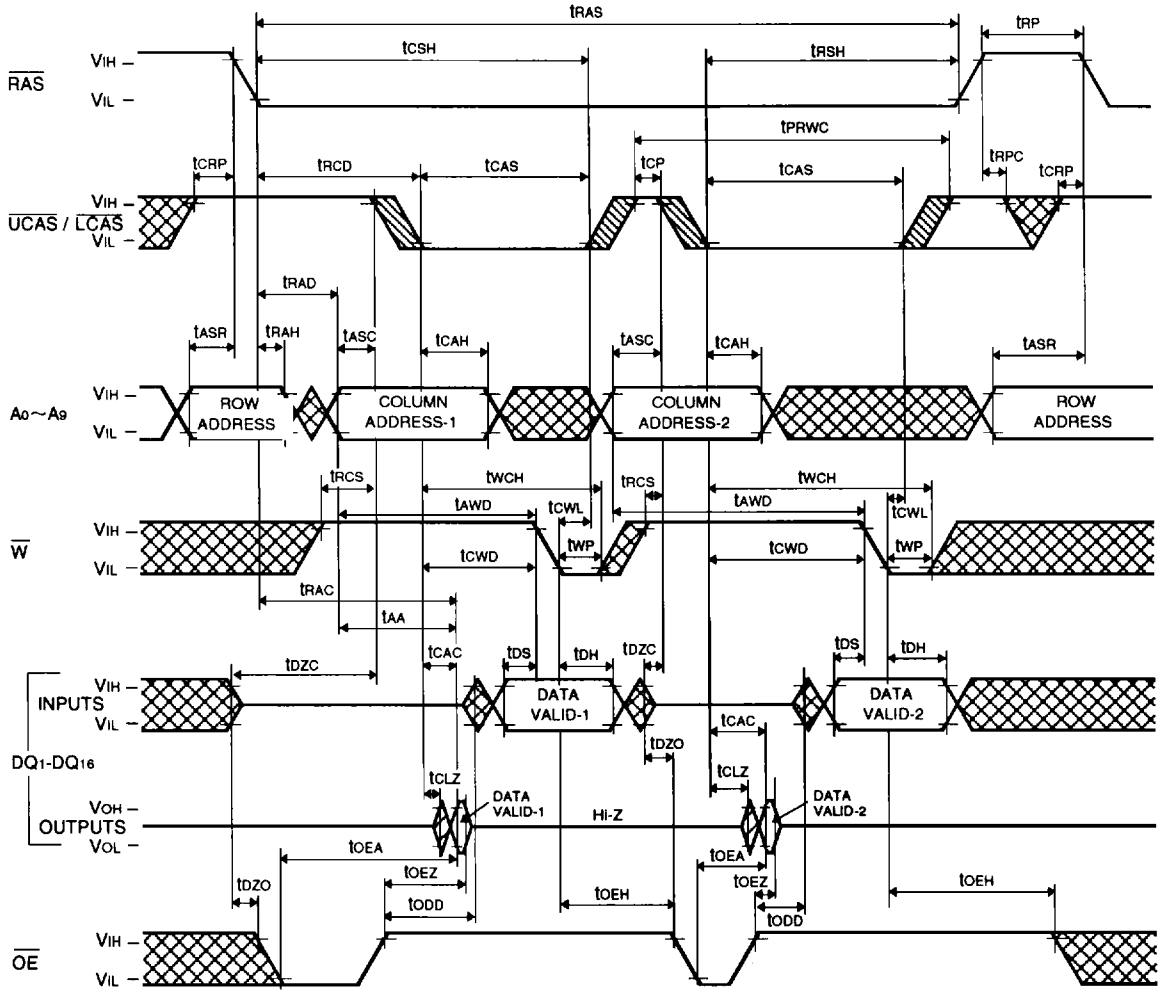
Fast Page Mode Write Cycle (Delayed Write)



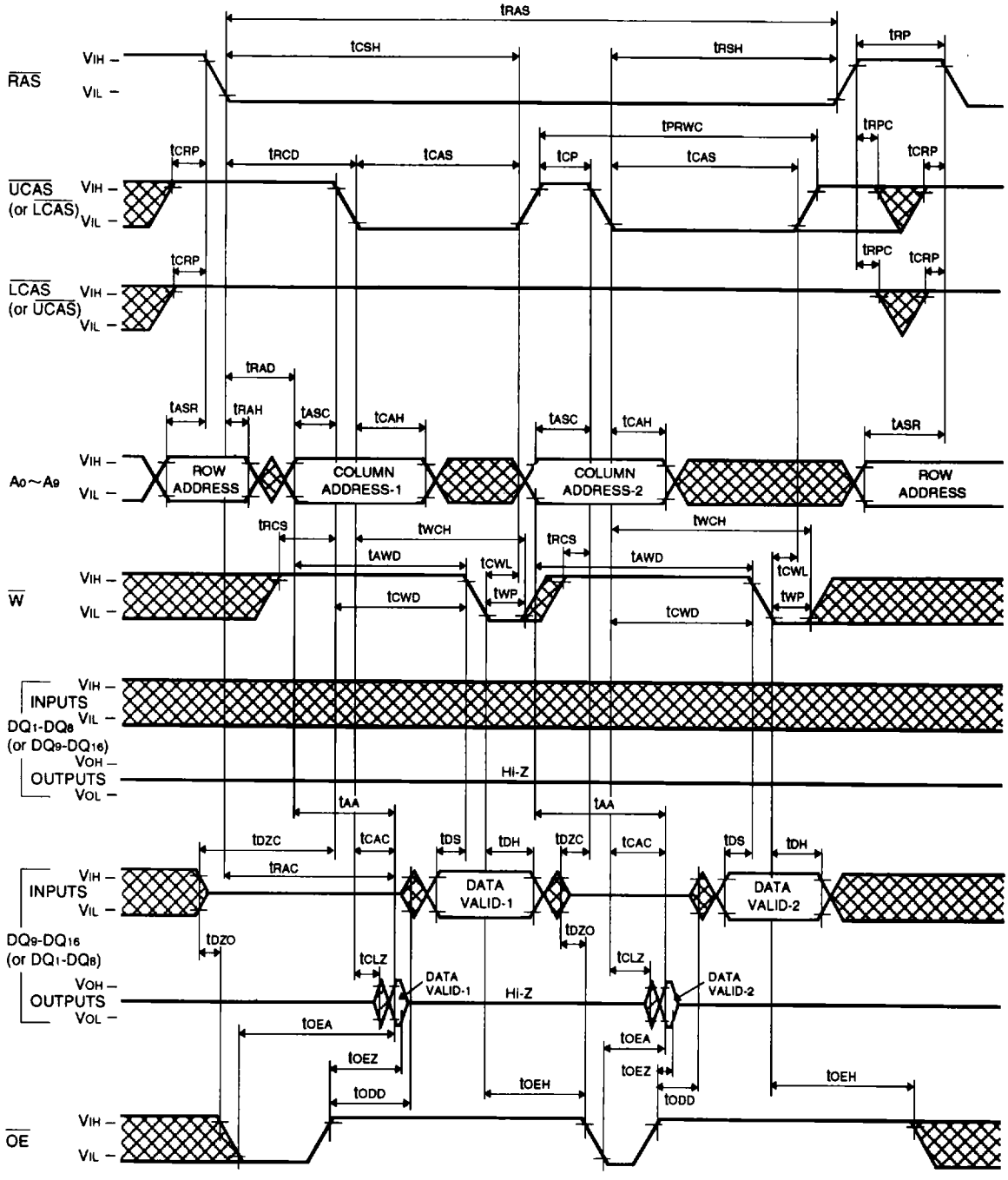
Fast Page Mode Upper / (Lower) Byte Write Cycle (Delayed Write)



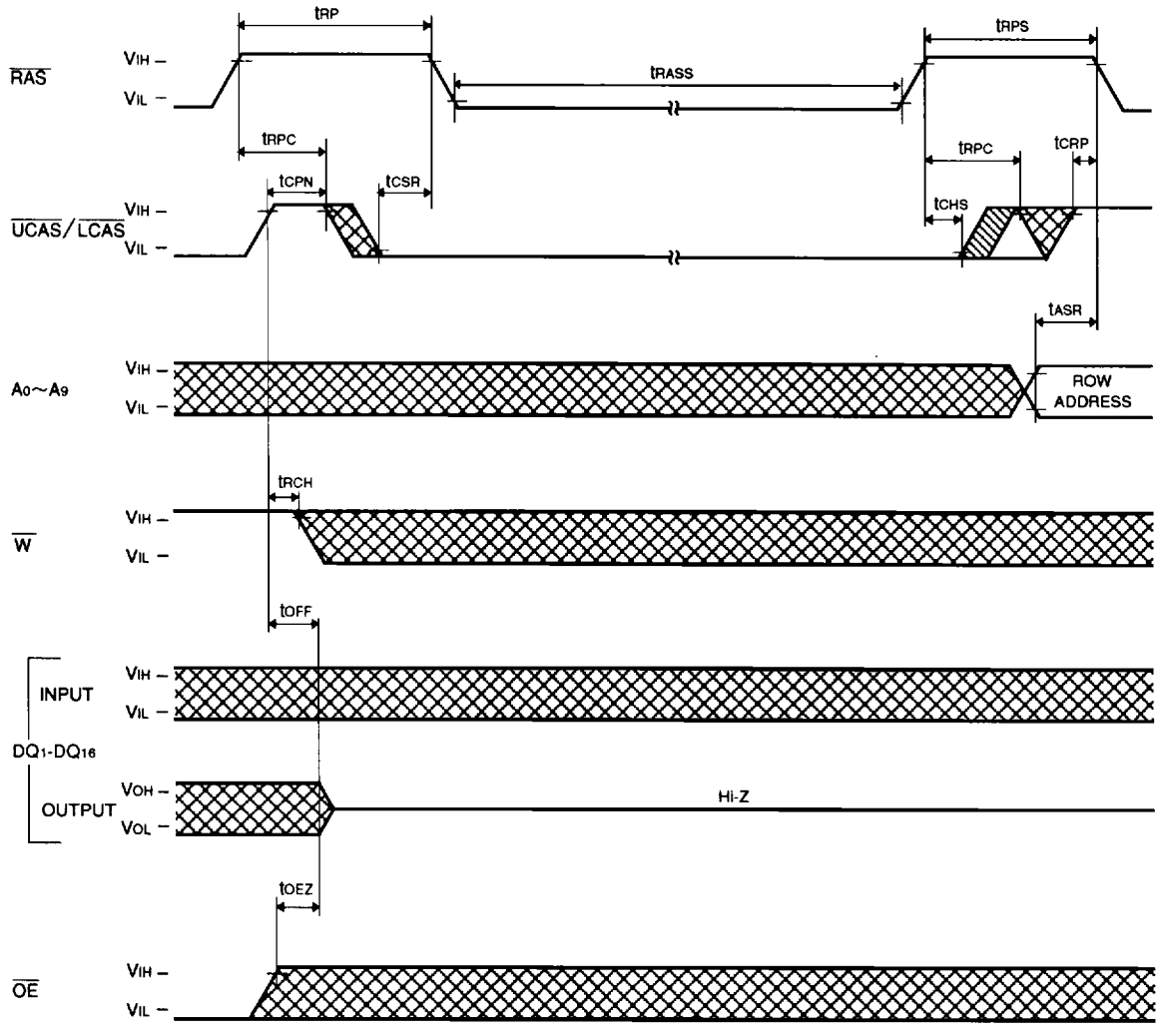
Fast Page Mode Read-Write, Read-Modify-Write Cycle



Fast Page Mode Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle



Self Refresh Cycle ∗



Upper / (Lower) Self Refresh Cycle*